Wuxi Sicomm Communication Technologies, Inc

SCT2400

2.4GHz Digital Voice and Data

Transceiver

Datasheet

Version: 2.0 Provisional

Date: 2019/05/02

Change History

| Version	Date	Change Description
1.0	2018-6-20	Preview
1.1	2018-11-16	Added Schematics (section 11)
2.0	2019-04-23	Added SMS support using external microcontroller information, Revised text

Table of Contents：

1. Overview

SCT2400 is a highly integrated RF transceiver and baseband chip for low-power, long range voice communications. The SCT2400 features a 2.4GHz band radio transceiver, supporting ultra-long-distance communication and strong anti-interference capabilities. The SCT2400 also integrates a voice and data transmission baseband core to handle the entire baseband processing. Interfacing to an external audio codec (ADC and DAC), it provides a complete physical and data link layer solution complying with Sicomm's Digital Family Radio (DFR) digital voice protocol, and most of the call control layer features. The DFR digital voice protocol is a proprietary digital voice protocol developed by Sicomm for the 2.4GHz band.

Figure 1-1 shows the use of the SCT2400 in a digital radio system.
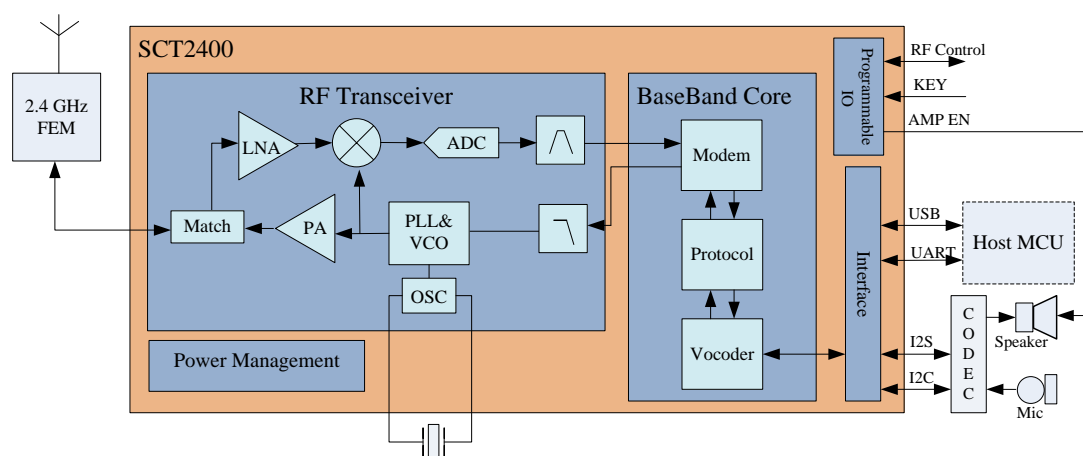
Figure 1-1   SCT2400 in Digital Radio System

The SCT2400 includes a set of I/O interfaces for connection of peripheral devices.

The SCT2400 connects to an external audio codec via a high speed I2S port for voice data and I2C for control. Additional UART and USB ports provide user interfacing, including support for customer programming, refer to the document *SCT2400 Test Guide and CPS Instructions*.

The SCT2400 includes a power management control module (built-in LDO). The typical operating voltage in the SCT2400 is 3.3V, and the typical I/O interface operating voltage is also 3.3V.

The SCT2400 is supplied in a 10 mm x 10 mm, 0.8 mm pitch BGA 144 package.

2. Features

2.4GHz RF Transceiver

- Meets all global 2.4GHz radio regulations including EN 300 440, FCC CFR 17 Part 15 and Japan's ARIB STD-T66

- Long Distance 2.4GHz Transceiver

- High sensitivity, up to -119 dBm during voice intercom

- Superior anti-interference ability

- High efficiency adjustable gain PA, maximum output +12 dBm

Baseband core

- Spread Spectrum Modulation Modem

- Air interface Physical Layer (Layer -1)

- Air interface Data Link Layer (Layer-2)

- Air Interface Call Control Layer (Layer-3)

- Sicomm DFR (Digital Family Radio) digital intercom communication protocol stack

- Built-in 3600bps low bit rate voice encoder implementing Advanced Forward Error Correction

Interface module

- One high speed serial port (I2S) for connection to Codec.

- One USB VCP (Virtual COM Port) for host communication control.

- One UART port for host communication control.

- Two I2C ports for external EEPROM and Codec.

- One VOX detection and one battery charge pin.

- One Beep tone output pin.

- One set of I/O interfaces to connect control devices such as peripheral keys.

Vocoder support

- 3600bps low bit rate vocoder

- High voice quality

- Noise suppression

- High error correction capability

Power Management Module

- Built-in linear LDO regulator

- Multiple receive operating modes to minimize current consumption

- 12.5mA Idle mode (scanning)

- 52.5mA current consumption in continuous receive mode

- 64mA current consumption in transmit mode

Package

- BGA144 package

- 0.8 mm ball pitch

- 10 mm x 10 mm outline

3. Pin Configuration

SCT2400 is supplied in a BGA144 package.

Pin assignment of SCT2400 is shown in Table 3-1 Pin List and 3-2 Pin Diagram:

Pin No.	Pin name	Type	Function
A1	I2C1_DAT	I/O	I2C1 data connect to external EEPROM
A2	I2C1_CLK	O	I2C1 clock connect to external EEPROM
A3	PE0	I/O	GPIO
A4	PB9	I/O	GPIO
A5	PB7_/PG (1)	I	Connect it to external Li-ion battery charger. Tie to VDDD if not used, refer to schematics in section 11
A6	PB3_/CHG (1)	I	Connect it to external Li-ion battery charger. Tie to VDDD if not used, refer to schematics in section 11
A7	TEST2	O	Test purpose only, leave open circuit
A8	SWCLK	I/O	SWCLK for MCU SWD port
A9	XTB	-	RF Reference oscillator connection
A10	XTA	-	RF Reference oscillator connection
A11	AVSS1	P	RF Ground
A12	VR_PA	O	Internal regulater output for internal PA, decouple with a 10nF capacitor to ground for stability
B1	OSC32IN	I	External 32.768 kHz oscillator connection to support an RTC function (not currently supported)
B2	PE3	I/O	GPIO
B3	PE1	I/O	GPIO
B4	BOOT0	I	Boot mode select

B5	PB6_KEY3 (2)	I	Connection for Function key
B6	PD7_KEY4 (2)	I	Connection for Function key
B7	TEST1	O	Test purpose only, leave open circuit
B8	TEST3	O	Test purpose only, leave open circuit
B9	AVSS2	P	RF Ground
B10	AVSS3	P	RF Ground
B11	VR_IN	I	Regulator input, connect to D8 VR_OUT
B12	RFIO	I/O	RF Transmit output and receive input
C1	OSC32OUT	O	External 32.768 kHz oscillator connection to enable support of an RTC function (not currently supported)
C2	PE4	I/O	GPIO
C3	PDR_ON	I	Connect to VDDD
C4	PB8_KEY2 (2)	I	Connection for Function key
C5	PB5	I/O	GPIO
C6	PD6	I/O	GPIO
C7	TEST4	O	Test purpose only, leave open circuit
C8	AVSS4	P	RF Ground
C9	AVSS5	P	RF Ground
C10	AVSS6	P	RF Ground
C11	AVSS7	P	RF Ground
C12	AVSS8	P	RF Ground
D1	NRESET	I	Chip Reset, active low

D2	PE5	I/O	GPIO
D3	VSSD1	P	Digital ground (base band)
D4	VDDD1	P	Digital power supply for base band
D5	PB4	I/O	GPIO
D6	PD5	I/O	GPIO
D7	VDDD2	P	Digital power supply for base band
D8	VR_OUT	O	Regulator output, connect to B11 VR_IN
D9	AVSS9	P	RF Ground
D10	AVSS10	P	RF Ground
D11	VDD_RF1	P	Power supply for RF
D12	AVSS11	P	RF Ground
E1	PC1	I/O	GPIO
E2	VBAT	P	Backup Operating Voltage
E3	VDDD3	P	Digital power supply for base band
E4	VSSD2	P	Digital ground of base band
E5	VSSD3	P	Digital ground of base band
E6	VDDD4	P	Digital power supply for base band
E7	VSSD4	P	Digital ground of base band
E8	AVSS12	P	RF Ground
E9	VR_SW	-	Leave open circuit
E10	VDD_RF2	P	Power supply for RF
E11	VDD_RF3	P	Power supply for RF

E12	VDD_RF4	P	Power supply for RF
F1	PC2	I/O	GPIO
F2	PC13_KEY1 (2)	I	Connection for Function key
F3	VDDD5	P	Digital power supply for base band
F4	VSSD5	P	Digital ground of base band
F5	VDDD6	P	Digital power supply for base band
F6	VSSD6	P	Digital ground of base band
F7	VSSD7	P	Digital ground of base band
F8	VSSD8	P	Digital ground of base band
F9	VCAP2	O	Connect a ceramic 2.2uF capacitor to ground
F10	SWDIO	I/O	SWDIO for MCU SWD port
F11	USB_FS_DP	I/O	USB interface positive
F12	USB_FS_DM	I/O	USB interface negative
G1	PC3_PTT	I	Connect to PTT button
G2	OSCIN	I	Connect to external oscillator which is optional, please check section 10.1 for more details
G3	VDDD7	P	Digital power supply for base band
G4	VSSD9	P	Digital ground of base band
G5	VSSD10	P	Digital ground of base band
G6	VSSD11	P	Digital ground of base band
G7	VSSD12	P	Digital ground of base band
G8	UART_TX	O	UART transmitter

G9	UART_RX	I	UART receiver
G10	PA8_CHL	O	Used for 2.4 GHz FEM control, leave open circuit if not used
G11	PC9_CTX	O	Used for 2.4 GHz FEM control, leave open circuit if not used
G12	PC8_CPS	O	Used for 2.4 GHz FEM control, leave open circuit if not used
H1	VREFP	P	Connect to VDDA recommended
H2	VSSA	P	Analog ground of base band
H3	PC0	I/O	GPIO
H4	OSCOUT	O	Connect to external oscillator which is optional, please check section 10.1 for more details
H5	VSSD13	P	Digital ground (base band)
H6	VSSD14	P	Digital ground (base band)
H7	VSSD15	P	Digital ground (base band)
H8	VDDD8	P	Digital power supply for base band
H9	PD15	I/O	GPIO
H10	PD14	I/O	GPIO
H11	I2S_MCLK	O	I2S master clock out
H12	PC7_CRX	O	Used for 2.4 GHz FEM control, leave open circuit if not used
J1	PA0	I/O	GPIO
J2	VDDA	P	Analog power supply for base band
J3	VDDD9	P	Digital power supply for base band

J4	VSSD16	P	Digital ground (base band)
J5	VSSD17	P	Digital ground (base band)
J6	VSSD18	P	Digital ground (base band)
J7	VSSD19	P	Digital ground (base band)
J8	VSSD20	P	Digital ground (base band)
J9	PD11	I/O	GPIO
J10	PD10	I/O	GPIO
J11	PD12	I/O	GPIO
J12	PD13_CSD	O	Used for 2.4 GHz FEM control, leave open circuit if not used
K1	BEEP_OUT	O	PWM Beep output
K2	PA1	I/O	GPIO
K3	PA2	I/O	GPIO
K4	BYPASS_REG	I	Connection to VSSD recommended
K5	VDDD10	P	Digital power supply for base band
K6	VSSD21	P	Digital ground (base band)
K7	VDDD11	P	Digital power supply for base band
K8	VSSD22	P	Digital ground (base band)
K9	VDDD12	P	Digital power supply for base band
K10	I2S_SDO	O	I2S Data output
K11	PD8	I/O	GPIO
K12	PD9	I/O	GPIO

L1	VOX_DET	AI	VOX detect voltage input
L2	BAT_DET	AI	Battery volatage detect
L3	PA6	I/O	GPIO
L4	PC5	I/O	GPIO
L5	PE8	I/O	GPIO
L6	PE12	I/O	GPIO
L7	I2C2_CLK	O	I2C2 clock connection to external codec
L8	I2C2_SDA	I/O	I2C2 data connection to external codec
L9	VCAP1	O	Connect a 2.2uF capacitor to ground
L10	I2S_WCK	O	I2S Word clock
L11	I2S_BCK	O	I2S Bit clock
L12	I2S_SDI	I	I2S Data input
M1	PA7	I/O	GPIO
M2	PC4	I/O	GPIO
M3	PB0/RX_LED (3)	I/O	Used for RX status LED control
M4	PB1/TX_LED (3)	I/O	Used for TX status LED control
M5	BOOT1	I	Connection to VSSD recommended
M6	PE7	I/O	GPIO
M7	PE9	I/O	GPIO
M8	PE10_EN2 (4)	I	Connect to channel switch
M9	PE11_EN3 (4)	I	Connect to channel switch
M10	PE13_AMPEN	O	External audio PA enable

M11	PE14_EN1 (4)	I	Connect to channel switch
M12	PE15_EN0 (4)	I	Connect to channel switch

Table 3-1   SCT2400 Pin List

1) The /PG and /CHG pins are used to detect the charging status of the external lithium battery charging IC. Please refer to Chapter 11 Reference Schematic Diagram for details.

2) KEY1-KEY4 is used to connect external function keys. The functions of the keys may be configured by the upper computer software. Please refer to Chapter 6 for details.

3) The RX_LED and TX_LED are used to indicate the status of receiving and transmission, respectively, and they are multiplexed as the charging status indicator of the external lithium battery charging IC. The RX_LED is multiplexed as the charging end indication, and the TX_LED is multiplexed to indicate that the charging is in progress. Refer to the reference application schematic in Chapter 11 for details.

4) EN0-EN3 is used to connect external channel coding switches. If 2-wire channel coding switch is used, connect to EN0 and EN1. If using 4-wire channel coding switch, connect EN0-EN3. Please refer to the Reference Schematic Diagram in Chapter 11 for details.

	1	2	3	4	5	6	7	8	9	10	11	12
A	I2C1_DAT	I2C1_CLK	PE0	PB9	PB7	PB3	TEST2	SWCLK	XTB	XTA	AVSS	VR_PA
B	OSC32IN	PE3	PE1	BOOT0	PB6	PD7	TEST1	TEST3	AVSS	AVSS	VR_IN	RFIO
C	OSC32OUT	PE4	PDR_ON	PB8	PB5	PD6	TEST4	AVSS	AVSS	AVSS	AVSS	AVSS
D	NRESET	PE5	VSSD	VDDD	PB4	PD5	VDDD	VR_OUT	AVSS	AVSS	VDD_RF	AVSS
E	PC1	VBAT	VDDD	VSSD	VSSD	VDDD	VSSD	AVSS	VR_SW	VDD_RF	VDD_RF	VDD_RF
F	PC2	PC13	VDDD	VSSD	VDDD	VSSD	VSSD	VSSD	VCAP2	SWDIO	USB_DP	USB_DM
G	PC3	OSCIN	VDDD	VSSD	VSSD	VSSD	VSSD	UART_TX	UART_RX	PA8	PC9	PC8
H	VREFP	VSSA	PC0	OSCOUT	VSSD	VSSD	VSSD	VDDD	PD15	PD14	I2S_MCLK	PC7
J	PA0	VDDA	VDDD	VSSD	VSSD	VSSD	VSSD	VSSD	PD11	PD10	PD12	PD13
K	BEEP_OUT	PA1	PA2	BYPASS_REG	VDDD	VSSD	VDDD	VSSD	VDDD	I2S_SDO	PD8	PD9
L	VOX_DET	BAT_DET	PA6	PC5	PE8	PE12	I2C2_CLK	I2C2_DAT	VCAP1	I2S_WCK	I2S_BCK	I2S_SDI
M	PA7	PC4	PB0	PB1	BOOT1	PE7	PE9	PE10	PE11	PE13	PE14	PE15

Table 3-2   SCT2400 Pin Diagram

4. RF Transceiver

The SCT2400 chip has a built-in half-duplex RF transceiver that can work in the global 2.4GHz ISM band. It implements a high-efficiency transmitter, supporting a maximum output power of +12dBm and a high-linearity receiver. RF signals can be input and output via common port pins. IF signal is generated from the RF signal via the Rx mixer and is digitised by subsequent ADC then entering the baseband for demodulation. The mixer's local oscillator signal is provided by a built-in VCO and a fractional divider PLL with a 52 MHz external crystal reference clock. In transmit the baseband signal is modulated by a direct digital modulation via a pre-filter, then the modulated RF signal is amplified by the PA for transmission. A transmit and receive switch has been integrated within the transceiver. The input and output RF signals all pass through the same pin.

The data communication process for RF transceiver and baseband core is described in Chapter 5, Sections 5.3.1 and 5.3.2.
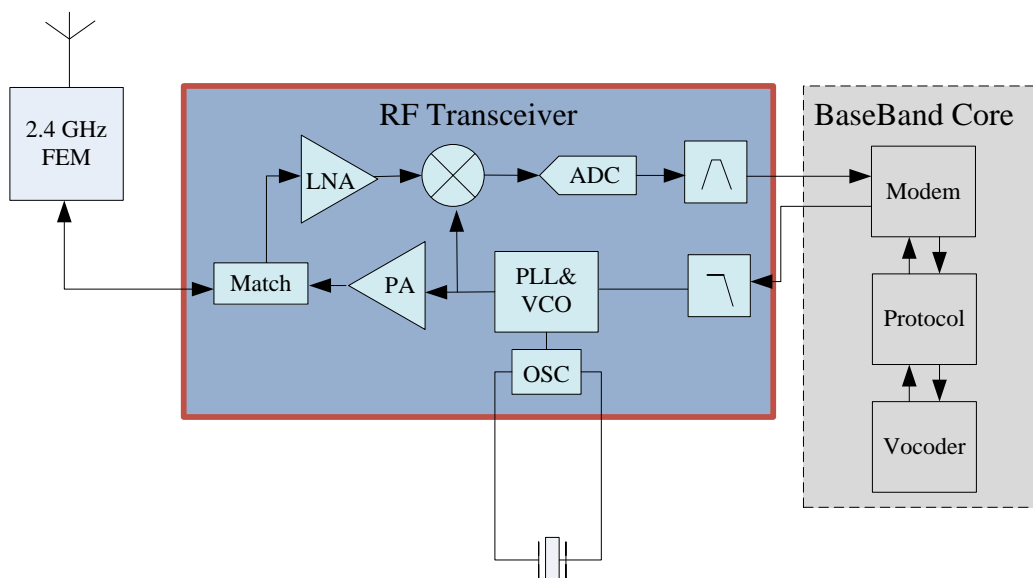

Figure 4-1   SCT2400 RF Transceiver Diagram

4.1. Transmitter

The transmit signal is directly modulated by the fractional frequency PLL after being output by the baseband core modem. Transmitter RF output power can be controlled in 1dB increments from -18dBm to +12dBm, which corresponds to the RF output power at the reference design antenna feed point (see Chapter 11 "Reference Schematic Diagram"). Sudden switching of RF power amplifier gains leads to unwanted spurious spectrum. Therefore, a precision DAC is used as a reference for the power supply of a transceiver power amplifier, which allows a smooth transition of transmit power to the target transmit power. The slope time for the PA to turn on and off can vary from 2 to 20 µs, before data transmission. In some applications and for regulatory testing

purposes, it may be useful to generate continuous carrier (CW) or enable continuous modulation output in transmit mode. These two functions can be set through the SCT2400 interface command control, which outputs an RF signal containing alternating logic "1" and "0" modulation data streams. Please refer to the document "*SCT2400 Packet Interface*" for more details.

4.2. Receiver

SCT2400 has built-in half-duplex Low IF/Zero IF receiver. The received RF signal is first amplified by the LNA through an on-chip impedance matching circuit, followed by a single-end to differential conversion to improve the receiver's second-order linearity. The signal is then converted to Zero IF or near Zero IF through a quadrature mixer to obtain I and Q signals. Then these signals are low-pass filtered and eventually digitized. The receiver link uses default enabled automatic gain control (AGC) to ensure that the best front-end gain is selected for receiving a given detection signal power.

The transceiver reports the signal strength by using the Received Signal Strength Indicator (RSSI) when a DFR signal or packet is received. This information can be obtained through the corresponding control interface command. For more details, please refer to the document "*SCT2400 Packet Interface*".

4.3. PLL&VCO

A third-order $\Sigma-\triangle$ fractional divider PLL works as a frequency synthesizer for the LO (Local Oscillator) of the receiver and transmitter. The PLL can perform fast auto-calibration to reduce switching time. The digital direct modulation of transmit data is also done by this PLL. The PLL Reference Frequency is from an external 52MHz crystal reference. The PLL settings and reference frequency will determine the RF center frequency. With a Reference Frequency of 52MHz, the chip RF default frequency is set to 2.4GHz.

RF center frequency of the transceiver can be set by via corresponding control command interface, and the frequency is set as 32-bit operand in Hz. For more details, please refer to the document "*SCT2400 Packet Interface*".

4.4. RC Oscillator

The SCT2400 has a built-in RC oscillator. The transceiver can use the internal 64 kHz RC oscillator in sleep mode to wake up the transceiver periodically or in duty cycle operation mode, which allows the device to be configured without turning on the crystal oscillator. The built-in oscillator has lower power consumption in sleep mode. A crystal oscillator can be used in place of the RC oscillator, except in the sleep mode.

4.5. RF Front-end circuit

The SCT2400 integrates transmit and receive switches and RF front-end circuits such as PA and LNA. The SCT2400 radio transceiver provides a maximum transmitter output power of up to +12 dBm and a receiver sensitivity of -119 dBm. If the user has a higher link budget, an additional 2.4 GHz Front End Module (FEM) can be added to the SCT2400's RF input and output ports to further increase performance (subject to applicable spectrum access regulations). In receiving mode, sensitivity can be improved to -123dBm.

For more details, please refer to the Schematic Diagram in Chapter 11.

5. Baseband Core

5.1. Overview

The SCT2400 baseband core mainly consists of modulation and protocol stacks.

5.2. Modem

The SCT2400 modem provides long-distance communication based on spread spectrum modulation. Compared to conventional FSK-based or OOK-based modulation, SCT2400 modem uses both spread-spectrum modulation and forward error correction (FEC) techniques to increase the range and robustness of radio communication links.

An important feature of SCT2400 modem is its superior anti-jamming performance. It can provide up to 15 dB suppression capability in same frequency channel. This anti-jamming capability allows the SCT2400 modulation system to co-exist in mixed communication networks; SCT2400 modulation ensures range and robustness in case where conventional modulations fail.

For any spread-spectrum device, each symbol of the payload information is represented via multiple information chips in the modulation. The Spreading Factor (SF) determines the ratio between the Symbol Rate (Rs) and the Chip Rate (Rc). The modem within the SCT2400 is dedicated to supporting the DFR functionality so the setting of the spreading factor (SF) is fixed. The table below shows the receiver sensitivity of the SCT2400 single chip.

PER	Receive Sensitivity(dBm)
1%	-119

Table 5-1　Receiver Sensitivity of SCT2400

5.3. DFR Protocol Stack

The SCT2400 supports the physical layer (Layer 1), data link layer (Layer 2), and DFR call control layer (Layer 3), and implements dialing rules in the appendix of this document. The protocol layer is shown in the figure below:
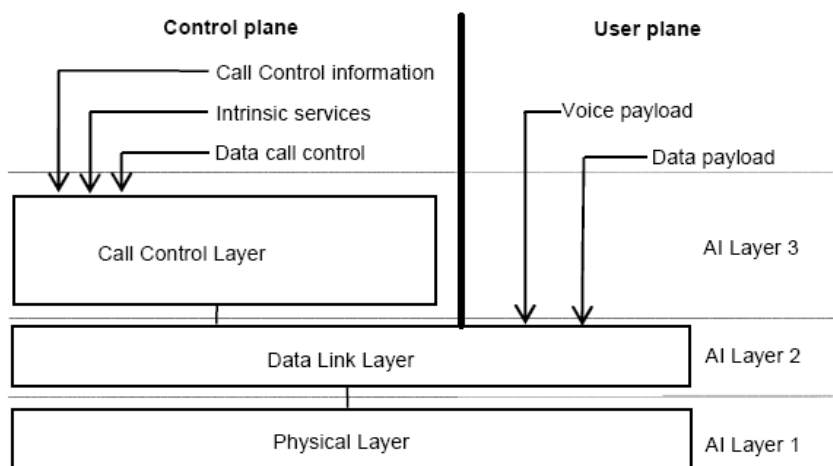
Figure 5-1   DFR Protocol Structure

More specifically, the following is the implementation of the SCT 2400 at each air interface layer:

Air Interface Physical Layer（Layer-1）

1.   Modulation and demodulation with programmable modulation index

2.   Definition of bit and symbol

3.   Frequency and Compliance

4.   Framing and decoding frame

Air Interface Data Link Layer（Layer-2）

1.   Channel coding (FEC, CRC)

2.   Interleaving, de-interleaving and bit sequence

3.   Creation of frame and super frame, and synchronization

4.   Transmission frame and parameter's definition

5.   Call address (source and destination)

6.   Voice application (vocoder data) and physical layer interfaces

7.   Data Bearer Service

8.   Exchange signaling and user data with the call control layer

**Air Interface Call Control Layer (Layer-3)**

1. Establishment, maintenance and termination of calls

2. Single call, group call's transmission and reception

3. Addressing of target address

4. Incoming call ID automatic matching

5. Delayed call support

DFR ISF (Annex A) Support

1. Full support for standard user interfaces (defined in Appendix A of this document)

2. Allow dialing with "*" group calls

3. Dial syntax check

5.3.1.DFR Transmitter Signal Flow

The signal flow at the transmitter is as shown in Figure 5-2 below:
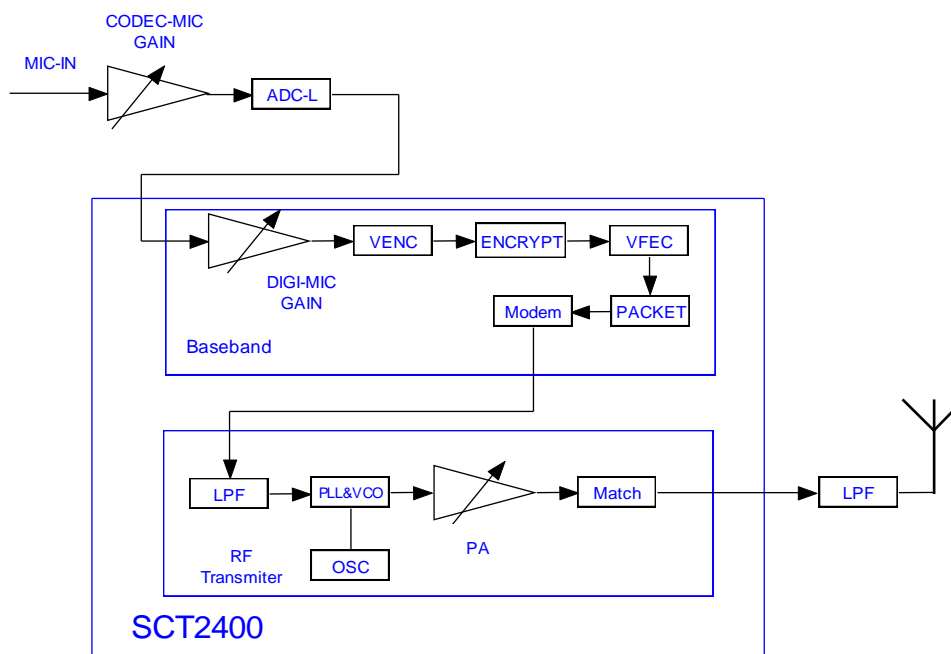
Figure 5-2   DFR Transimitter Signal Flow

The microphone signal is amplified by a VGA (Variable Gain Amplifier) on the external codec, converted into a digital signal by the codec, and stored in the left input channel buffer of the SCT2400. The digitized signal is processed as follows:

1. DIGI_MIC_GAIN, microphone digital gain, used to amplify or reduce the microphone signal,

usually to reduce the saturation of the microphone signal

2. VENC, Voice encoder, compresses voice signal to 2400 bit rate compressed signal

3. ENCRYPT, Password-configurable encryption module

4. VFEC, voice coding module, 1200 bit rate error correction code to make up 3600 bit rate signal

5. PACKET, framing, adding protocol control information

6. Modem modem

7. LPF, optional pre-configured filter to improve adjacent channel power effects

8. PLL&VCO, A $\Sigma-\triangle$ (third-order sigma-delta) fractional divider PLL as the frequency synthesizer for the LO (Local Oscillator) of the receiver and transmitter chain

9. PA, RF Output Power Amplifier, Controllable in 1 dB increments from -18 dBm to +12 dBm

10. Match, integrated matching circuit, which generates RF signals through internal processing, can be connected with an antenna port, and an RF half-duplex operation can be implemented without an external RF switch.

5.3.2. DFR Receiver Signal Flow

The figure below shows the signal flow at the receiving end of the DFR:
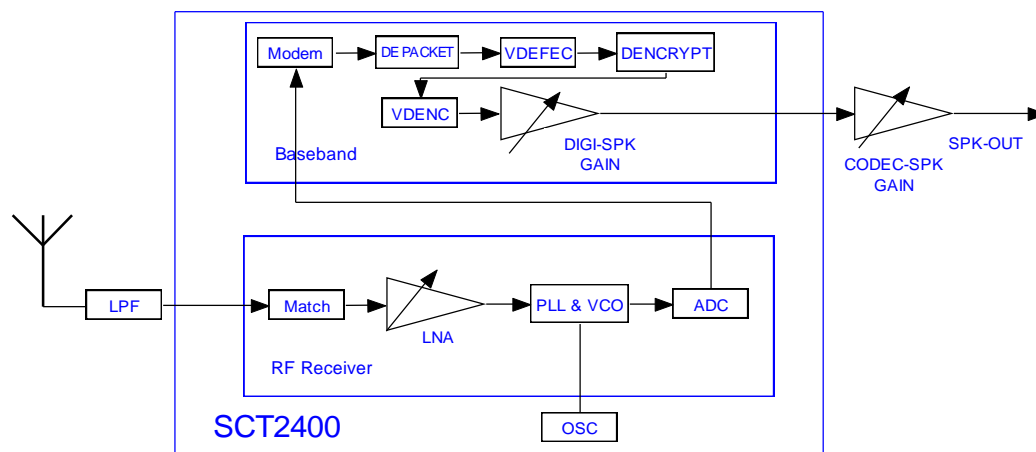
Figure 5-3   DFR Receiver Signal Flow

The digital signal reception process is shown as follows:

1. MATCH, integrated matching circuit

2. LNA, Built-in Low Noise Amplifier

3. PLL & VCO, A third-order $\Sigma-\triangle$ fractional divider PLL as a frequency synthesizer for the

LO (local oscillator) of the receiver and transmitter link.

4. Modem, modem

5. DEPACK, protocol to de-frame, extract control and voice information

6. DFEC, channel solution decoding module, extracting compressed voice signals

7. DECRYPT, decryption

8. VDEC, voice decoder, decoded voice signal

9. DIGI SPK-Gain, Audio Output Digital Gain

The received RF signal is amplified by the LNA through the built-in impedance matching circuit of the SCT2400, and then single-ended to differential conversion is performed to improve the second-order linearity of the receiver. The signal is then down-converted to ZIF (Zero Intermediate Frequency) or near ZIF through a quadrature mixer to obtain I and Q signals, which are then low-pass filtered and eventually digitized. The receive link uses default enabled automatic gain control (AGC) to ensure that the best front-end gain is selected for receiving a given detected signal power.

I/Q signal is converted to a digital signal by an ADC and input to the modem. After demodulation, the protocol stack is parsed. The built-in voice encoder decodes and outputs the voice signal, which is converted to analog by an external codec and amplified by CODEC_SPK_GAIN on the codec and finally given to the audio PA output.

6. Programmable Function Keys

SCT2400 provides 4 programmable function keys. With the host computer software (Sicomm CPS), each key can be independently configured, and the default configuration function is described in the following table.

PIO Function	I/O	Index Value	Description
FUNC_KEY1	I	0	Programmable function key1
FUNC_KEY2	I	1	Programmable function key2
FUNC_KEY3	I	2	Programmable function key3
FUNC_KEY4	I	3	Programmable function key4

Table 6-1   Default Key Function

Table 6-2 lists the functions that can be assigned to the 4 programmable function keys of SCT2400:

Function	Description
CH+	Make the channel number increase
CH-	Make the channel number decrease
VOL+	Make the audio output volume increase
VOL-	Make the audio output volume decrease
SCAN ON/OFF	Start or Stop scan the channel
Emergency Call	Start an emergency call
Remote Stun	Remote stun
Remote Revival	Remote revival
Remote Monitor	Remote monitor

Table 6-2   List of Programmable Function Keys

Grey text indicates options not currently supported

7. Control Command Protocol

The Control Command interface Protocol defines the physical interface between the SCT2400 and the external programming device (USB, COM port). For the two different physical interfaces, the form of the control command interface is exactly the same. The details of the command are defined individually in document: *"SCT2400 Packet Interface"*

8. Interface and Timing Sequence

This chapter provides timing information for the operation of the SCT2400. It contains the following sections:

- Section 8.1   Power Supply

- Section 8.2   Reset and Power Up Timing

- Section 8.3   I2S High-speed Serial Port Timing

- Section 8.4   I2C Interface

- Section 8.5   USART Interface

- Section 8.6   USB Interface

- Section 8.7   Other Interfaces

8.1. Power Supply

The SCT2400 has four power supplies, which are described below

- VSSD, VDDD operating voltage range 1.8V to 3.6V, a typical value of 3.3V, and is the baseband main power. The internal power monitor is enabled by holding the PDR_ON pin high, so connecting the PDR_ON pin to VDDD is recommended. This feature has an integrated power-on reset (POR)/power-down reset (PDR) circuit and brown-out reset (BOR) circuit.

- VSSA, VDDA operates from 1.8V to 3.6V，with typical value of 3.3V, and is the analog power supply for the ADC, reset module, RC oscillator and PLL. The voltage difference between VDDA and VDDD must not exceed 300mV, so it is recommended that VDDA and VDDD be powered by the same power supply, and isolated from each other.

- The VBAT operating voltage range is 1.8V to 3.6V, with a typical value of 3.3V. Recommended to connect VBAT to VDDD

- AVSS, VDD_RF operating voltage range is 1.8V to 3.6V, with a typical value of 3.3V. It is the SCT2400 internal RF transceiver power supply. In practice, it is necessary to perform decoupling processing and isolate the baseband power supply.

8.2. Reset and Power Up Timing

8.2.1.Baseband Core Operating Frequency

Baseband core uses an internal 16MHz RC oscillator that is factory trimmed to provide ±1% accuracy at 25°C. The RC oscillator is clocked into the baseband PLL and the system operating frequency is multiplied to 96 MHz. The baseband core clock frequency is kept at 96 MHz while the baseband core is active.

8.2.2.BOOT Mode

At startup, the BOOT pins are used to select one of two boot options. The specific true value is shown in the following Table 8-1:

- Start from main storage space
- Start from system storage space

BOOT1	BOOT0	BOOT MODE	Description
x	0	Main storage space	Start from main storage space
0	1	System storage space	Start from system storage space

Table 8-1   BOOT Mode Selection

The status of the BOOT0 and BOOT1 pins is captured on the rising edge of the fourth system clock after a system reset to determine which boot mode to use. The normal operating mode of the SCT2400 is to boot from the main storage space. When it is necessary to upgrade the chip firmware, the SCT2400 needs to boot from the system memory space. The boot loader is located in the system memory. It is used to reprogram the flash memory by using the UART or DFU (device firmware upgrade). As for the chip firmware upgrading, please refer to the document *SCT2400 Test Guide and CPS Instructions*.

## 8.3. I2S High-speed Serial Port Timing

The I2S high-speed serial port on the SCT2400 is preconfigured to allow connection to an external audio codec. With this connection the SCT2400 provides clock and synchronization signals. For the SCT2400, both I2S_CK and I2S_WS are output signals. SCT2400 provides the output MCLK clock signal which can be used as the main clock source for the codec. MCLK output frequency is fixed: 8 * 256 kHz.

The I2S connection pin configuration in SCT2400 is shown below in Table 8-2:

Pin Number	I2S Interface name	I/O
L10	I2S_WCK	O
L11	I2S_BCK	O
L12	I2S_SDI	I
K10	I2S_SDO	O
H11	I2S_MCLK	O

Table 8-2   I2S Pin Configuration

I2S Serial Interface format and Configuration Parameter is shown as Figure 8-1 and Table 8-2:
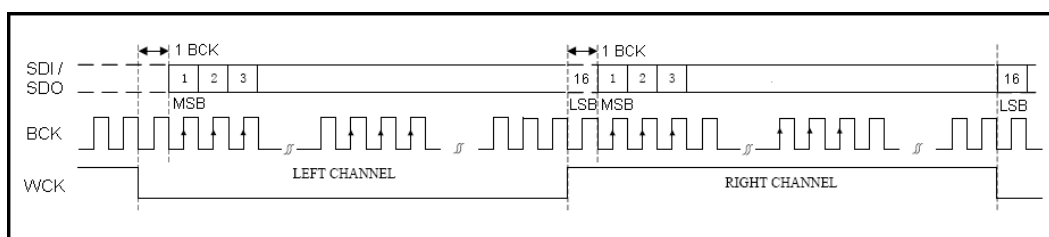
Figure 8-1   I2S Interface Data Format

Master-Slave Mode	I2S Host
Interface Mode	Standard I2S Mode
Sampling Rate	8 kHz
Bit Clock Rate	256 kHz
Number of Channel	2 (Stereo)
Format	PCM
Number of Bits per Channel	16

Table 8-3   Codec I2S Configuration

Figure 8-1 shows Communication Timing of SCT2400 in the current I2S Connection Configuration.
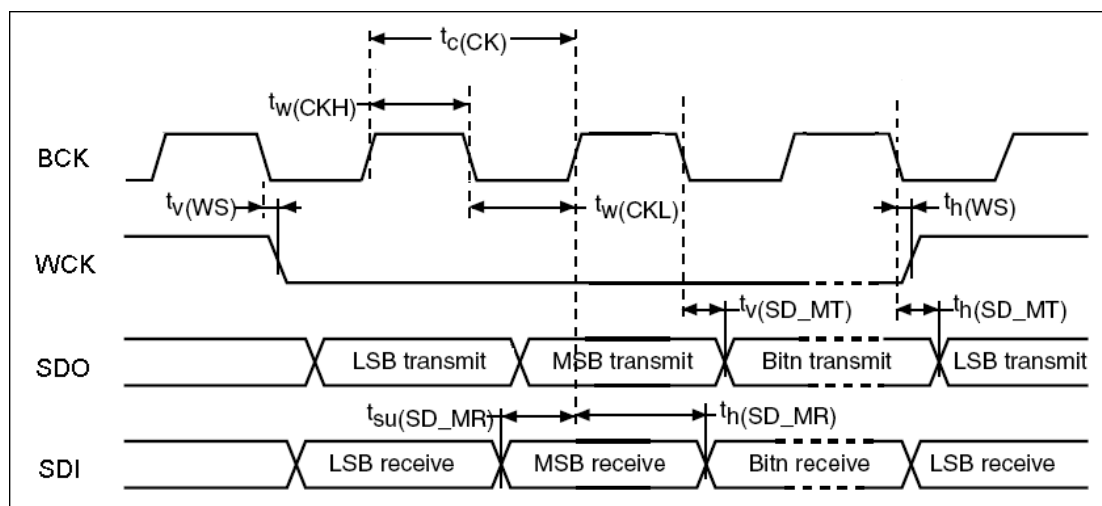
Figure 8-2 Codec Serial Port Transimission Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCLK}	I2S Main clock	-	-	256 x FS	-	kHz
f_{CK}	I2S Clock	16bit	-	32 x FS	-	kHz
D_{CK}	I2S clock duty cycle	Master mode	-	50	-	%
$t_{v(ws)}$	WCK valid time	Master mode	0	-	7	ns
$t_{h(ws)}$	WCK hold time	Master mode	1.5	-	-	ns
$t_{su(SD\_MR)}$	DI setup time	Master receive	1	-	-	ns
$t_{h(SD\_MR)}$	DI hold time	Master receiver	7	-	-	ns
$t_{su(SD\_MT)}$	DO setup time	Master transmitter	-	-	6	ns
$t_{h(SD\_MT)}$	DO hold time	Master transmitter	6	-	-	ns

Table 8-4 I2S Serial Port Transmission Timing Value

8.4. I2C Interface

There are two sets of I2C interfaces in the SCT2400, where I2C1 is configured to connect an external EEPROM (default setting) for storage of user channel settings. I2C2 is pre-configured to connect to an external codec for codec control purposes. In this connection the SCT2400 acts as a

master clock signal, using the standard (up to 100 kHz) rate mode.

I2C connection pin configuration in SCT2400 is as below:

Pin	Pin Name	I/O	Function
A1	I2C1_DAT	I/O	Connect external EEPROM for user to store some channel settings
A2	I2C1_CLK	O	
L7	I2C2_CLK	O	Connect external Codec to initialize Codec
L8	I2C2_DAT	I/O	

Table 8-5   I2C Pin Configuration

8.5. UART Interface

The SCT2400 provides a UART interface as an external communication interface. The UART interface is a universal asynchronous interface. The fixed configuration is: baud rate is 38400 bit/s, stop bit is 2 bits, data bit is 8 bits, parity check is turned off.

UART connection pin configuration in SCT2400 is as below:

Pin	UART Interface Name	I/O	Function
G8	UART_TX	O	Host control interface, can also use this interface to complete SCT2400 firmware upgrade
G9	UART_RX	I	

Table 8-6   USART Pin Configuration

8.6. USB Interface

The SCT2400 supports USB OTG Full-Speed Device/Host/OTG Peripheral with Integrated Transceiver built in. The USB OTG FS peripheral conforms to USB 2.0 and OTG1.0 specification. The USB interface has software configurable endpoint settings and supports suspend/resume. The built-in USB OTG interface in the SCT2400 chip has been packaged as a virtual communication port VCP. To know how the host (PC) communicates with the SCT2400 through the VCP port, please refer to the VCP driver installation related documentation.

USB connection pin configuration in SCT2400 is as below:

Pin	Pin Name	I/O	Function
F12	USB_DM	I/O	Upper computer control interface, also used to complete SCT2400 firmware upgrade
F11	USB_DP	I/O	

Table 8-7   USB Pin Configuration

8.7. Other Interfaces

For user's convenience, SCT2400 also provides VOX detection, battery power detection and sound output interface.

- VOX detection, this function must work together with the external VOX circuit. For the recommended VOX circuit, refer to the Schematic Diagram in Chapter 11. This function is monitored by one of input pins of the chip's internal ADC (Pin L1 VOX_DET). The maximum input voltage is 3.0V. The SCT2400 determines whether to start the transmission according to the voltage detected by this pin. The threshold of this voltage can be modified using the SCT2400 CPS programming software.

- Battery charge detection, this function is monitored by one of the input pins of the chip's internal ADC (Pin L2 BAT_DET), where the maximum input voltage allowed is 3.0V. Consequently to use this pin to check the battery power, bettery voltage must be dropped by an external potential divider. The recommended input voltage is 1/2 of the battery voltage and the impedance of the potential divider should be high to minimize the current drawn. SCT2400 detects the battery level based on the voltage detected by this pin, and outputs a tone when the battery is low. The low voltage threshold can be modified using the SCT2400 CPS programming software.

- SCT2400 has the capability to output some simple beep sounds, for example, when power is on and a key is pressed. The function is realized as a PWM output from the chip (Pin K1 BEEP_OUT), so the user needs to add external RC filtering (for details refer to the Schematic Diagram in Chapter 11). Users can enable or disable this function through the upper control software of SCT2400. However, it should be noted that the sound volume of the BEEP_OUT is not controllable. The Reference Schematic Diagram given in Chapter 11 sends the sound signal output from the SCT2400 to the codec and outputs it, so that the sound volume can be controlled. When using this method to control the volume, the volume setting is also set by using the upper control software of SCT2400.

VOX detection, battery power and prompt sound output interface pins are as follows:

Pin	Pin Name	I/O	Function
L1	VOX_DET	AI	VOX detection input pin

L2	BAT_DET	AI	Battery power detection input pin
K1	BEEP_OUT	O	Beep sound ouput

Table 8-8   Other Interfaces Pin Configuration

9. Battery Management

This section describes the power management features of the SCT2400.

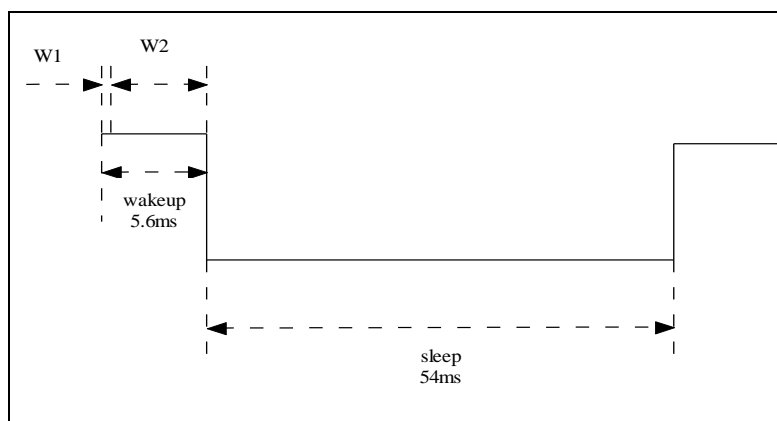SCT2400 goes into the sleep/wake-up cycle in standby state, as described in the following figure.

Figure 9-1   Sleep Wake Control

Work Mode	Time	Description
Wake Mode 1（W1）	0.6 ms	Baseband core active, RF transceiver sleep，codec sleep
Wake Mode 2（W2）	5 ms	Baseband core sleeps, RF transceiver active，codec sleep
Sleep Mode（Sleep）	54 ms	Baseband core sleep, RF transceiver sleep，codec sleep
Normal Mode(Idle)	-	Baseband core active, RF transceiver active，codec sleep
Rx Active Mode (RX)	-	Baseband core active, RF transceiver active，codec active, Receiving audio control is on, Receiving LED light control is on

Tx Active Mode(TX)	-	Baseband core active, RF transceiver active，codec active，transimssion RF power control is on, transmission LED light control is on.

Table 9-1　SCT2400 Operating Modes

As shown in Table 9-1, the SCT2400 has 6 operating modes. When the SCT2400 is in the standby state, it gets into the wake control cycle, shown in Figure 9-1:

When the SCT2400 is in wake mode 1, the RF transceiver and external audio codec are in a sleep mode, the baseband is active and the RF transceiver is controlled to enter the signal detection mode, and then the baseband goes to sleep. If no active signal is detected during wake-up mode 2 then SCT2400 goes into sleep mode. If an active signal is detected, the SCT 2400 switches to the normal mode, and the baseband core enters the baseband demodulation process.

After the baseband core receives demodulation and receives an address match through the DFR protocol stack, SCT2400 enters the RX mode.

When the transmission condition is triggered (PTT button or control command interface), SCT2400 enters the TX mode.

10. Specification

10.1. Recommended Operating Conditions

Table 10-1 lists the recommended operating conditions for the SCT2400:

Parameter	Symbol	Min	Typ	Max	Unit
Digital Power Voltage	VDDD	1.8	3.3	3.6	V
Analog Power Voltage	VDDA (1)	1.8	3.3	3.6	V
Backup Operation Voltage	VBAT (2)	1.8	3.3	3.6	V
RF Power Voltage	VDD_RF	1.8	3.3	3.6	V
RF Crystal Oscillator Frequency	Fosc	-	52	-	MHz
BB Crystal Oscillator Frequency	OSC (3)	-	12	-	MHz

Table 10-1   SCT2400 Recommended Operating Conditions

Instructions:

(1) The voltage difference between VDDA and VDDD must not exceed 300mV. It is recommended that VDDA and VDDD be powered by the same power supply with ferrite beads for isolation.

(2) VBAT power supply is recommended to be connected to VDDD.

(3) The baseband external clock crystal is optional. The internal RC oscillator of the SCT2400 can provide the system clock with an accuracy of ±1% at room temperature. For applications where the clock accuracy is more stringent, an external crystal is recommended as the system clock.

10.2. Power Consumption

The SCT2400 has built-in baseband core and RF transceiver modules. The following describes the power consumption of the two.

Table 10-2 shows the characteristics of the baseband core power consumption:

Work Mode	Frequency (MHz)	Voltage	Current consumption (Typical)
Active	96	3.3 V	40 mA

Standby	-	3.3 V	7 mA

Table 10-2   Baseband Core Power Consumption

Table 10-3 shows the characteristics of the RF transceiver power consumption:

Work Mode		Voltage	Current Consumption （Typical）	Test Conditions
Active	TX	3.3V	24 mA	Pout = 0 dBm
	RX	3.3V	12.5 mA	-
Standby	Idle	3.3V	2 mA	-

Table 10-3   RF Transceiver Power Consumption

10.3. ESD

Table 10-4 lists the ESD ratings of the SCT2400.

CDM	HBM
500V	1000V

Table 10-4   ESD Ratings
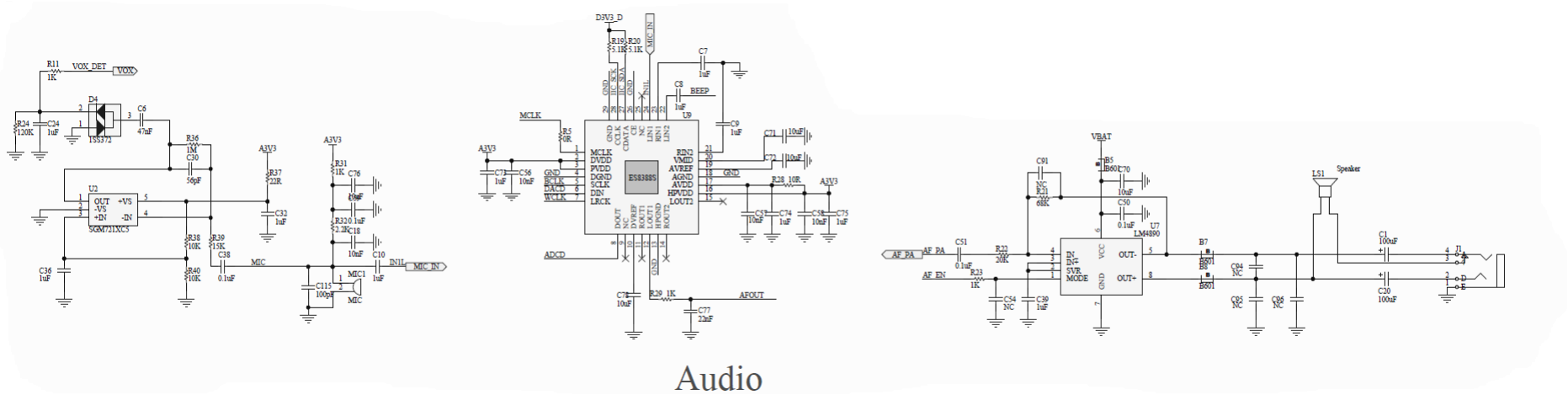
10.4. Parameter Performance

All acceptance tests have a 1% PER as a lower limit. Unless otherwise specified, all interference signals used for dual signal detection are continuous wave (CW) signals.

Symbol	Description	Min	Typ	Max	Unit
IIP3	3rd Order input intercept for max gain setting				
	In-band interferer <6 MHz	-	-25	-	dBm
	In-band interferer @ 6 MHz	-	-6	-	dBm

	In-band interferer @10 MHz	-	-4	-	dBm
	In-band interferer @ 20 MHz	-	-4	-	dBm
IMR	Image rejection	-	30	-	dB
CCR	Co-channel rejection	-	15	-	dB
BI	Blocking immunity				
	+/- 1 MHz	-	60	-	dB
	+/- 2 MHz	-	63	-	dB
	+/- 10 MHz	-	81	-	dB
ACR	Adjacent channel rejection at 1.5 BW	-	37	-	dB
Sensitivity		-	-119	-	dBm
RFOPMIN	Minimum RF output power	-	-18	-	dBm
RFOPMAX	Maximum RF output power	-	12	-	dBm

Table 10.5   Parameter Performance

11. Reference Schematic Diagram

SCT2400 enables a complete 2.4GHz digital walkie-talkie to be designed together with some simple peripheral devices. The following shows a complete reference schematic diagram of 2.4GHz digital radio. Users can quickly start their own design by referring to this diagram.

SCT2400

Audio

Peripheral Device

Power supply

Optional

2.4 GHz FEM
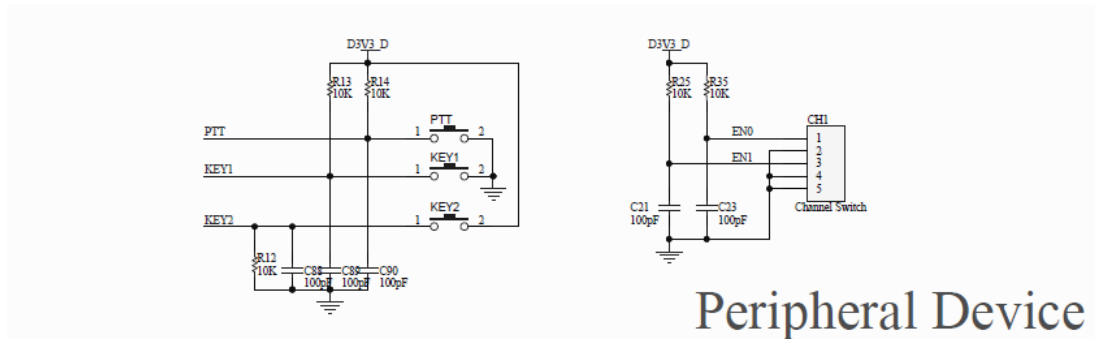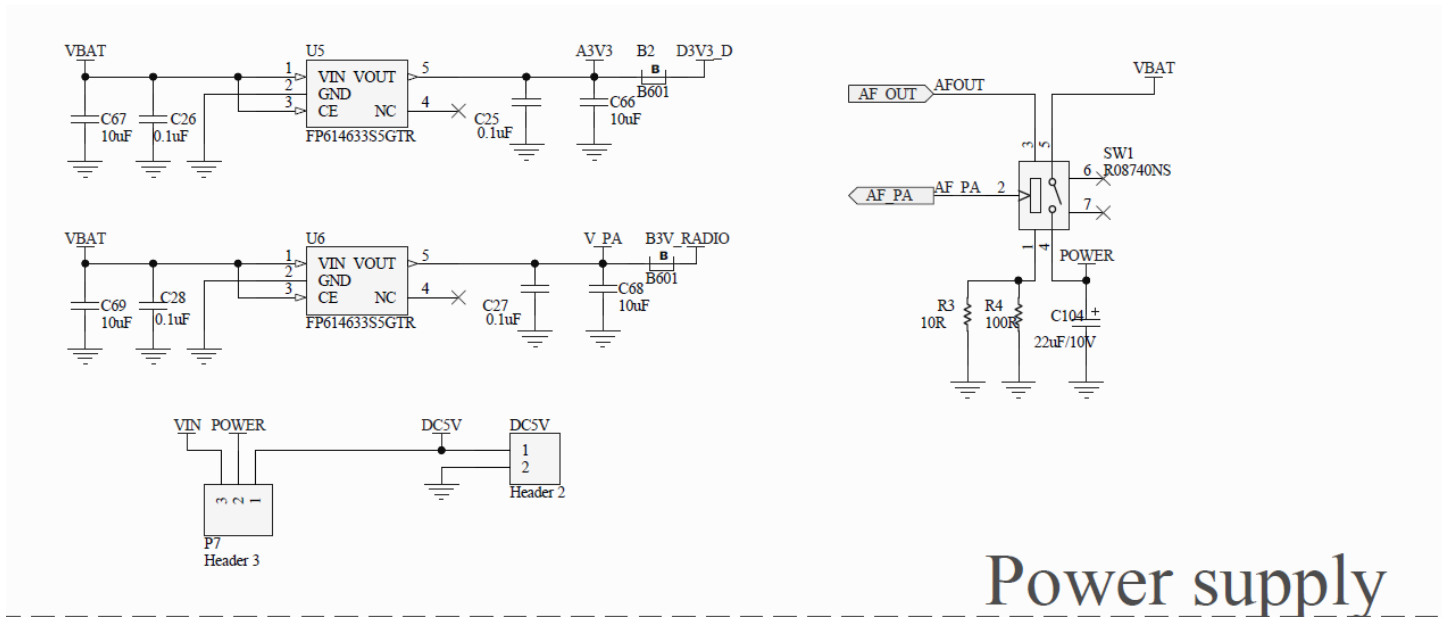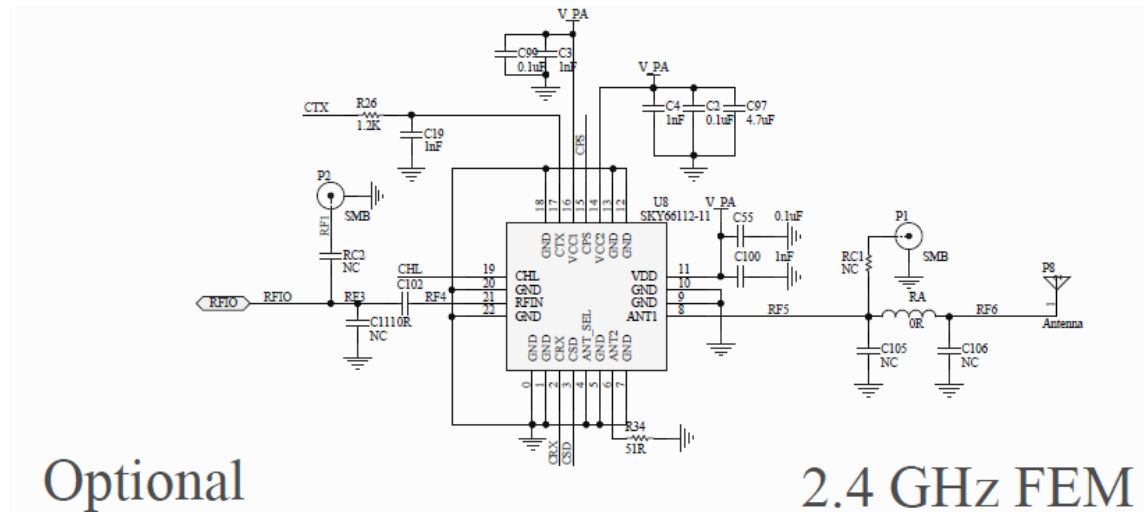
12. Text messaging support

In addition to its voice capabilities the SCT2400 is also capable of providing text communications. This requires the addition of a low cost external microcontroller to handle keypad scanning and display driving. The text message function is accessed using an extended AT command +SENDSMS. Details of the command are contained in the document: *"SCT2400 Packet Interface".* The maximum message length is 300 ASCII characters.
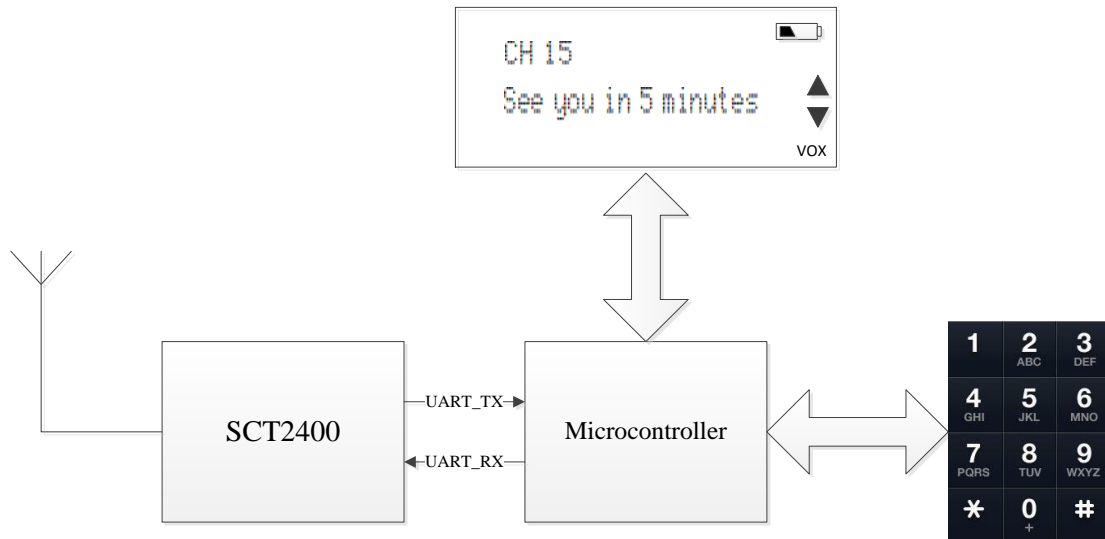
Figure 12.1   Text Message Support Configuration

13. Package Information
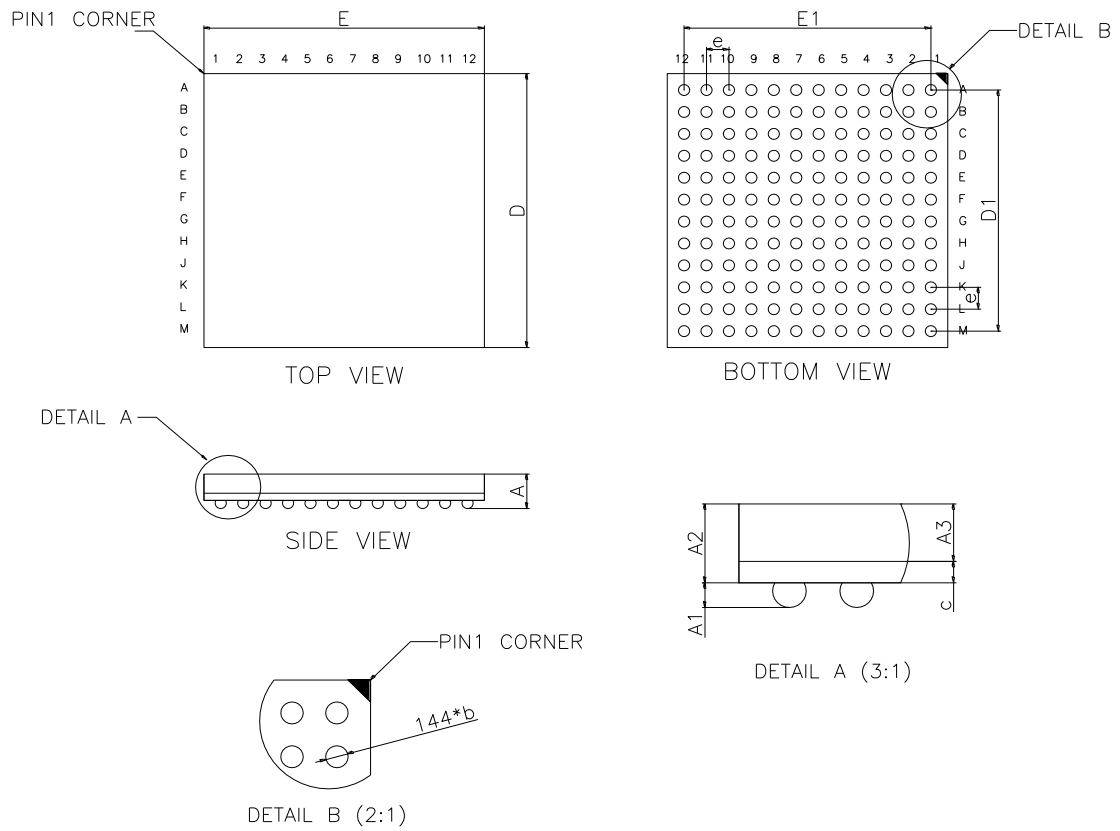
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	−−	−−	1.33
A1	0.25	0.30	0.35
A2	0.91	0.96	1.01
A3	0.7 BASIC		
c	0.22	0.26	0.30
D	9.90	10.00	10.10
D1	8.8 BASIC		
E	9.90	10.00	10.10
E1	8.8 BASIC		
e	0.8 BASIC		
b	0.35	0.40	0.45

Figure 13-1   SCT2400 BGA144 packaging

14. Ordering Information

Part number – SCT2400HDA

1st suffix

Code	Comment
H	Half Duplex operation

2nd suffix

Code	Comment
D	Vocoder option – proprietary vocoder types 1 and 2

3rd suffix

Code	Comment
A	ES8388S codec support

Appendix A

The radio protocol name is DFR and the designation details for DFR is as below:

1. simplex protocol (ISF) structure is as below:
   Frame structure (39Bytes, 80ms): CCH (3Bytes) + VCH (36bytes)

2. CCH (24bits) structure of voice CALL in ISF mode:
   1) Sync type : 1bit (0: voice sync, 1:data sync)
   2) Addressing mode : 1bit (0: ISF,1:CSF)
   3) VSS (voice call start/stop) : 1bit (0:voice frame continue, 1:voice frame end)
   4) Call format : 1bit (0: peer to peer, 1: group call)
      Note: if the target id is 0xff--> indicates ALL call. Call format should be set to 1 in ALL call mode.
   5) Voice_type:1bit (0: normal, 1: emergency)
   6) Vocoder_type:1bit
   7) Reserved : 2bits
   8) Target address : 8bits
   9) Source address : 8bits

CCH (3Bytes)	Byte[0][Bit0]:Sync type (0：voice sync，1：data sync)
	Byte[0][Bit1]:Addressing mode (0: ISF,1:CSF）
	Byte[0][Bit2]:VSS (0:voice frame continue, 1:voice frame end)
	Byte[0][Bit3]:Call format (0:peer to peer, 1:group call)
	Byte[0][Bit4]:Voice_type(0:normal,1:emergency)
	Byte[0][Bit5]:Vocoder_type
	Byte[0][Bit6-7]:Reserved
	Byte[1]:Target address
	Byte[2]:Source address
VCH(36Bytes)	Vocoder encode data(80ms voice data)