ACPL-352J and ACFJ-3520

5.0 Amp Output Current IGBT and SiC MOSFET Gate Drive Optocoupler with Integrated Over Current Sensing, Fault, Gate and UVLO Status Feedback

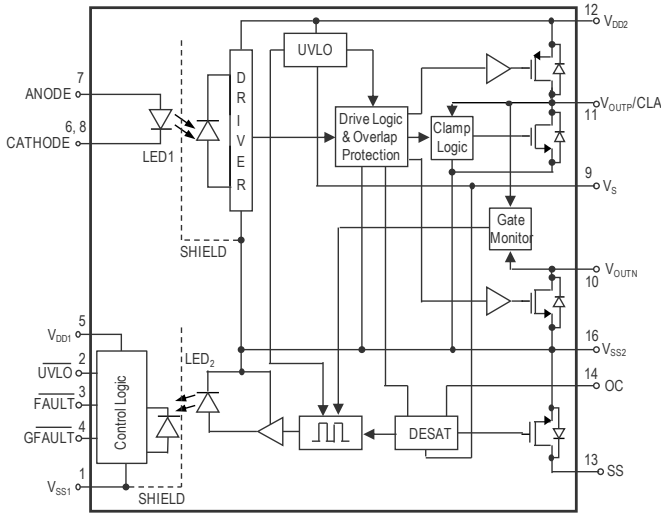
Data Sheet

Description

The ACPL-352J and ACFJ-3520 are advanced 5.0 A output current, easy-to-use, intelligent IGBT and SiC MOSFET gate drive optocoupler.. The high operating voltage range and peak output current of the output stage makes it ideally suited for driving IGBT or SiC MOSFET directly in motor control and inverter applications

The ACPL-352J/ACFJ-3520 contains AlGaAs LED. The LED is optically coupled to an integrated circuit with two power output stages (V_{OUTP} and V_{OUTN}) with non-overlapping timing to control the turning on and off timing separately. It is also integrated with features such as over current detection, under voltage lockout (UVLO), "soft" turn-off, and isolated fault feedback to provide maximum design flexibility and circuit protection. The ACPL-352J/ACFJ-3520 has an insulation voltage of V_{IORM} = 1414 V_{peak}.

ACPL-352J Functional Diagram



Features

- 5.0 A maximum peak output current
- 4.5 A minimum peak output current
- Dual output drive to control turning on and off time
- Over current detection
- Open drain isolated FAULT, GATE and UVLO status feedback
- Configurable "Soft" shutdown during fault
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- 150 ns maximum propagation delay over temperature range.
- 50 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- Wide Operating V_{DD2} Range: 15 to 30 Volts
- Industrial temperature range: -40°C to 105°C
- Package, Creepage and Clearance
  - ACPL-352J SO16 8.3mm
  - ACFJ-3520 SO20 10mm
- Safety Approval Pending
  - UL Recognized 5000 V_{RMS} for 1min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1414 Vpeak

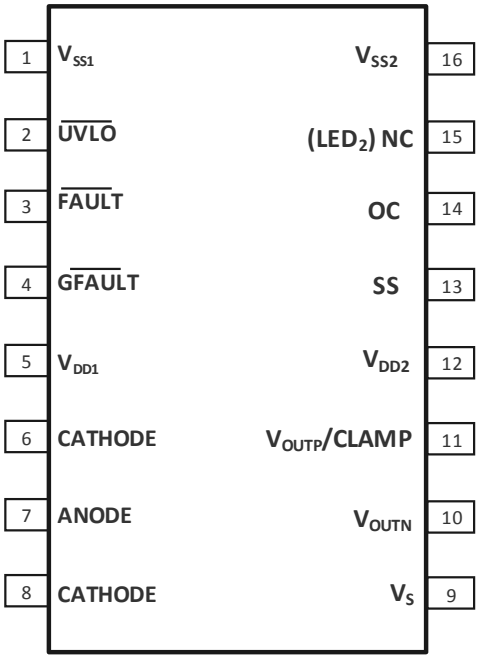
Applications

- IGBT/SiC MOSFET gate drive
- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial Inverters
- Switching power supplies

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments

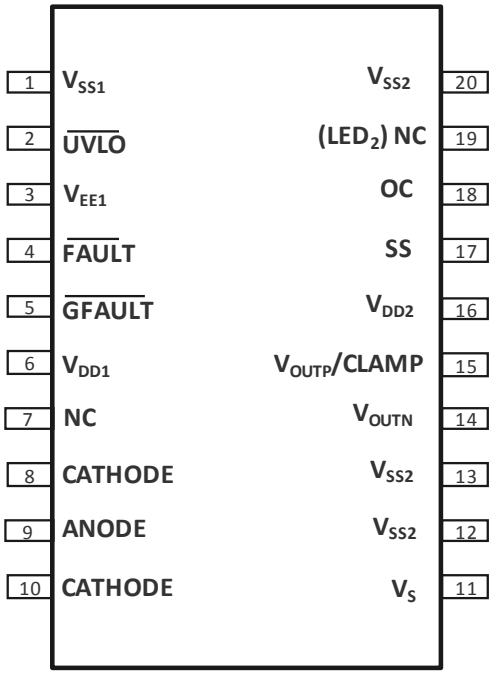
Pin Description

ACPL-352J



Pin	Symbol	Description
1	V_{SS1}	Input ground
2	UVLO	V_{DD2} under voltage lock out feedback
3	FAULT	Over current fault feedback
4	GFAULT	IGBT or MOSFET Gate status feedback
5	V_{DD1}	Input power supply
6	CATHODE	Input LED cathode
7	ANODE	Input LED anode
8	CATHODE	Input LED Cathode
9	V_S	Common (IGBT emitter or MOSFET source) output supply voltage.
10	V_{OUTN}	Driver output to turn off IGBT or MOSFET Gate
11	V_{OUTP}/CLAMP	Driver output to turn on IGBT or MOSFET Gate / Miller Clamp
12	V_{DD2}	Positive output power supply
13	SS	Soft shutdown
14	OC	Over current input pin. When the voltage on OC pin exceeds an internal reference voltage of 7 V while the IGBT is on, FAULT output is changed from logic high to low state.
15	(LED_2)NC	No connection
16	V_{SS2}	Negative output power supply

ACFJ-3520



Pin	Symbol	Description
1	V_{SS1}	Input ground
2	UVLO	V_{DD2} under voltage lock out feedback
3	V_{SS1}	Input ground
4	FAULT	Over current fault feedback
5	GFAULT	IGBT or MOSFET Gate status feedback
6	V_{DD1}	Input power supply
7	NC	No connection
8	CATHODE	Input LED cathode
9	ANODE	Input LED anode
10	CATHODE	Input LED cathode
11	V_S	Common (IGBT emitter or MOSFET source) output supply voltage.
12	V_{SS2}	Negative output power supply
13	V_{SS2}	Negative output power supply
14	V_{OUTN}	Driver output to turn off IGBT or MOSFET Gate
15	V_{OUTP}/CLAMP	Driver output to turn on IGBT or MOSFET Gate / Miller Clamp
16	V_{DD2}	Positive output power supply
17	SS	Soft shutdown
18	OC	Over current input pin. When the voltage on OC pin exceeds an internal reference voltage of 7 V while the IGBT is on, FAULT output is changed from logic high to low state.
19	(LED_2)NC	No connection
20	V_{SS2}	Secondary ground

Ordering Information

ACPL-352J/ACFJ-3520 is UL Recognized with 5000 Vrms for 1 minute per UL1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-352J	-000E	SO-16	X		X	45 per tube
	-500E		X	X	X	850 per reel
ACFJ-3520	-000E	SO-20	X		X	45 per tube
	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

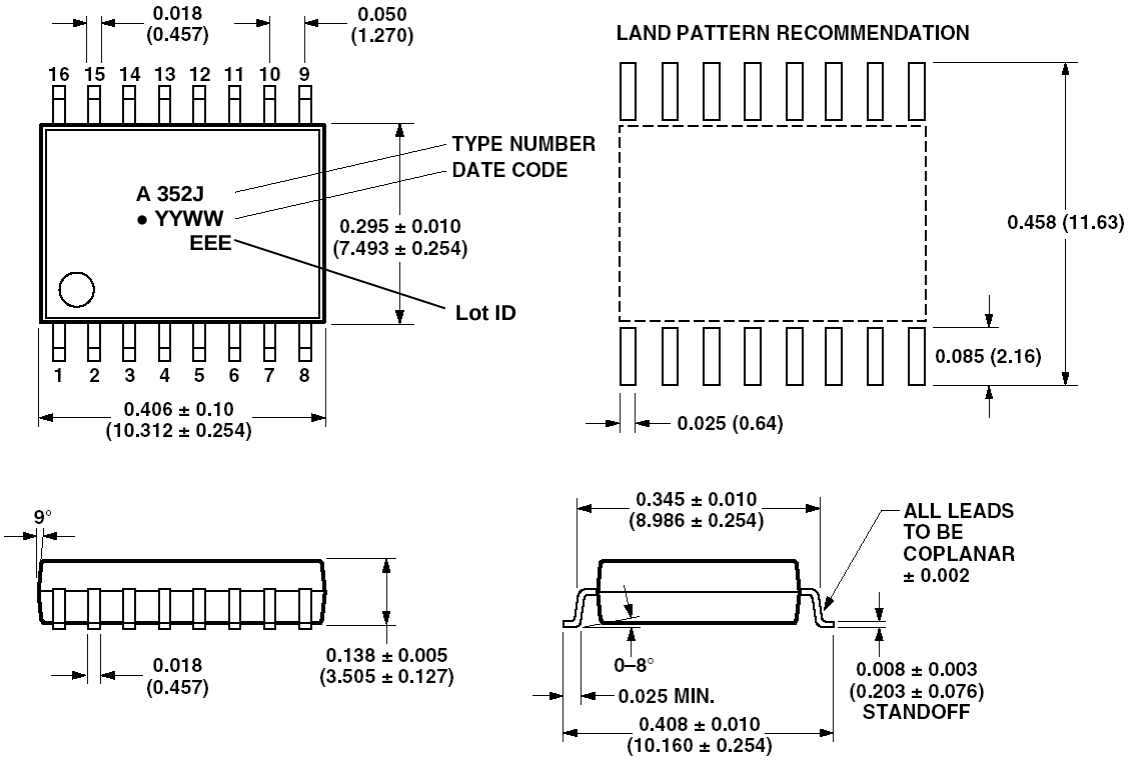
Example 1:

ACPL-352J-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

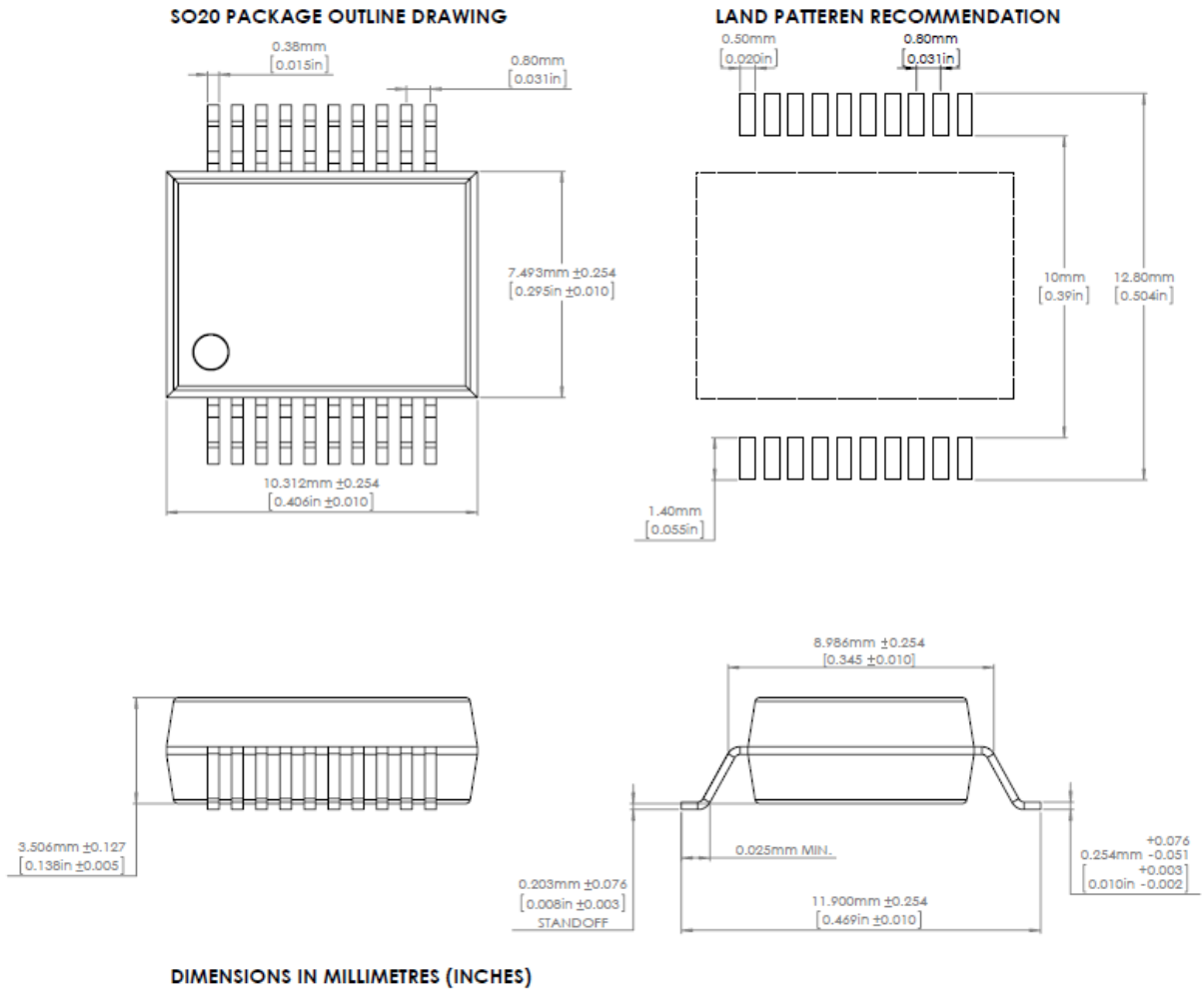
ACPL-352J 16-Lead Surface Mount Package



Dimensions in inches (millimeters)

Floating Lead Protrusion is 0.25 mm (10 mils) max.

ACFJ-3520 20-Lead Surface Mount Package



Notes: Initial and continued variation in the color of the ACPL-352J/ACFJ-3520's white mold compound is normal and does not affect device performance or reliability.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-352J/ACFJ-3520 is pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-5
Maximum working insulation voltage V_{IORM} = 1414V_{PEAK}

UL
Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}. File E55361.

CSA
Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – IV	
for rated mains voltage ≤ 1000 V_{rms}		I – III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b** V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a** V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	400	mA
Output Power	$P_{S, OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.
** Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Avago Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-352J	ACFJ-3520	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	10	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	10	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Notes: All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J		125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		5	A	2
Positive Input Supply Voltage	V_{DD1}	0	7	V	
FAULT Output Current	I_{FAULT}		8	mA	
FAULT Pin Voltage	V_{FAULT}	-0.5	V_{DD1}	V	
Total Output Supply Voltage	$(V_{DD2} - V_{SS2})$	-0.5	35	V	
Negative Output Supply Voltage	$(V_S – V_{SS2})$	-0.5	17	V	
Positive Output Supply Voltage	$(V_{DD2} – V_S)$	-0.5	$35 - (V_S - V_{SS2})$	V	
Input Current (Rise/Fall Time)	$t_{r(IN)}/t_{f(IN)}$		500	ns	
High Side Pull Up Voltage	V_{OUTP}	V_{SS2} - 0.5	V_{DD2} + 0.5	V	
Low Side Pull Down Voltage	V_{OUTN}	V_{SS2} - 0.5	V_{DD2} + 0.5	V	
Over Current Pin Voltage	V_{OC}	V_S - 0.5	V_{DD2} + 0.5	V	
Output IC Power Dissipation	P_O		600	mW	3
Input LED Power Dissipation	P_I		110	mW	4

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/ °C.
2. Maximum pulse width = 10µs.The output must be limited to -5.0 A / 5.0 A of peak current by external resistors and connected to total load bigger than 2nF during all applications or board testing.
3. Derate linearly above 95°C free-air temperature at a rate of 20 mW/ °C.
4. Derate linearly above 95°C free-air temperature at a rate of 3.7 mW/ °C. The maximum LED junction temperature should not exceed 125°C.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	- 40	105	°C	
Positive input supply voltage	V_{DD1}	4.5	5.5	V	
Total Output Supply Voltage	(V_{DD2} - V_{SS2})	15	30	V	
Negative Output Supply Voltage	(V_S – V_{SS2})	0	15	V	
Positive Output Supply Voltage	(V_{DD2} - V_S)	15	30 - (V_S - V_{SS2})	V	
Input Current (ON)	$I_{F(ON)}$	6	10	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	

Table 5. Electrical Specifications (DC)

All typical values at T_A = 25°C, V_{DD1} = 5V, V_{DD2} – V_S = 15 V, V_S - V_{SS2} = 15 V; All minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
V_{OUTP} High Level Peak Output Current	I_{OH}	-4.5	TBD		A	V_{DD2} - V_{OUTP} =15V		1
V_{OUTN} Low Level Peak Output Current	I_{OH}	4.5	TBD		A	V_{OUTN} – V_{SS2} = 15V		1
V_{OUTP} Output PMOS $R_{DS(ON)}$	R_{OUTP}	TBD	0.7	1	Ω	I_{OP} = -4.5 A, I_F = 8mA,		1
V_{OUTN} Output NMOS $R_{DS(ON)}$	R_{OUTN}	TBD	0.6	1	Ω	I_{ON} = 4.5 A, V_F = 0V ,		1
V_{OUTP} Output Voltage	V_{OH}	V_{DD2} - 0.60	V_{DD2} - 0.06		V	I_{OP} = -100mA, I_F = 8mA		2, 3
V_{OUTN} Output Voltage	V_{OL}		V_{SS2} + 0.04	V_{SS2} + 0.60	V	I_{ON} = 100mA, V_F = 0V		
Clamp Threshold Voltage	V_{TH_CLAMP}		2	3	V			
Clamp Low Level Sinking Current	I_{CLAMP}	2	2.9		A	V_{CLAMP}=V_{SS2}+2.5V		
Clamp Output Transistor $R_{DS(ON)}$	$R_{DS,CLAMP}$		0.8		Ω	I_{CLAMP}=2.5A		
SS Pull Down Current	I_{OSS}	100			mA	SS - V_{SS2} ≥ 5V, I_F = 8mA , OC= Open		
SS R_{DSON}	R_{OUTSS}		16	TBD	Ω	I_{SS} = 100mA, I_F =8mA , OC = Open		
High Level Output Supply Current (V_{DD2})	I_{DD2H}		6.1	TBD	mA	I_F= 8 mA, No Load,		
Low Level Output Supply Current (V_{DD2})	I_{DD2L}		5.1	TBD	mA	V_F = 0 V, No Load,		
High Level Output Supply Current (V_{SS2})	I_{SSH}	TBD	-1.75		mA	I_F= 8 mA, No Load,		
Low Level Output Supply Current (V_{SS2})	I_{SSL}	TBD	-0.75		mA	V_F = 0 V, No Load,		
Threshold Input Current Low to High	I_{FLH}		2.3	TBD	mA			
Threshold Input Voltage High to Low	V_{FHL}	TBD			V			
Input Forward Voltage	V_F		1.55		V	I_F = 8 mA		
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.7		mV/°C	I_F = 8 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 100 μA		
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V		

UVLO Threshold, V_{DD2}-V_S	V_{UVLO+}	TBD	12.9	TBD	V	I_F = 8mA, V_{OUTP} - V_E > 5 V		2,3,4
	V_{UVLO-}	TBD	11.9	TBD	V	I_F = 8 mA, V_{OUTP} - V_E < 5 V		2,3,5
UVLO Hysteresis, V_{DD2}-V_S	V_{UVLO+} -V_{UVLO-}		1		V			
OC Sensing Voltage Threshold	V_{OC}	TBD	9	TBD	V	V_{DD2} - V_S > V_{UVLO+}		3
Blanking Capacitor Charging Current	I_{CHG}	0.92	1.1	1.08	mA	V_{OC} = 2 V		3, 6
OC Low Voltage when Blanking Capacitor Discharge	V_{DSCHG}		1.1	3	V	I_{DSCHG} = 50mA		3, 6
Input Supply Current (V_{DD1})	I_{DD1}		1.6	TBD	mA			
FAULT Logic Low Output Current	I_{FAULTL}	4	9.2		mA	V_{FAULT} = 0.4 V V_{DD1} = 5 V		
FAULT Logic High Output Current	I_{FAULTH}			20	µA	V_{FAULT} = V_{DD1} = 5 V		
UVLO Logic Low Output Current	I_{UVLOL}	4	9.2		mA	V_{UVLO} = 0.4 V V_{DD1} = 5 V		
UVLO Logic High Output Current	I_{UVLOH}			20	µA	V_{UVLO} = V_{DD1} = 5 V		
GFAULT Logic Low Output Current	$I_{GFAULTL}$	4	9.2		mA	V_{GFAULT} = 0.4 V V_{DD1} = 5 V		
GFAULT Logic High Output Current	$I_{GFAULTH}$			20	µA	V_{GFAULT}= V_{DD1} = 5 V		

Notes:

1. Output is sourced at -4.5 A /4.5 A with a maximum pulse width = 10 µs.
2. 15 V is the recommended minimum operating positive supply voltage (V_{DD2} - V_S) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of TBD V. For High Level Output Voltage testing, V_{OUTP} is measured with a 50us pulse load current. When driving capacitive loads, V_{OUTP} will approach V_{DD2} as I_{OUTP} approaches zero units.
3. Once the system is out of UVLO (V_{DD2} – V_S > V_{UVLO+}), the OC detection feature of the ACPL-352J/ACFJ-3520 will be the primary source of IGBT protection. UVLO needs to be unlocked to ensure DESAT is functional. Once V_{DD2} exceeds V_{UVLO+} threshold, DESAT will remain functional until V_{DD2} is below V_{UVLO-} threshold. The OC detection and UVLO features of the ACPL-352J/ACFJ-3520 work in conjunction to ensure constant IGBT / MOSFET protection.
4. This is the “increasing” (i.e. turn-on or “positive going” direction) of V_{DD2} – V_S.
5. This is the “decreasing” (i.e. turn-off or “negative going” direction) of V_{DD2} – V_S.
6. See the over current fault detection blanking time section in the applications notes at the end of this data sheet for further details.

Table 6. Switching Specifications (AC)

All typical values at T_A = 25°C, V_{DD1} = 5V, V_{DD2} – V_S = 15 V, V_S - V_{SS2} = 15 V; All minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High V_{OUTP} Output Level	t_{PLH}	TBD	100	150	ns	R_{GP} = 5Ω, R_{GN} = 5Ω, C_G = 5nF, f = 20 kHz, Duty Cycle = 50%, I_F = 6 mA to 10 mA.	2	1
Propagation Delay Time to Low V_{OUTN} Output Level	t_{PHL}	TBD	90	150	ns			2
Pulse Width Distortion	PWD	-75	10	75	ns			3
Propagation Delay Difference Between Any Two Parts	PDD (t_{PLH} - t_{PHL})	-75		75	ns			4
Propagation Delay Skew	t_{PSK}			60	ns			5
10% to 90% Rise Time on V_{OUTP}	t_R		37		ns	R_{GP} = 5Ω, R_{GN} = 5Ω, C_G = 2nF, f = 20 kHz, Duty Cycle = 50%, I_F = 8mA.	2	
90% to 10% Fall Time on V_{OUTN}	t_F		30		ns			
OC Blanking Time	$t_{OC(BLANKING)}$		0.78	TBD	us	R_{GP} = 5Ω, R_{GN} = 5Ω, C_G = 5 nF, f = 100 Hz, Duty Cycle = 50%, I_F = 8 mA, R_{SS}=133Ω, C_F = 330 pF, R_F = 10 kΩ,	5	6
OC Detection to 90% V_{GATE} Delay	$t_{OC(90\%)}$		0.28		us		5	7
OC Detection to V_{GATE}=2V Delay	$t_{OC(2V)}$		2.5		us		5	8
OC Detection to OC Pull Low Propagation Delay	$t_{OC(LOW)}$		0.25		us		5	9
OC Detection to SS Pull Low Propagation Delay	$t_{SS(LOW)}$		0.2	TBD	us		5	10
OC Detection to Low Level FAULT Signal Delay	$t_{OC(FAULT)}$		1.7	3	us		5	11
Output Mute Time due to Over Current	$t_{OC(MUTE)}$	TBD	3	TBD	ms		5	12
Time Input Kept Low Before Fault Reset to High	$t_{OC(RESET)}$	TBD	3	TBD	ms	C_F = 330 pF, R_F = 10 kΩ	5	13
V_{DD2} to UVLO High Delay	t_{PLH_UVLO}		13.5	TBD	us	C_U = 330 pF, R_U = 10 kΩ	4	14
V_{DD2} to UVLO Low Delay	t_{PHL_UVLO}		13.5	TBD	us	C_U = 330 pF, R_U = 10 kΩ	4	15
V_{DD2} UVLO to V_{OUTP} High Delay	t_{UVLO_ON}		4		us		4	16
V_{DD2} UVLO to V_{OUTN} Low Delay	t_{UVLO_OFF}		1.5		us		4	17
Delay Time to V_{GATE} Status Check	t_{GFAULT}	7.5	9.5	13	us		6	18
V_{GATE} Status Check to Low Level GFAULT Signal Delay	$t_{GFAULT(10\%)}$		13.5	TBD	us	C_{GF} =330 pF, R_{GF} = 10 kΩ	6	19
Input Logic Change to High Level GFAULT Signal Delay	$t_{GFAULT(90\%)}$		10	TBD	us	C_{GF} = 330 pF, R_{GF} = 10 kΩ	6	20
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	50			kV/µs	T_A = 25°C, V_{CM} = 2000 V, V_{DD1} = 5 V, C_F = 330 pF, R_F = 10 kΩ, I_F = 8 mA		21, 23
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	50			kV/µs	T_A = 25°C, V_{CM} = 2000 V, V_{DD1} = 5 V, C_F = 330		22,23

						pF, R_F = 10 kΩ, V_F = 0 V		

Notes:

1. t_{PLH} is defined as propagation delay from 50% of LED input I_F, to 50% of V_{OUTP} high level output.
2. t_{PHL} is defined as propagation delay from 50% of LED input I_F, to 50% of V_{OUTN} low level output.
3. Pulse Width Distortion (PWD) is defined as |tPHL - tPLH| for any given unit.
4. Propagation Delay Difference (PDD) is the difference between t_{PHL} and t_{PLH} between any two units under the same test condition.
5. Propagation Delay Skew (t_{PSK}) is the difference in t_{PHL} or t_{PLH} between any two units under the same test condition.
6. The internal delay time to respond to a OC fault condition without any external blanking capacitor.
7. The amount of time from when OC threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.
8. The amount of time from when OC threshold is exceeded to V_{GATE} at 2 V at mentioned test conditions.
9. The amount of time from when OC threshold is exceeded to 10% of OC low voltage.
10. The amount of time from when OC threshold is exceeded to 10% of SS(Soft Shut) low voltage.
11. The amount of time from when OC threshold is exceeded to FAULT output low.
12. The amount of time when OC threshold is exceeded, output is muted to LED input.
13. The amount of time when OC mute time is expired, LED input must be kept low for FAULT status to return to High.
14. The delay time when V_{DD2} exceeds UVLO+ threshold to UVLO high – 50% of UVLO positive-going edge.
15. The delay time when V_{DD2} exceeds UVLO- threshold to UVLO low – 50% of UVLO negative-going edge.
16. The delay time when V_{DD2} exceeds UVLO+ threshold to 50% of V_{OUTP} high level output.
17. The delay time when V_{DD2} exceeds UVLO- threshold to 50% of V_{OUTN} low level output.
18. The delay to allow sufficient time for the gate to charge or discharge to its final level before checking gate voltage corresponds to LED input logic.
19. The delay time when gate voltage does not correspond to LED input logic to GFAULT output low.
20. The delay time when GFAULT returns to high after LED input logic change or gate voltage crosses the intended level threshold.
21. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_{DD2} – V_{OUTP}$ < 1.0 V or FAULT > 2V). V_{DD2} must be higher than V_{UVLO+}.
22. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_{OUTN} - V_{SS2}$ < 1.0 V or FAULT > 2 V). V_{DD2} must be higher than V_{UVLO+}.
23. Split resistor network in the ratio 3:1 with 324 Ω at the anode and 107 Ω at the cathode.

Table 7. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{rms}	RH < 50%, t = 1 min., T_A = 25°C		1, 2
Input-Output Resistance	R_{I-O}		> 10^9		Ω	V_{I-O} = 500 V		2
Input-Output Capacitance	C_{I-O}		1.3		pF	freq=1 MHz		

Notes

1. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table, if applicable.
2. Device considered a two-terminal device: For ACPL-352J, pins 1 to 8 are shorted together and pins 9 to 16 are shorted together. For ACFJ-3520, pins 1 to 10 are shorted together and pins 11 to 20 are shorted together.

Applications Information

Product Overview Description

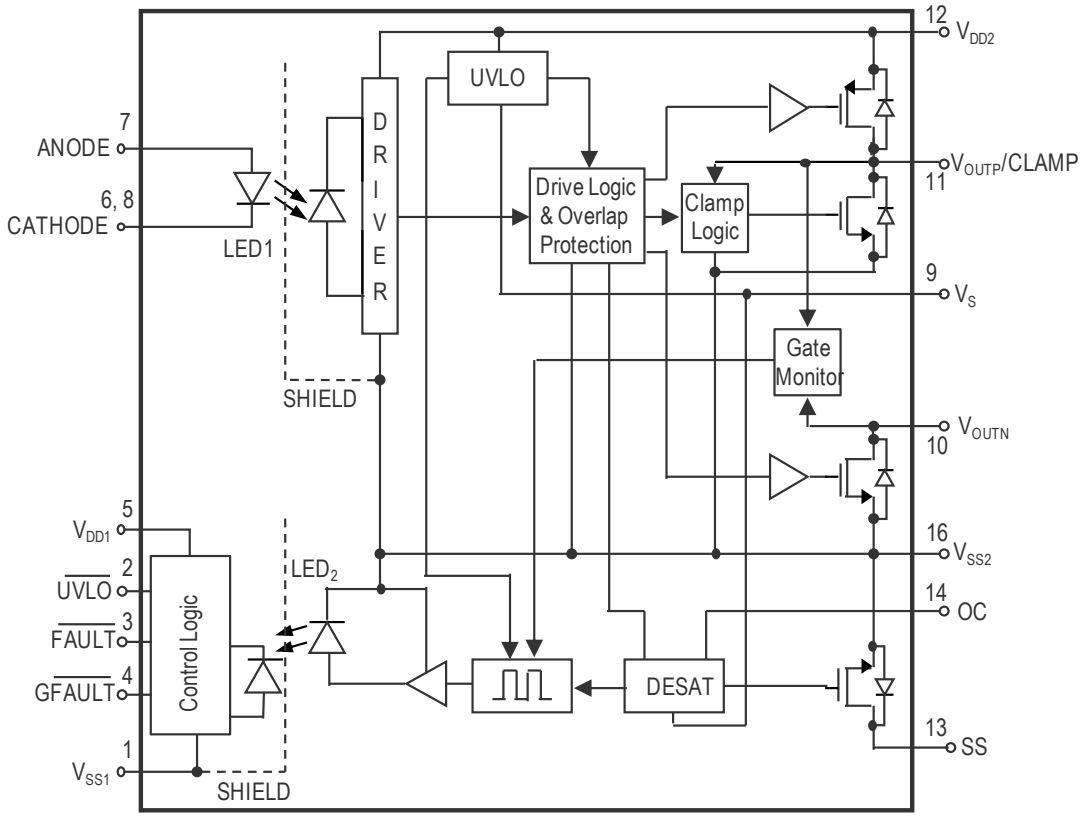


Figure 1.Block Diagram of ACPL-352J

Recommended Application Circuit

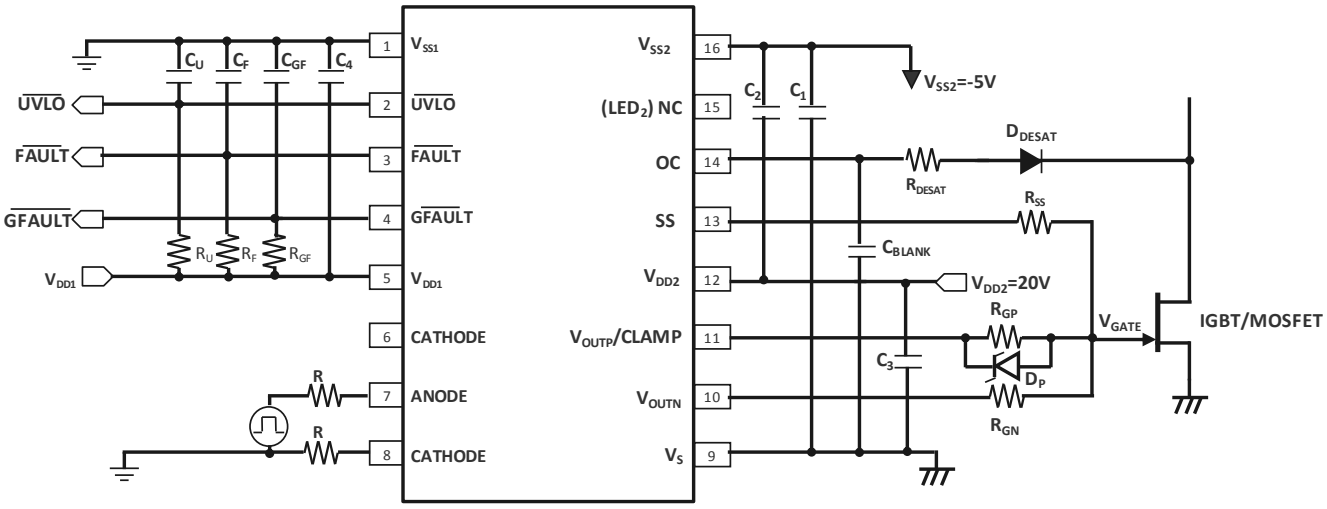


Figure 2.Recommended application circuit with over current detection and fault feedback for ACPL-352J

Output Control

The outputs (V_{OUTP}, V_{OUTN}, FAULT and UVLO) of the ACPL-352J/ACFJ-3520 are controlled by the combination of V_{DD1}, V_{DD2}, LED current I_F and over current condition. The table below shows the logic truth table for these outputs.

Condition	Inputs				Outputs				
	V_{DD1}	V_{DD2}	I_F	OC	V_{OUTN}	V_{OUTP}/CLAMP	SS	FAULT	UVLO
V_{DD1} Under Voltage	Low	High	Low	X	Low	Low	High-Z	Low	Low
	Low	High	High	Low	High-Z	High	High-Z	Low	Low
V_{DD2} UVLO	Low	Low	X	X	Low	Low	High-Z	Low	Low
	High	Low	X	X	Low	Low	High-Z	High	Low
Over Current	Low	High	High	High	High-Z	Low	Low	Low	Low
	High	High	High	High	High-Z	Low	Low	Low	High
Normal Switching	High	High	Low	X	Low	Low	High-Z	High	High
	High	High	High	Low	High-Z	High	High-Z	High	High

The logic level is defined by the respective threshold of each function pin.

Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high the output of ACPL-352J/ACFJ-3520 is capable of delivering 5A sourcing current to drive the IGBT's/MOSFET's gate. While LED is switched off the gate driver can provide 5A sinking current to switch the gate off fast. Additional miller clamping pull-down transistor is activated when output voltage reaches about 2V with respect to V_{SS2} to provide low impedance path to miller current as shown

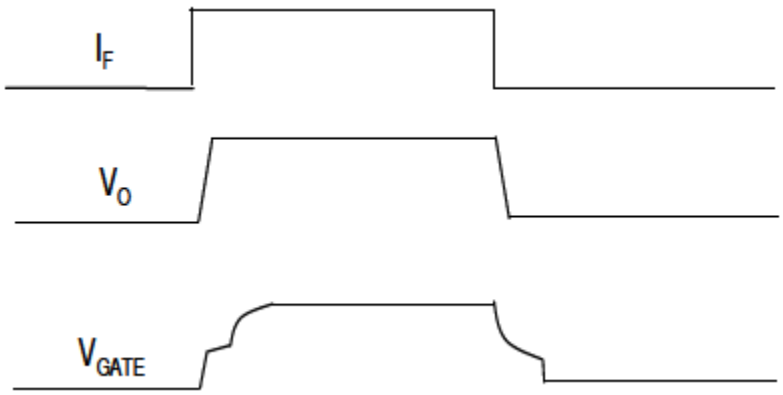


Figure 3.Gate Drive Signal Behavior

Description of Under Voltage Lock Out (Refer to Figure 4)

Insufficient gate voltage to IGBT/MOSFET can increase turn on resistance of IGBT/MOSFET, resulting a large power loss and IGBT/MOSFET damage due to high heat dissipation. ACPL-352J/ACFJ-3520 monitors the output power supply constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect IGBT/MOSFET from low voltage bias. During power up, the UVLO feature forces the gate driver output to low to prevent unwanted turn on at lower supply voltage.

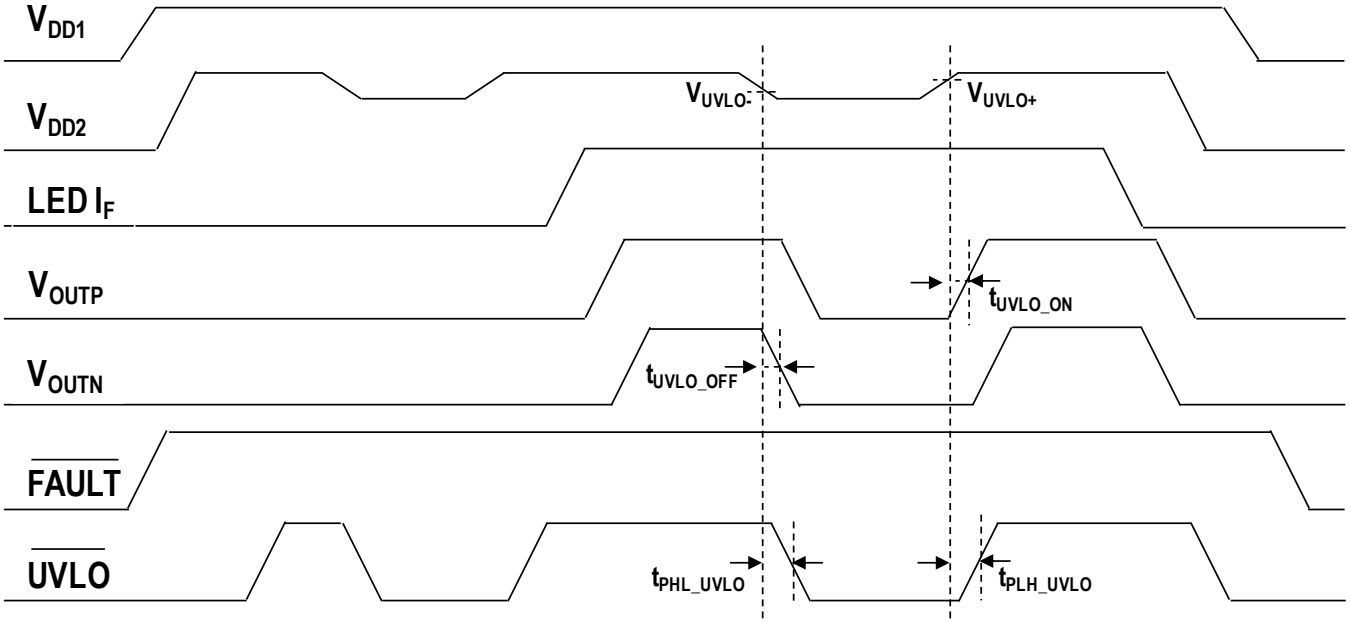


Figure 4.Circuit behaviors at power up and power down

Description of Operation during Over Current Condition (Refer to Figure 5)

1. OC terminal monitors IGBTs V_{CE} or MOSFET V_{DS} voltage.
2. When the voltage on the OC terminal exceeds 9 volts, the output voltages (V_{OUTP} and V_{OUTN}) go to Hi-Z state and the SS pull down the V_{GATE} slowly via resistor R_{SS}.
3. FAULT output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.
5. When $t_{OC(MUTES)}$ expires, LED input need to be kept low for $t_{RESET(SS)}$ before fault condition is cleared. FAULT status will return to high and SS output will return to Hi-Z state.
6. V_{GATE} starts to respond to LED input after fault condition is cleared.

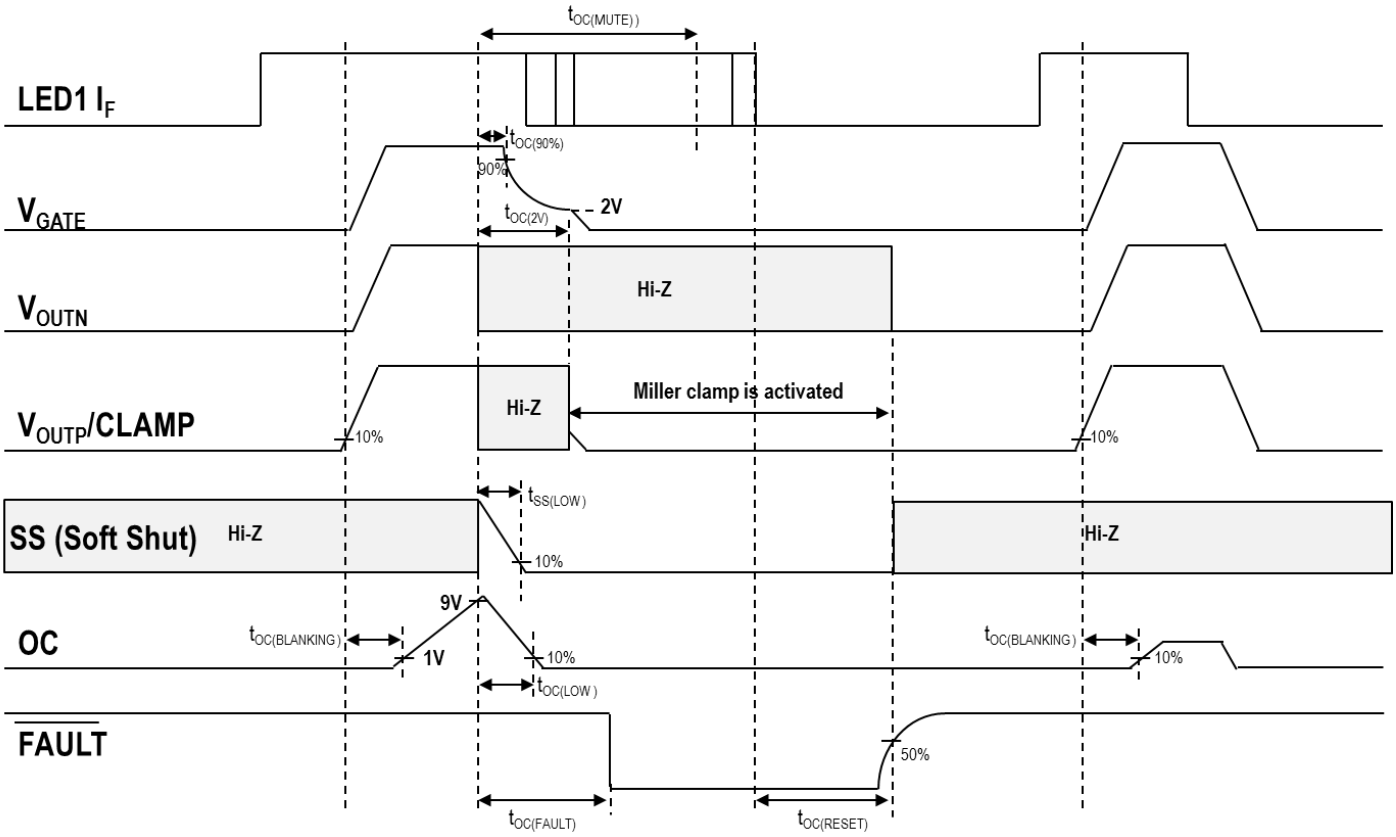


Figure 5.Circuit behaviors during over current event

Description of Gate Status Monitoring (Refer to Figure 6)

The status of the IGBT/MOSFET gate voltage is monitored by output pins V_{OUTP} and V_{OUTN}. The GFAULT output goes low when the gate voltage does not correspond to the LED input logic. The status of the gate is checked after a minimum delay time t_{GFAULT} to allow sufficient time for the gate to charge or discharge to its final level. There will no check for short input pulses to prevent false GFAULT reporting since the gate will not be able to reach its intended level.

When the LED input logic is high, V_{OUTN} will be sensed to check if the gate voltage is higher than V_{DD2}-2V after t_{GFAULT} delay. GFAULT output will go low if gate voltage is lower than V_{DD2}-2V. Likewise, when the LED input logic is low, V_{OUTP} will be sensed to check if the gate voltage is lower than V_{SS2}+2V. GFAULT output will return to high upon input logic change or if the gate voltage manages to cross the threshold of V_{DD2}-2V or V_{SS2}+2V.

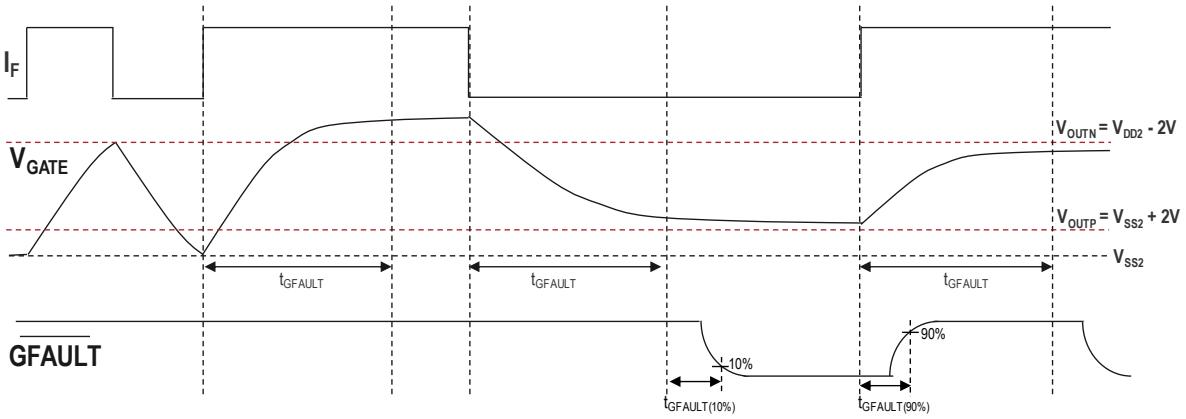


Figure 6.Circuit behaviors during gate status monitoring