



**RoHS compliant**  
**1310 nm multi-mode Transceiver (2 km)**  
**1x9, SC Duplex Connector, 5.0 V**  
**155 Mbps ATM/ Fast Ethernet**



### Features

- RoHS compliant
- Industry standard 1×9 footprint
- SC duplex connector
- Single power supply 5.0 V
- Differential PECL inputs and outputs
- Class 1 laser product complies with EN 60825-1

### Ordering Information

PART NUMBER	INPUT/OUTPUT	SIGNAL DETECT	VOLTAGE	TEMPERATURE
LM32-A5C-PC-N	DC/DC	PECL	5.0 V	0°C to 70°C
LM32-A5C-PI-N	DC/DC	PECL	5.0 V	-40°C to 85°C

### Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	$T_S$	-40	85	°C	
Supply Voltage	$V_{CC}$	-0.5	6.0	V	
Input Voltage	$V_{IN}$	-0.5	$V_{CC}$	V	
Soldering Temperature	$T_{SOLD}$	---	260	°C	10 seconds on leads



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### Operating Environment

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Ambient Operating Temperature	$T_{AMB}$	0 -40	70 85	°C	
Supply Voltage	$V_{CC}$	3.1	3.5	V	

### Transmitter Electro-optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate	$B$	50	155	200	Mb/s	
Output Optical Power 62.5/125 $\mu$ m fiber	$P_{out}$	-20	---	-14	dBm	Average
Output Optical Power 50/125 $\mu$ m fiber		-23.5	---	-14	dBm	Average
Extinction Ratio	$ER$	10	---	---	dB	
Center Wavelength	$\lambda_c$	1260	---	1360	nm	
Spectral Width (FWHM)	$\Delta\lambda$	---	---	20	nm	
Rise/Fall Time (10–90%)	$T_{r,f}$	---	---	3	ns	
Duty Cycle Distortion	$DCD$			0.6	ns	
Data Dependent Jitter	$DDJ$			0.6	ns	
Random Jitter	$RJ$			0.6	ns	
Power Supply Current	$I_{CC}$	---	---	130	mA	Note 1
Transmitter Data Input Voltage-High	$V_{IH} - V_{CC}$	-1.1	---	-0.74	V	
Transmitter Data Input Voltage-Low	$V_{IL} - V_{CC}$	-2.0	---	-1.58	V	

Note 1: Not including the terminations.



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### Receiver Electro-optical Characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate	$B$	50	155	200	Mb/s	
Optical Input Power-maximum	$P_{IN}$	-8	---	---	dBm	Note 1
Optical Input Power-minimum (Sensitivity)	$P_{IN}$	---	---	-31	dBm	Note 1
Operating Center Wavelength	$\lambda_C$	1260	---	1610	nm	
Signal Detect-Asserted	$P_A$	---	---	-31	dBm	Average
Signal Detect-Deasserted	$P_D$	-45	---	---	dBm	Average
Signal Detect-Hysteresis	$P_A - P_D$	0.5	---	---	dB	
Signal Detect Output voltage-High	$V_{OH} - V_{CC}$	-1.1	---	-0.74	V	
Signal Detect Output voltage-Low	$V_{OL} - V_{CC}$	-2.0	---	-1.58	V	
Power Supply Current	$I_{CC}$	---	---	120	mA	Note 2
Data Output Rise, Fall Time (10-90%)	$T_{r,f}$	---	---	3	ns	
Data Output Voltage-High	$V_{OH} - V_{CC}$	-1.1	---	-0.74	V	
Data Output Voltage-Low	$V_{OL} - V_{CC}$	-2.0	---	-1.58	V	

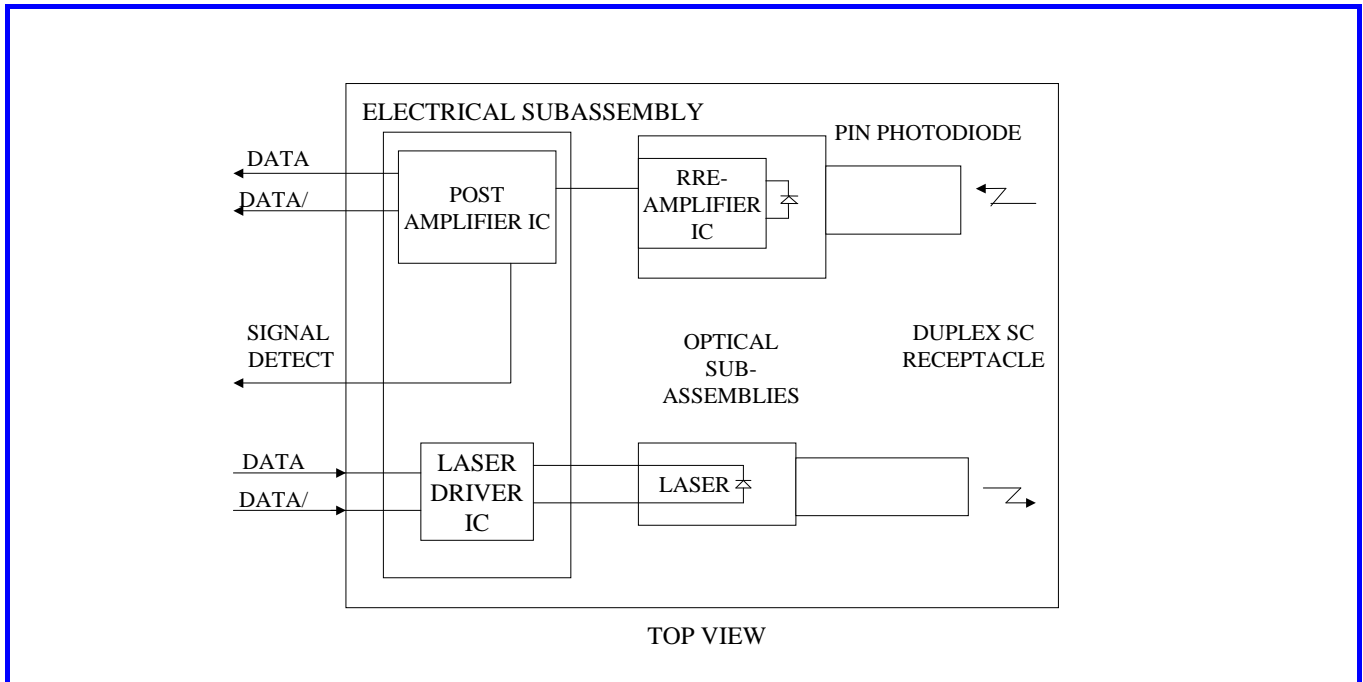
Note 1: The input data is at 155.52 Mbps,  $2^{23}-1$  PRBS data pattern. The receiver is guaranteed to provide output data with Bit Error Rate (BER) better than or equal to  $2.5 \times 10^{-10}$ .

Note 2: The current exclude the output load current.



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### Block Diagram of Transceiver



#### Transmitter Section

The transmitter section consists of a 1310 nm laser in an optical subassembly (OSA) which mates to the fiber cable. The OSA is driven by a driver IC which converts differential input PECL logic signals into an analog driving current.

#### Receiver Section

The receiver utilizes an InGaAs PIN photodiode mounted together with a trans-impedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

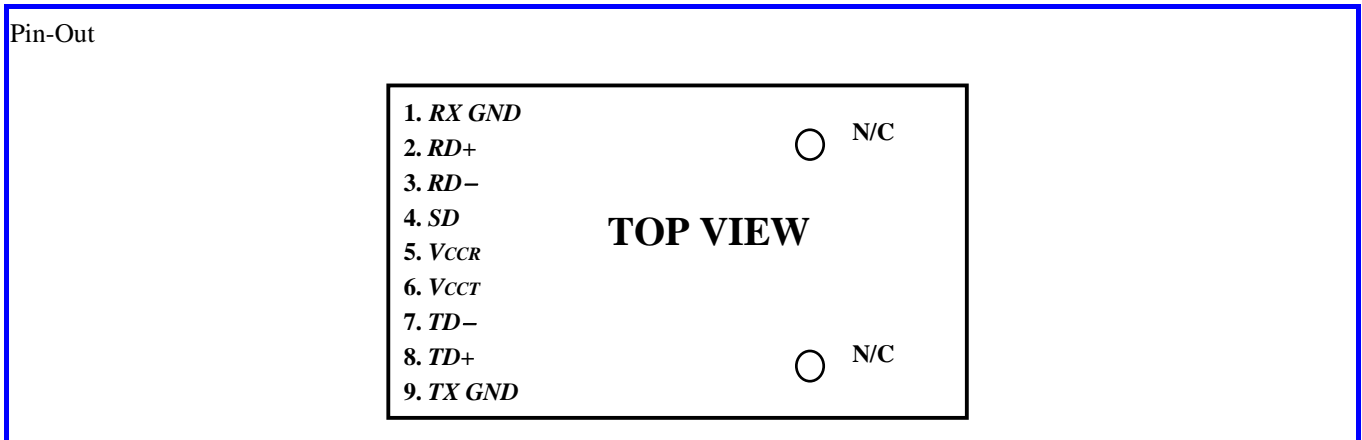
#### Receiver Signal Detect

Signal Detect is a basic fiber failure indicator. This is a single-ended PECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point).



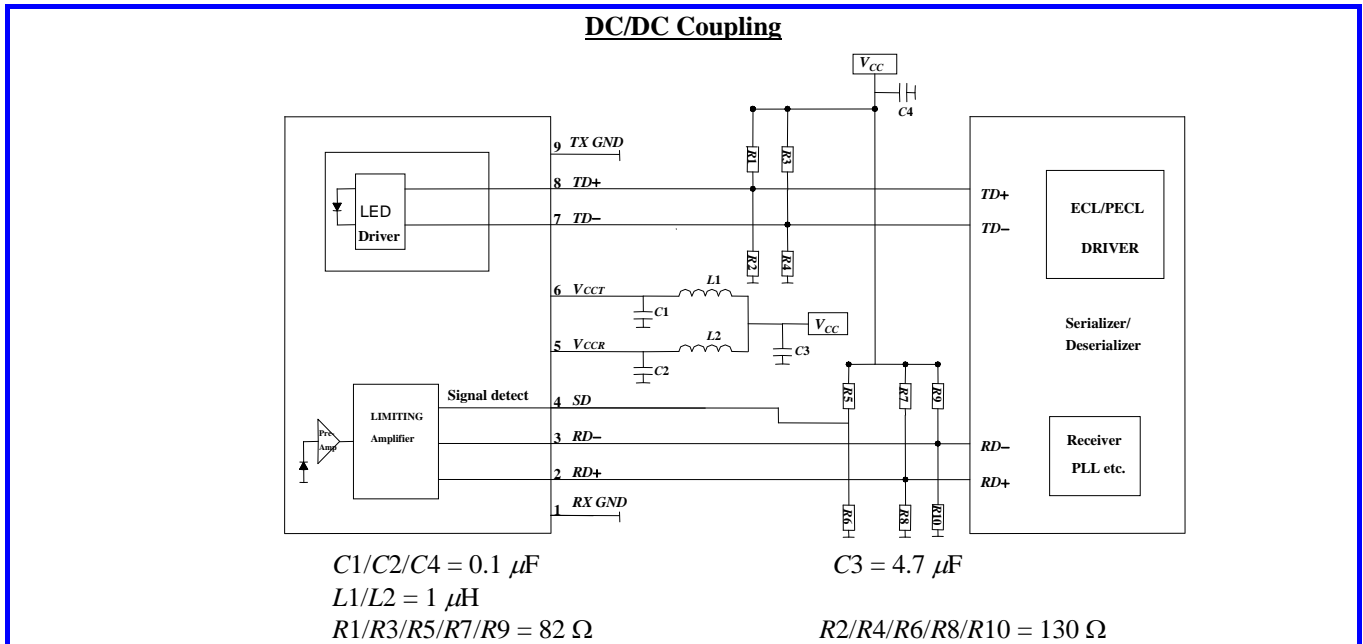
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**Connection Diagram**



PIN	SYMBOL	DESCRIPTION
1	<i>RX GND</i>	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	<i>RD+</i>	<i>RD+</i> is an open-emitter output circuit. Terminate this high-speed differential PECL output with standard PECL techniques at the follow-on device input pin. (See recommended circuit schematic)
3	<i>RD-</i>	<i>RD-</i> is an open-emitter output circuit. Terminate this high-speed differential PECL output with standard PECL techniques at the follow-on device input pin. (See recommended circuit schematic)
4	<i>SD</i>	Signal Detect. Normal optical input levels to the receiver result in a logic “1” output, $V_{OH}$ , asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output $V_{OL}$ , deasserted Signal Detect is a single-ended PECL output. <i>SD</i> can be terminated with PECL techniques via $50\ \Omega$ to $V_{CCR} - 2\text{ V}$ . Alternatively, <i>SD</i> can be loaded with a $510\ \Omega$ resistor to <i>RX GND</i> to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a LVPECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	<i>VCCR</i>	Receiver Power Supply. Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>VCCR</i> pin.
6	<i>V CCT</i>	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>V CCT</i> pin.
7	<i>TD-</i>	Transmitter Data In-Bar. Terminate this high-speed differential PECL input with standard PECL techniques at the transmitter input pin. (See recommended circuit schematic)
8	<i>TD+</i>	Transmitter Data In. Terminate this high-speed differential PECL input with standard PECL techniques at the transmitter input pin. (See recommended circuit schematic)
9	<i>TX GND</i>	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.

### Recommended Circuit Schematic



In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic.

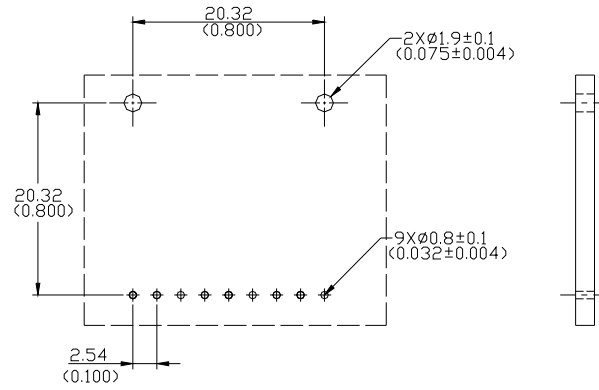
When designing the circuit interface, there are a few fundamental guidelines to follow.

- (1) The differential data lines should be treated as 50  $\Omega$  Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.
- (2) For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.
- (3) Multi layer plane PCB is best for distribution of  $V_{CC}$ , returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.
- (4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress  $V_{CC}$  noise over a broad frequency range, this prevents receiver sensitivity degradation due to  $V_{CC}$  noise.
- (5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1  $\mu\text{F}$  capacitors and a surface-mount coil inductor for 1  $\mu\text{H}$  inductor. Ferrite beads can be used to replace the coil inductors when using quieter  $V_{CC}$  supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the  $V_{CC}$  pins of the receiver and transmitter.
- (6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.



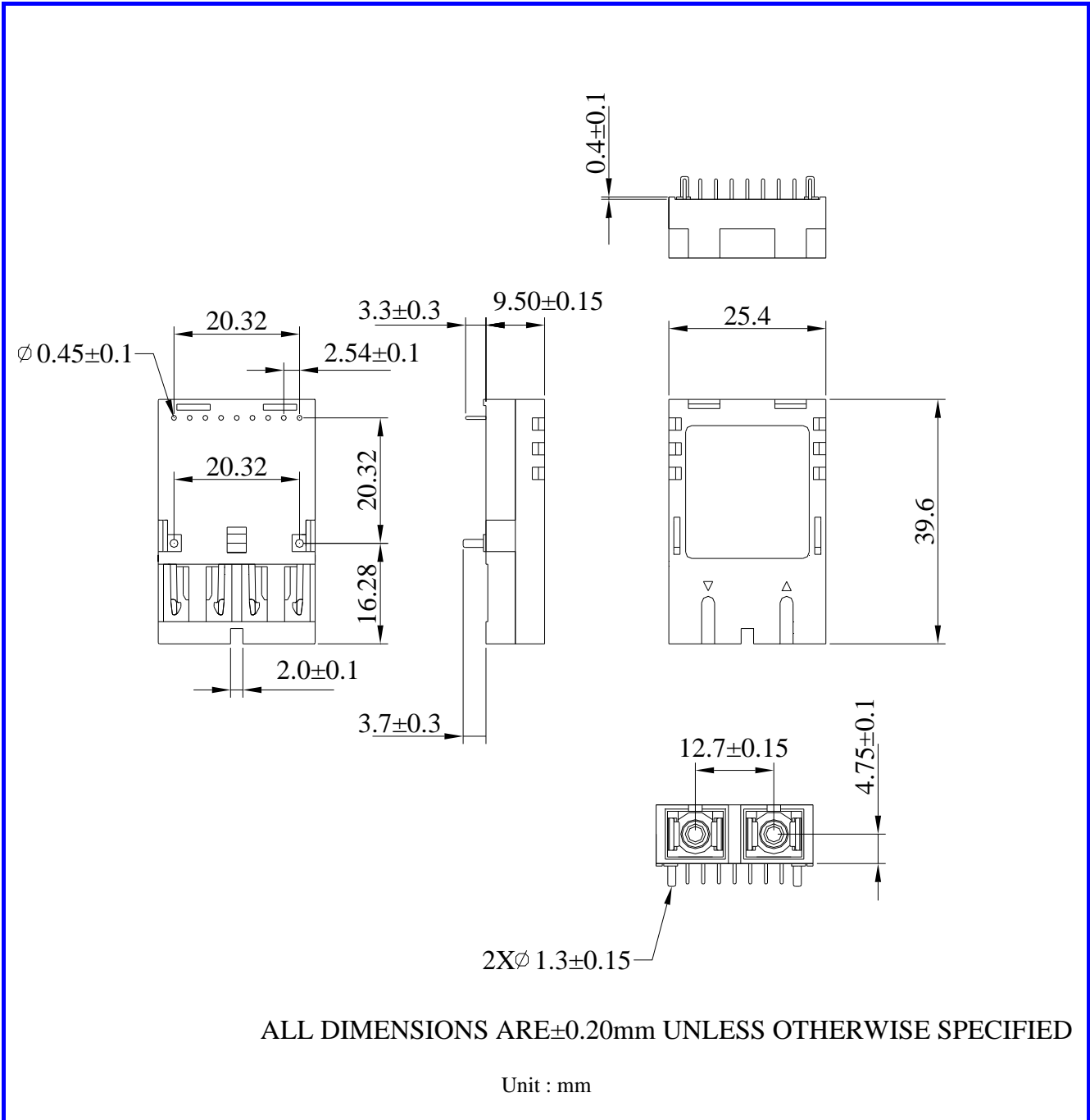
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### Recommended Board Layout Hole Pattern



Unit : mm(inches)

### Drawing Dimensions



**Note : All information contained in this document is subject to change without notice.**