

# Shenzhen Leadtek Electronics Co.,Ltd

## PRODUCT SPECIFICATION

### TFT-LCD MODULE

**Module No:** LTK040WVBLM10-V0

☒ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
<i>jona</i>	<i>tom</i>	<i>lan</i>

### Final Approval by Customer

Approved by	Comment

※The specification of "TBD" should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.



1.Document Revision History

Version	Contents	Date	Note
V0	NEW	2023.10.07	



## 2. General Description

No	Item	Specification	Unit
1	Screen Size	3.97	inch
2	LCD Type	TFT	mm
3	LCD manufacturer	BOE	mm
4	Viewing Direction	ALL O'CLOCK	Best Image
5	Display Mode	480*3RGB (H) X800 (V)	Pixel
6	Resolution	Normally Black	-
7	Active Area	51.84 (H) *86.40 (V)	mm
8	Outline Dimension	56.34 (H) *95.70 (V) *2.0 (T)	mm
9	Driver IC	ST7701S	without RAM
10	Interface	2 lines MIPI	-
11	Back Light	White Led*8	-
12	Operating temperature	-20 ~ +70	℃
13	Storage temperature	-30 ~ +80	℃
14	Weight	TBD	g

## 3.EXTERNAL DIMENSIONS



## 4. Interface Specification

NO.	Symbol	Function	Remark
1	GND	Power Ground	
2	MTP_PWM(NC)	NC	
3	IOVCC 1.8V	I/O Power supply : 1.65V ~ 3.3V	
4	VCI 2.8V	Power supply : 2.6V ~ 3.6V	
5	TE	Tearing effect output pin is used to synchronize MCU frame writing,	
6	GND	Power Ground	
7	MIPI_1P	MIPI-DSI clock data Lane 1 pegative-end input/output pin.	
8	MIPI_1N	MIPI-DSI clock data Lane 1 nositive-end input/output pin.	
9	GND	Power Ground	
10	MIPI_CKP	MIPI-DSI clock data Lane pegative-end input pin.	
11	MIPI_CKN	MIPI-DSI clock data Lane nositive-end input pin.	
12	GND	Power Ground	
13	MIPI_0P	MIPI-DSI clock data Lane 1 pegative-end input/output pin.	
14	MIPI_0N	MIPI-DSI clock data Lane 1 nositive-end input/output pin.	
15	GND	Power Ground	
16	GND	Power Ground	
17	NC	NC	
18	LEDK	Power supply for backlight cathode input terminal.	
19	LEDK	Power supply for backlight cathode input terminal.	
20	LEDA	Power supply for backlight anode input terminal.	

21	LEDA	Power supply for backlight anode input terminal.	
22	NC	NC	
23	GND	Power Ground	
24	NC	NC	
25	RESET	Reset signal input terminal. Active at 'L'.	
26	CTP_RST	Touch panel reset	
27	CTP_SCL	Touch panel I2C clock	
28	CTP_SDA	Touch panel I2C data	
29	CTP_INT	Touch panel interrupt output	
30	CTP_VCC	Touch panel Power supply 2.8~3.3V	

## 5. Electrical Characteristics

### 5.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	IOVCC	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VCC	2.6	2.8	3.6	V

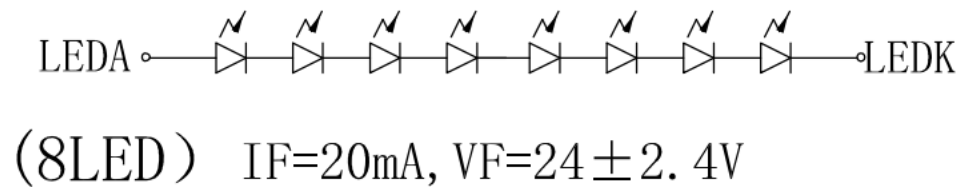
## 5.2 LED Backlight Specification

The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Item	Symbol	Min	Typ	Max	Unit	Notes
Forward voltage	Vf	21.6	24.0	26.4	V	--
Forward current	IF	--	20	--	mA	--
Luminance(With LCD)	Lv	--	300	-	cd/m <sup>2</sup>	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:(1) The "LED life time" is defined as the module brightness decrease to 50% of original brightness at IL=20mA/LED. The LED life time could be decreased if operating IL is larger than 25mA/LED.

### LED circuit:



## 6.Timing Characteristics

### Timing POWER ON/OFF SEQUENCE

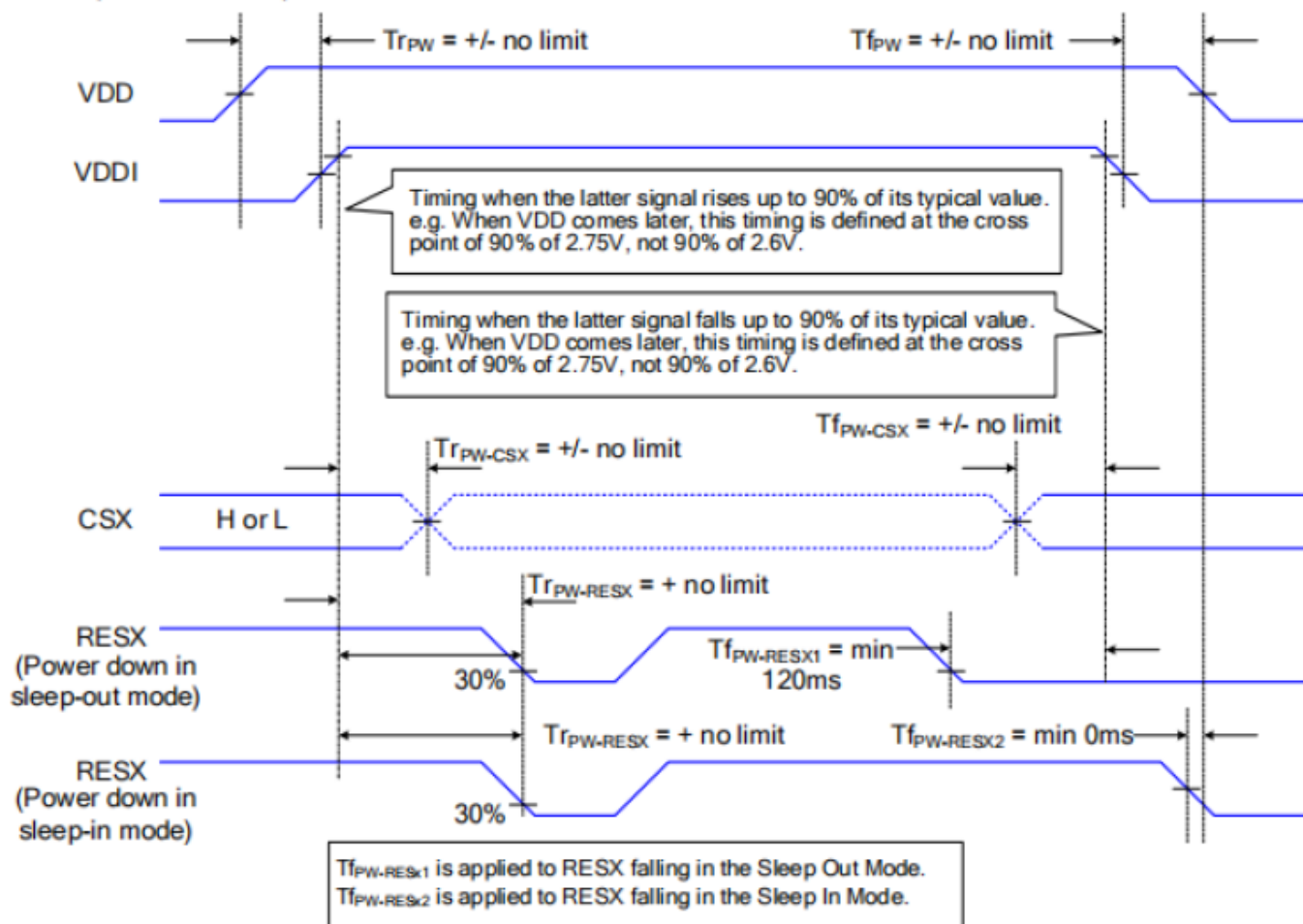
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below





## DSI-MIPI Interface Timing Characteristics of IC

### High Speed Mode



### DSI clock channel timing

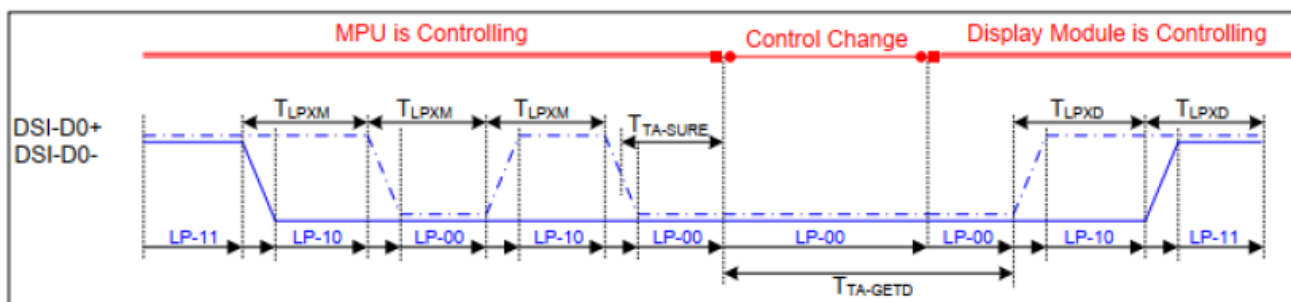
#### Rising and falling time on clock and data channel

$V_{DDI}=1.8, V_{DD}=2.8, A_{GND}=D_{GND}=0V, T_a=25^{\circ}C$

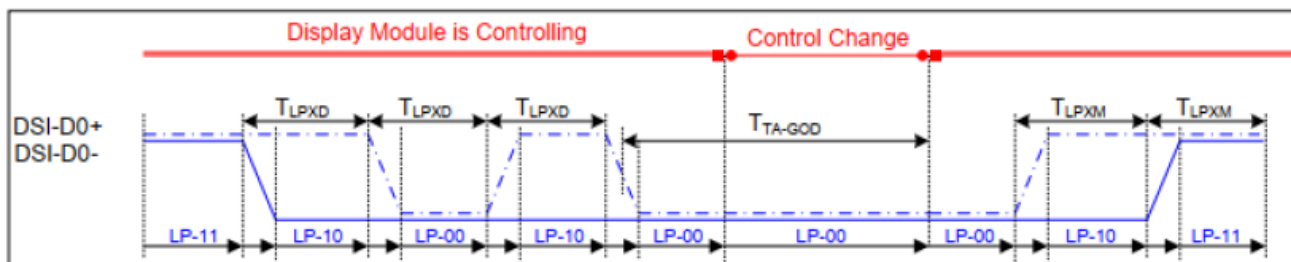
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xU_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	$U_{INSTA}$ $U_{INSTB}$	UI instantaneous halves	2	12.5	ns	$UI = U_{INSTA} = U_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

### Mipi Interface- High Speed Mode Timing Characteristics

### Low Power Mode



#### Bus Turnaround (BTA) from display module to MPU Timing



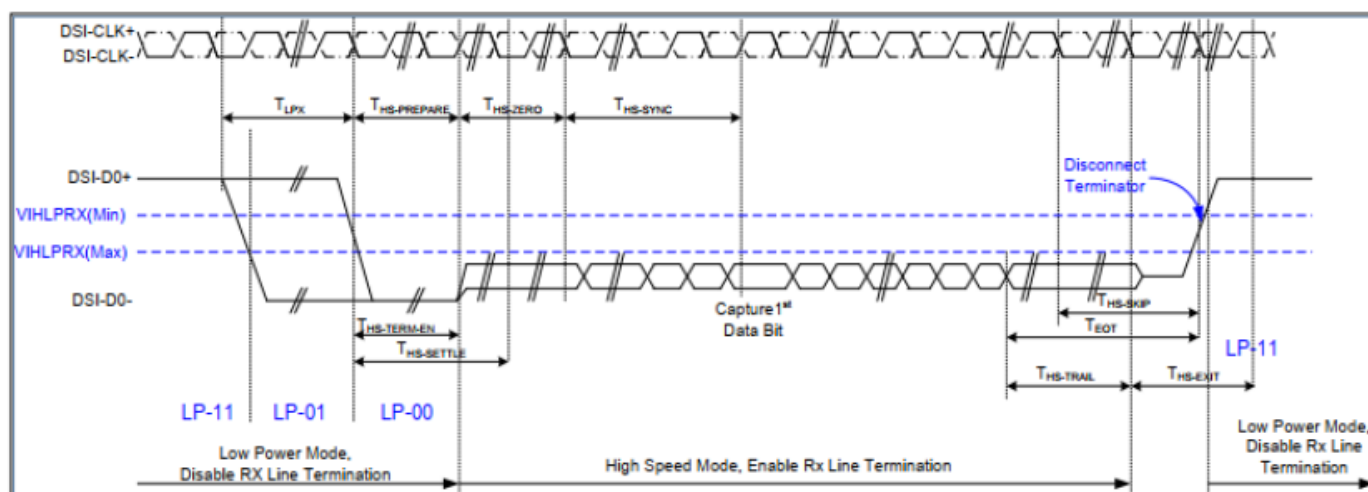
#### Bus Turnaround (BTA) from MPU to display module Timing

$VDDI=1.8, VDD=2.8, AGND=DGND=0V, T_a=25\text{ }^{\circ}\text{C}$ 

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	$T_{LPXD}$	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5 \times T_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4 \times T_{LPXD}$		ns	Output

Mipi Interface Low Power Mode Timing Characteristics

## DSI Bursts Mode



The diagram illustrates the timing relationships for DSI HS mode. It features two signal traces: DSI-CLK+ / DSI-CLK- (clock) and DSI-D0+ / DSI-D0- (data). The clock signal transitions between HS-0/1, HS-0, LP-11, LP-01, LP-00, HS-0, and HS-0/1 states. The data signal is shown in a high-impedance state during the LP-11, LP-01, and LP-00 states. Key timing parameters are indicated by arrows and labels:  $T_{EOT}$  (End of Transaction),  $T_{CLK-MISS}$  (Clock Miss),  $T_{CLK-SETTLE}$  (Clock Settle),  $T_{CLK-TERMEN}$  (Clock Termination),  $T_{CLK-POST}$  (Clock Post),  $T_{CLK-TRAIL}$  (Clock Trail),  $T_{HS-EXIT}$  (HS Exit),  $T_{LPX}$  (LP Exit),  $T_{CLK-PREPARE}$  (Clock Prepare),  $T_{CLK-ZERO}$  (Clock Zero),  $T_{CLK-PRE}$  (Clock Pre),  $T_{HS-PRERE$  (HS Pre),  $T_{HS-SKIP}$  (HS Skip), and  $T_{HS-EXIT}$  (HS Exit). The diagram also shows the voltage levels for  $VIHLPRX(\text{Min})$  and  $VIHLPRX(\text{Max})$ .

### Clock lanes- High Speed Mode to/from Low Power Mode Timing

$VDDI=1.8, VDD=2.8, AGND=DGND=0V, T_a=25\text{ }^{\circ}\text{C}$ 

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105ns+12 UI	ns	Input

## Reset Description:

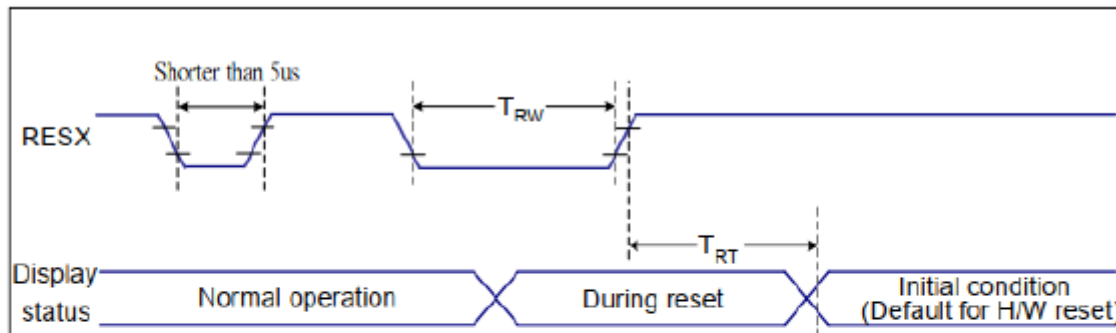


Figure 9 Reset Timing

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

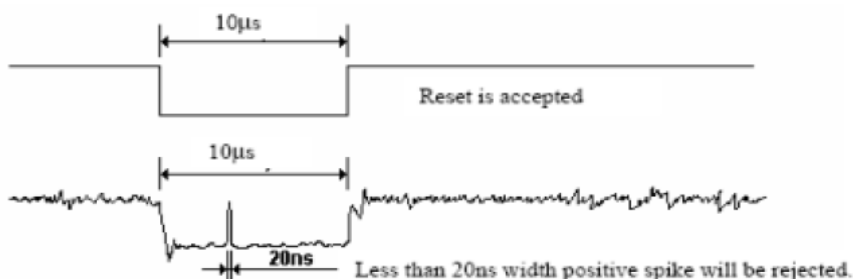
### Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

- Spike Rejection also applies during a valid reset pulse as shown below:



- When Reset applied during Sleep In Mode.

- When Reset applied during Sleep Out Mode.

- It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 7.Optical Specification

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Response time	Tr+Tf	$\Theta=0^{\circ}$ $\varnothing=0^{\circ}$ $T_a=25^{\circ}\text{C}$		35		ms	
Contrast ratio	Cr		550	800			
Color gamut	S (%)		-	-		%	
Luminance uniformity	WHITE		80			%	
Viewing angle range	$\Theta_{x+}$	$CR \geq 10$ $T_a=25^{\circ}\text{C}$	80	85		deg	
	$\Theta_{x-}$		80	85		deg	
	$\Theta_{y+}$		80	85		deg	
	$\Theta_{y-}$		80	85		deg	
LCM Luminance (with TP)	LV	$\Theta=0^{\circ}$ $\varnothing=0^{\circ}$ $T_a=25^{\circ}\text{C}$		300			
CIE(X,Y)Chromaticity	White(X)		0.277	0.292	0.307		
	White(Y)		0.318	0.333	0.348		

**Note:**

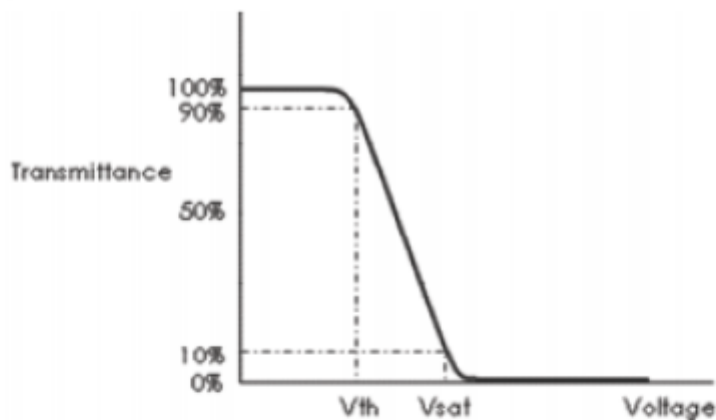
1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).
2. Contrast measurements shall be made at viewing angle of  $\Theta = 0$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

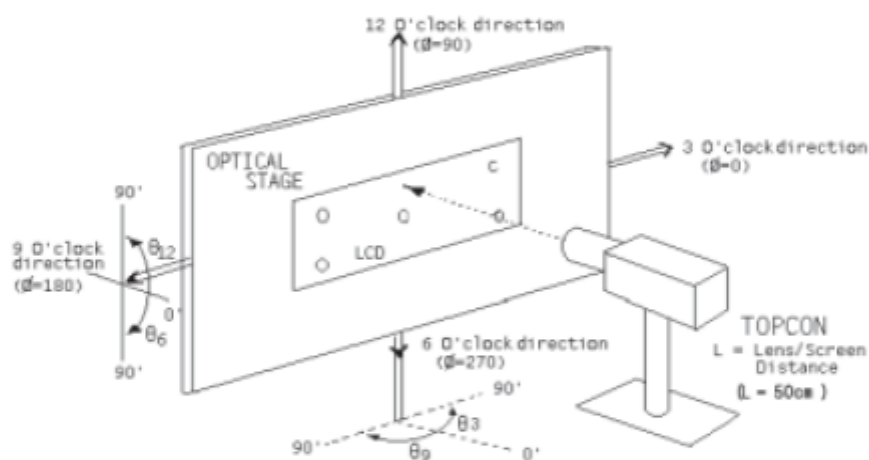
3. Transmittance is the Value with Polarizer
4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is  $T_r$ , and 90% to 10% is  $T_d$ .



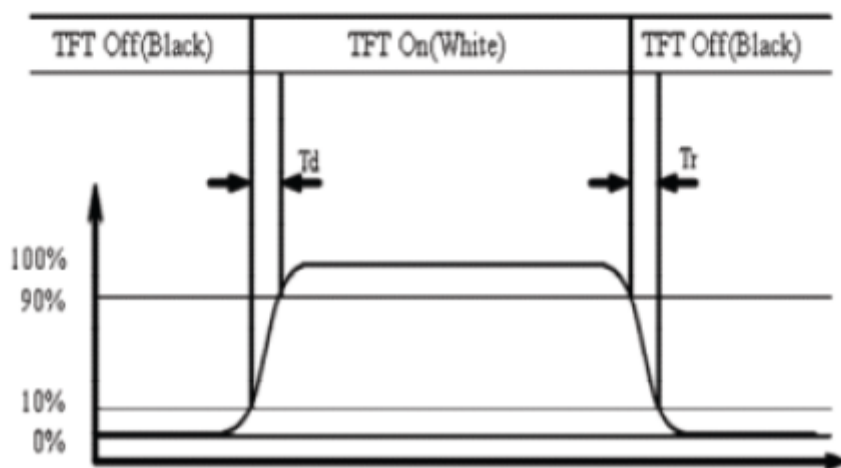
**Figure 1. The Definition of  $V_{th}$  &  $V_{sat}$**



**Figure 2. Measurement Set Up**



**Figure 3. Response Time Testing**





## 8. Reliability Test Items

Item	Test Condition	Criterion
High Temperature Operation	70 °C, 48 hrs	Note1, Note2
Low temperature operation	-20 °C, 48 hrs	
High Temperature Storage	80 °C, 48 hrs	
Low Temperature Storage	-30 °C, 48 hrs	
High Temp. & High Humidity Storage	40 °C, 80% RH, 48hrs	
Thermal Shock (Static)	-20°C, 30 min /60°C, 30 min, 20 cycles	

Note1: Evaluation should be tested after storage at room temperature for two hours.

Note2:

Pass: Normal display image no line defect.

Fail: No display image, or line defects.

Partial transformation of the module parts should be ignored.

## 9. Precautions

Please pay attentions to the followings as using the LCD module.

### Handling

- (a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.
- (b) Because the polarizer is very fragile and easy to be damaged, do not hit, press or rub the display's surface with hard materials.
- (c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.
- (d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

- (e) Avoid using Ketone type materials (e.g. Acetone), Toluene, Ethyl acid or Methyl chloride to clean the display surface. It might damage the touch panel surface permanently. The recommended solvents are water and Isopropyl alcohol.
- (f) Wipe off water droplets or oil immediately.
- (g) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.
- (h) Do not touch the output pins directly with bare hands.
- (i) Do not disassemble the LCD module.
- (j) Do not lift the FPC of Touch Panel.

## Storage

- (a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.
- (b) Do not expose the LCD modules to sunlight directly.
- (c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.
- (d) Avoid condensation of water. It may cause improper operation.
- (e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

Operation (a) When mounting or dismounting the LCD modules, turn the power off.

- (b) Protect the LCD modules from electric shock.
- (c) The Driver IC control algorithms stated above should always be obeyed to avoid damaging the LSI and electronic circuit.
- (d) Be careful to avoid mixing up the polarity of power supply for backlight.
- (e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.
- (f) When a static image is displayed for a long time, remnant image is likely to occur.
- (g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.
- (h) Most of the touch screens have air vent to equalize the inside air pressure to the outside one. The air vent must

be open and liquid contact must be avoided as the liquid may be absorbed if the liquid is accumulated near the air vent.

(i) For the fragility of ITO film, it should avoid to use too tapering pen as the input material.

(a) If a cushion is used between bezel/housing and film must be choose as free as enough to absorb the expansion and contraction to avoid the distortion of film.

(b) The cushion must be placed out of the Viewing Area.

(c) Bezel/Housing edge must be posited between Key Area and Viewing Area. The edge enters the Key Area may cause unexpected input if the gap is too narrow or foreign particles like dusts exist between Bezel/Housing and ITO film.

(d) Mounting example:

The corner part has conductivity. Do not touch any metal part after mounting.

## Others

a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

b) For the fragility of polarizer, it is recommended to attach a transparent protective plate over the display surface.

c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic charge can be minimized.

## 10.HSF Requirements

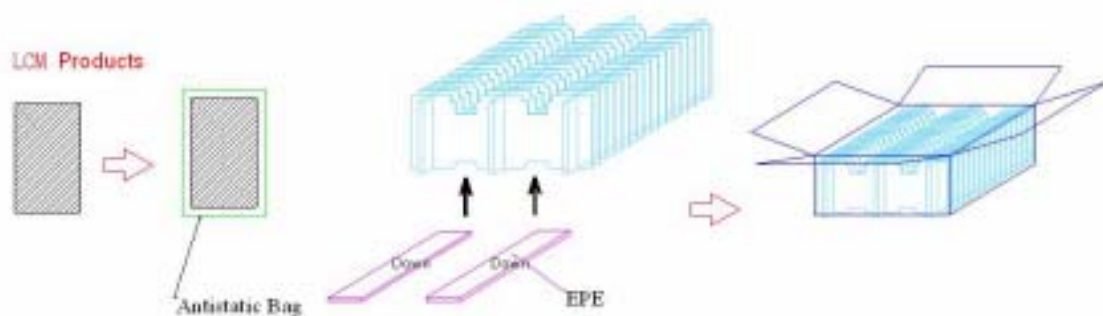
☒ RoHS( Restriction of the use of certain Hazardous Substances)

☐ HF (Halogen Free)

☐ REACH (Regulation the Registration, Evaluation, Authorization and Restriction of Chemicals)

☐ Other regulations

## 11.Packaging diagram



### 第一步

将产品装入静电袋

### 第二步

把长卡、短卡组成卡阵（短卡朝向一致）形状和数量按照 BOM 实际物料，卡阵底部放对应的白色珍珠棉后装箱

### 第三步

每个卡槽内放两片产品，2 片产品显示面相对，中间粉色珍珠棉一起

### First step

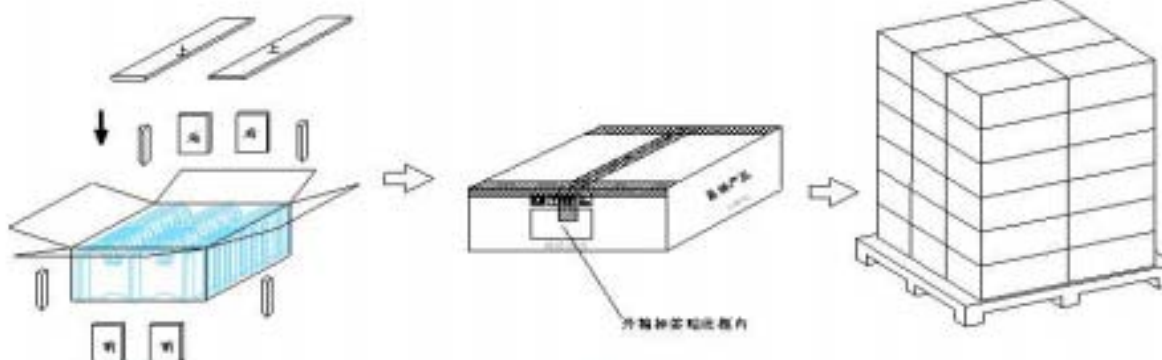
Putting every piece of LCM into anti-static bag.

### Second step

Assemble a carton matrix with the right white EPE down below ,then place them into the carton.

### Third step

Put a pink EPE between 2 pcs products(face to face) while insert all of them into the carton matrix.



### 第四步

装箱后，按照 BOM 实际物料在纸箱内侧与卡阵避空位置放白色泡棉

### 第五步

用胶带封箱，贴外箱标签

### 第六步

将箱子整齐的放在栈板上并包裹，最高可堆叠泡棉：6 层：

### Fourth step

Insert all other white EPE into the right place of the carton matrix .

### Fifth step

seal the carton with cellulose tape ;Stick on a carton label,

### Sixth step

Place the boxes together on a pallet (6 layers at most),

## 12.IIS Standard

### 12. INSPECTION STANDARD

#### 12.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

##### 12.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM CHENGHAO TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 TO 40 ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

##### 12.1.2. INCOMING INSPECTION

###### (A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

###### (B) THE STANDARD OF QUALITY

ISO-2859-1 ( SAME AS MIL-STD-105E ) , LEVEL SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

###### (C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED.

PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

##### 12.1.3. WARRANTY POLICY

CHENGHAO WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. U.R.T. WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF CHENGHAO.

#### 12.2. CHECKING CONDITION

12.2.1. CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

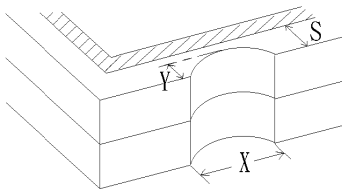
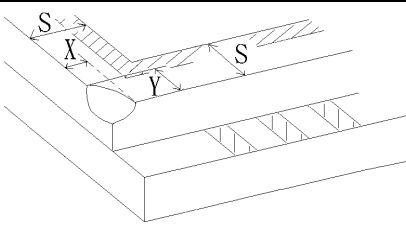
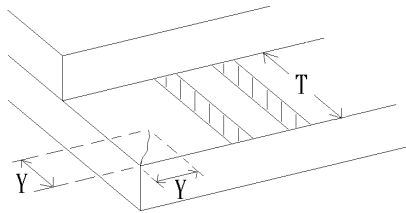
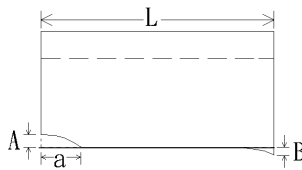
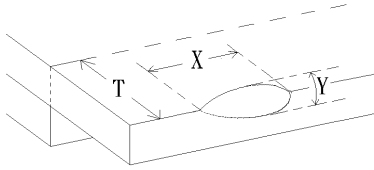
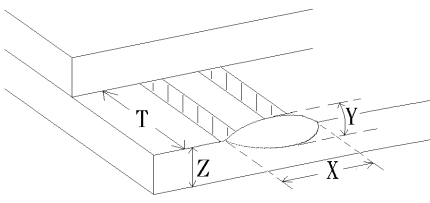
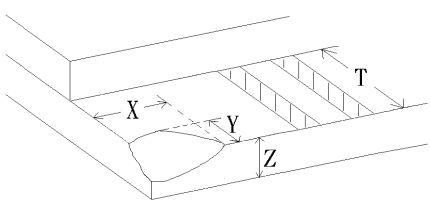
12.2.2. CHECKER SHALL SEE OVER 300±25 mm WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

### 12.3. INSPECTION PLAN :

CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA .....REJECTED	Minor
	6. BLEMISH, BLACK SPOT, WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION ( INSIDE VIEWING AREA )	Minor
	7. BLEMISH, BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION ( INSIDE VIEWING AREA )	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION ( INSIDE VIEWING AREA )	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR ( OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE ( IF NEEDED, AND INSIDE VIEWING AREA )	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS ( CONTRAST, VOP, CHROMATICITY ... ETC )	ACCORDING TO SPECIFICATION OR DRAWING . ( INSIDE VIEWING AREA )	Critical
	11.MISSING LINE	MISSING DOT, LINE, CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT, WRONG PATTERN DISPLAY	NO DISPLAY, WRONG PATTERN DISPLAY, CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. DOT DEFECT (FOR COLOR AND TFT)	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

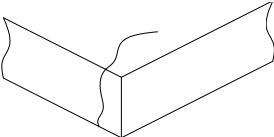
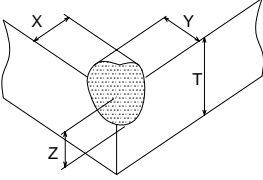
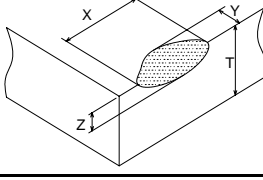
## 12.4. STANDARD OF VISUAL INSPECTION

NO.	CLASS	ITEM	JUDGEMENT																																	
12.4.1	MINOR	BLACK AND WHITE SPOT FOREIGN MATERIEL DUST IN THE CELL BLEMISH SCRATCH	<div>(A) ROUND TYPE: <span>unit : mm.</span><table><tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr><tr><td><math>\Phi \leq 0.1</math></td><td>DISREGARD</td></tr><tr><td><math>0.1 &lt; \Phi \leq 0.25</math></td><td>3 (D&gt;5mm)</td></tr><tr><td><math>0.25 &lt; \Phi</math></td><td>0</td></tr></table><div>NOTE: <math>\Phi=(\text{LENGTH}+\text{WIDTH})/2</math></div><div>(B) LINEAR TYPE: <span>unit : mm.</span><table><tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr><tr><td>-----</td><td><math>W \leq 0.03</math></td><td>DISREGARD</td></tr><tr><td><math>L \leq 5.0</math></td><td><math>0.03 &lt; W \leq 0.07</math></td><td>3 (D&gt;5mm)</td></tr><tr><td>-----</td><td><math>0.07 &lt; W</math></td><td>FOLLOW ROUND TYPE</td></tr></table></div></div>	DIAMETER (mm.)	ACCEPTABLE Q'TY	$\Phi \leq 0.1$	DISREGARD	$0.1 < \Phi \leq 0.25$	3 (D>5mm)	$0.25 < \Phi$	0	LENGTH	WIDTH	ACCEPTABLE Q'TY	-----	$W \leq 0.03$	DISREGARD	$L \leq 5.0$	$0.03 < W \leq 0.07$	3 (D>5mm)	-----	$0.07 < W$	FOLLOW ROUND TYPE													
DIAMETER (mm.)	ACCEPTABLE Q'TY																																			
$\Phi \leq 0.1$	DISREGARD																																			
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-----	$W \leq 0.03$	DISREGARD																																		
$L \leq 5.0$	$0.03 < W \leq 0.07$	3 (D>5mm)																																		
-----	$0.07 < W$	FOLLOW ROUND TYPE																																		
12.4.2	MINOR	BUBBLE IN POLARIZER DENT ON POLARIZER	<div><span>unit : mm.</span><table><tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr><tr><td><math>\Phi \leq 0.2</math></td><td>DISREGARD</td></tr><tr><td><math>0.2 &lt; \Phi \leq 0.5</math></td><td>2 (D&gt;5mm)</td></tr><tr><td><math>0.5 &lt; \Phi</math></td><td>0</td></tr></table></div>	DIAMETER	ACCEPTABLE Q'TY	$\Phi \leq 0.2$	DISREGARD	$0.2 < \Phi \leq 0.5$	2 (D>5mm)	$0.5 < \Phi$	0																									
DIAMETER	ACCEPTABLE Q'TY																																			
$\Phi \leq 0.2$	DISREGARD																																			
$0.2 < \Phi \leq 0.5$	2 (D>5mm)																																			
$0.5 < \Phi$	0																																			
12.4.3	MINOR	Dot Defect	<table><tr><th>Items</th><th>ACC. Q'TY</th></tr><tr><td>Bright dot</td><td><math>N \leq 4</math> (D&gt;5mm)</td></tr><tr><td>Dark dot</td><td><math>N \leq 4</math> (D&gt;5mm)</td></tr></table> <div>Pixel Define<table><tr><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td></tr><tr><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td></tr><tr><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td></tr></table><div>Not 1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot. Not 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. Not 3: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green ,blue pattern.</div></div>	Items	ACC. Q'TY	Bright dot	$N \leq 4$ (D>5mm)	Dark dot	$N \leq 4$ (D>5mm)	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
Items	ACC. Q'TY																																			
Bright dot	$N \leq 4$ (D>5mm)																																			
Dark dot	$N \leq 4$ (D>5mm)																																			
R	G	B	R	G	B	R	G	B																												
R	G	B	R	G	B	R	G	B																												
R	G	B	R	G	B	R	G	B																												

NO.	CLASS	ITEM	JUDGEMENT
12.4.4	MINOR	LCD GLASS CHIPPING	 $Y > S$ Reject
12.4.5	MINOR	LCD GLASS CHIPPING	 $X \text{ or } Y > S$ Reject
12.4.6	MAJOR	LCD GLASS GLASS CRACK	 $Y > (1/2) T$ Reject
12.4.7	MAJOR	LCD GLASS SCRIBE DEFECT	 <ol style="list-style-type: none"> <li><math>a &gt; L/3</math>, <math>A &gt; 1.5\text{mm}</math>. Reject</li> <li>B : ACCORDING TO DIMENSION</li> </ol>
12.4.8	MINOR	LCD GLASS CHIPPING ( ON THE TERMINAL AREA )	 $= (x+y)/2 > 2.5 \text{ mm}$ Reject
12.4.9	MINOR	LCD GLASS CHIPPING ( ON THE TERMINAL SURFACE )	 $Y > (1/3) T$ Reject
12.4.10	MINOR	LCD GLASS CHIPPING	 $Y > T$ Reject



## 12.5 INSPECTION STANDARD OF TOUCH PANEL (Contains the CTP)

NO.	CLASS	ITEMS		JUDGEMENT	
12.5.1	MAJOR	Touch Panel Crack			Reject
12.5.2	MINOR	Touch Panel Chipping	Corner	 $X \leq 2\text{mm}, Y \leq 2\text{mm}, Z < 1/2T$	Accept
			Edge	 $X \leq 3\text{mm}, Y \leq 3\text{mm}, Z < 1/2T$	Accept
12.5.3	MINOR	Scratch Dust and Foreign materiel (Linear Type)	$W \leq 0.05, L \leq 5.0\text{mm}$		Accept
			$0.05\text{mm} < W \leq 0.07\text{mm}; L \leq 5.0\text{mm}$ Distance between scratch $> 5.0\text{mm}$		Accept 3 ea Max.
			$W > 0.07\text{mm}$		Reject
12.5.4	MINOR	Scratch Dust and Foreign materiel (Round Type : $\leq (\text{Length} + \text{Width})/2$ )	$0.25\text{mm}$		Accept
			$0.25\text{mm} < \leq 0.35\text{mm}$ Distance between spots $> 5.0\text{mm}$		Accept 5 ea Max.
			$> 0.35\text{mm}$		Reject
12.5.5	MINOR	Touch Panel Dent / Fish Eyes	$0.35\text{mm}$		Accept
			$0.35\text{mm} < \leq 1.0\text{mm}$ Distance $> 5.0\text{mm}$		Accept 3 ea Max.
			$> 1.0\text{mm}$		Reject
12.5.6	MINOR	Touch Panel Air Bubble	$0.2\text{mm}$		Accept
			$0.2\text{mm} < \leq 0.5\text{mm}$ Distance between bubbles $> 5.0\text{mm}$		Accept 3 ea Max.
			$> 0.5\text{mm}$		Reject
12.5.7	MINOR	Touch Panel Printing area Scratch	$0.03\text{mm} < W \leq 0.05\text{mm}, L \leq 5\text{mm}$ Distance between scratch $> 5.0\text{mm}$		Accept 3 ea Max.
			$W > 0.05\text{mm}$ or $L > 5\text{mm}$ ( $W > 0.05$ Follow 8.5.4 Round type )		Reject
12.5.8	MINOR	Touch Panel White Haze Mark / Dust		Can not be removed	Reject