Titan2 Series FPGA Device Data Sheet

(DS05001 , V1.1)

(2021.8.20)

revision history

date	revision	Description
2020.8.31	V0.1	Initial Alpha version released.
2021.1.20	V0.2	1.Delete the equivalent LUT4 resource description in Table 1-1, and add the logical unit resource description; 2.Table 1-3 adds "Titan2 Board Hardware Design Guide"; 3.Table 2-1, Table 2-2 add $V_{CCA\_IO\_G0}$ voltage description ; 4.Table 2-3, increase the typical value of "n" and "r"; 5.Add Table 2-5 HP I/O The maximum allowable overshoot and undershoot voltage of VIN; 6.Table 2-6 Typical quiescent current increase $V_{CCA\_IO\_G0}$ quiescent current description; 7.Table 2-9 The value of CDM_SERDES in ESD and Latch-Up indicators is changed to ±250V; 8.Updated chapter 3.2 I/O DC characteristic parameters; 9.Modify Table 4-6 DQS AC characteristic data; 10.Table 4-11, T_{PL} and T_{POR} values ; 11.Modify Table 5-1 HR I/O LVDS performance.
2021.2.3	V0.3	Chapter 3.1 adds hot swap instructions
2021.3.5	V0.4	Errata, modify Table 1-1, the number of logical units is 389760
2021.4.15	V0.5	1. Update Table 2-1, Table 2-2 $V_{CCA\_IO\_G0}$ data ; 2. Table 2-3 IPU, IPD_{data} update ; 3. Chapter 3.1 adds V_{CC} and V_{CCA} power-on requirements ; 4. Update the hot swap instructions in Chapter 3.1; 5. Table 4-12 increase slave serial DI setup time and DI hold time CFG_CLK falling edge data, and the minimum value of CFG_CLK to CSO_DOUT ; 6. Modify Table 5-2 HP I/O LVDS performance; 7. Modify Table 5-6 APM performance; 8. Update Table 7-8 data; 9. Update Table 7-9 HSST_$T_{RXIDLETIME}$ and HSST_RX $_{VPPOOB}$ data .
2021.5.11	V0.6	1. Add abbreviation description; 2. Update inaccurate instructions in documentation; 3. Add notes to each table; 4. Update Table 2-3 IPU, IPD_{data} ; 5. Table 2-6 The maximum quiescent current value when updating 100 degrees; 6. Update Table 2-9 ESD parameters, supplement V_{CCIO_CFG} and the HBM_IO value of the dedicated configuration input IO; 7. Table 2-10 T_j The maximum temperature is changed to 100℃; 8. Update the description of power-on and power- off and hot -plug, update the power-on and power-off sequence to logical power-on and power-off sequence, add 3.1.4 The overall power-on and power-off sequence, update the pull-up resistor value of the hot-swappable I2C bus application scenario; 9. Update the standard input and output voltage range of LVCOM15 level in Table 3-2 ; 10. Table 3-5 delete MIPI level standard; 11. Table 3-6 Added SSTL12D level standard DC characteristic parameters; 12. Update Table 4-1, Table 4-2, Table 4-3 AC characteristic parameters;

		13. DQS AC characteristics increase HR IO DQS parameter; HP IO memory interface performance remove LPDDR ; DDR2 , QDRII +, RLDRAM3, RLDRAM2 rate to TBD ; 15. Updated Table 7-3 , Table 7-8 , Table 7-9 data.
2021.6.30	V1.0	1. Table 2-3 Update R_{INTERM} , I_{PU} , I_{PD} data, add notes to Table 2-3 ; 2. Update Table 2-6 Quiescent current , the table contains typical quiescent current and maximum quiescent current and adds relevant instructions; 3. Table 2-7 Power up ramp-up time increase HSSTAVCC, HSSTAVCCPLL, HSSTVCCA Supply Ramp rise time; 4. Update ESD in Table 2-9 parameter; 5. Chapter 3.1.1 updated the power-on and power-off requirements , and chapter 3.1.3 added the description of the power-on and power-off sequence of the HSST power supply , and added the description of hot-swap specifications; Added the precautions for prohibiting power on and off , and added the description of the conditions for simultaneous power off ; 6. Update the VICM minimum value of LVDS in Table 3-3 to 1.0V ; 7. Table 3-4 , Table 4-13 Delete the relevant description of MIPI level standard; 8. Update Figure 4-1 Power up Timing feature ; 9. Update the incorrectly merged cells in Table 4-4 and Table 4-5 ; 10. Table 4-12 Slave Serial,Slave The frequency of Parallel and internal slave parallel is changed to 50M , and the pulse width is changed to 10ns ; 11. Update Table 5-3 , Table 5-4 The highest data rate of DDR interface; 12. Table 5-6 updates the performance of input and output registers using only APM ; 13. Table 7-4 HSST_Fhpll_max changed from 16Ghz to 8Ghz , HSST_Fhpll_max changed from 9Ghz to 4.5Ghz ; 14. Table 7-6 Modify the maximum value of $HSST\_T_{PLLLOCK\ to}$ 2.5ms ; 15. Update Table 7-8 HSST_TJ , HSST_DJ data; 16. Table 7-9 delete HSST_TRXIDLETIME, HSST_RXVPPOOB two parameters; 17. Update PCIe related parameters and descriptions; 18. Update HSSTHP maximum data rate to 12.5Gbps ; 19. Update DRM maximum performance ; 20. Update APM maximum performance ; 21. Update the input clock jitter of the GPLL to the input clock cycle jitter of the GPLL ; 22. Update the input clock jitter of the PPLL to the input clock cycle jitter of the GPLL ; 23. Update the maximum value of HSST_RRCLK parameter to 400 ; 24. Update CLM AC characteristic parameter value ; 25. Update DRM AC characteristic parameter value ; 26. Update APM AC characteristic parameter value ; 27. Update IOB AC characteristic parameter value ; 28. Update the value of the sinusoidal jitter tolerance parameter on the receiving side of the HSST ; 16. Update the HSST_VDINPP value in the HSST hard core DC parameters ;

2021.8.20	V1.1	1. Updated Figure 3-3 to delete RSTN signal; 2. Updated the description of the power-on and power-off sequence of HSST ; 3. Updated Figure 4-1 and Figure 4-2 to indicate power-on and reconfiguration features respectively, and corrected RSTN signal names; 4. Update Table 4-11, correct RSTN name ; 5. Table 4-1, add name column; 6. Table 4-12, add name column ; 29. surface 5-5, DRM(NW mode & read register enable) and DRM (synchronous FIFO mode & read register enable) for maximum performance.

This article mainly includes a brief description of the characteristics of Titan2 series FPGA devices, a list of product models and resource scales, AC and DC characteristics, etc. Users can learn about the characteristics of Titan2 series FPGA devices through this article, which is convenient for device selection.

1. Overview of Titan2 Series FPGAs

The Titan2 series programmable logic devices use a 28nm process. It includes modules such as configurable logic module (CLM) , dedicated 36Kb storage unit (DRM), arithmetic processing unit (APM), high-performance I/O , multi-function I/O and abundant on-chip clock resources, and integrates modulus Conversion module (ADC), PCIe and other hard core resources, support multiple configuration modes, and provide bit stream encryption and authentication, device ID (UID) and other functions to protect the user's design security. Based on the above characteristics, Titan2 series FPGA can be widely used in video, industrial control, communication, computer, medical, LED display security monitoring, instrumentation, consumer electronics and other application fields.

1.1. Features of Titan2 series FPGA products

- **High performance**
  - Mature 28nm CMOS process
  - 1.0V core voltage
- **Support a variety of standard IO**
  - Up to 500 user IO
  - HR I/O Support 1.2V to 3.3V IO standard
  - HP I/O 1.2V~1.8V
  - Support HSTL , SSTL , POD storage interface standards
  - Support differential standards such as LVDS, MINI-LVDS, TMDS (applied to HDMI, DVI interface)
  - Programmable IO BUFFER , high performance IO LOGIC
- **Flexible Programmable Logic Module CLM**
  - LUT6 logical structure
  - Each CLM contains 4 multi-function LUT6, 8 registers
  - Supports fast arithmetic carry logic
  - Distributed RAM support model
  - Support cascading chain
- **Supports DRM with multiple read and write modes**
  - A single DRM provides 36Kb of storage, configurable as 2 independent 18Kb storage blocks
  - Supports multiple operating modes, including single-port (SP) RAM, dual-port (DP) RAM, simple dual-port (SDP) RAM, ROM, and FIFO modes
  - Dual-port RAM and simple dual-port RAM support dual-port mixed data widths
  - Support ECC function
  - Support Normal-Write, Transparent-Write and Read-before-Write three write modes
  - Support Byte-Write function
  - Optional address latches, output registers
- **Efficient Arithmetic Processing Unit APM**
  - Each APM supports one 25*18 operation or

two 12*9 operations
- Support input and output registers
- Support 48bit addition
- Support for signed data operations

➢ Integrated ADC hard core

- 12bit resolution, 1MSPS (independent ADC dual core) sampling rate
- Up to 12 input channels
- Integrated temperature sensor

➢ Rich clock resources

- Supports Class 3 clock network for flexible configuration
- Support global clock (GLOBAL CLOCK) network
- Support for REGIONAL CLOCK network
- Support for I/O CLOCK (I/O CLOCK) network
- Integrate multiple PLLs, each supporting up to 5 clock output

➢ Flexible configuration

- Supports multiple programming modes
- JTAG mode compliant with IEEE 1149.1, IEEE 1149.6 standards
- Master SPI can choose up to 8bit data bit width, effectively improving programming speed
- Support Slave Serial, Slave Parallel mode
- Support AES256-GCM bit stream encryption, support 96bit UID protection
- Support digital signature authentication for bitstream files
- Support for eFuse key storage
- Supports battery-backed RAM (BB-RAM) key storage for chip-level security
- Supports disabling bitstream readback
- Supports JTAG security management
- Support anti-DPA attack
- Support SEU error detection and correction
- Support multi-version bitstream fallback function
- Support watchdog timeout detection
- Support programming download tool Fabric Configuration
- Support online debugging tool Fabric Debugger

➢ High-performance memory interface

- HR I/O supports DDR3, DDR3L, DDR2, LPDDR, QDRII+, RLDRAM2
- HP I/O supports DDR4, DDR3, DDR3L, DDR2, QDRII+, RLDRAM3, RLDRAM
- Supports x4, x8, x16, x32, x64 bit widths

➢ High Performance High Speed Serial Transceiver HSSTHP

- Supports Data Rates up to 12.5Gbps
- Flexible configurable PCS, supporting PCIe GEN1/GEN2, Gigabit Ethernet, XAUI, Gige and other protocols

1.2. Titan2 series FPGA resource scale and packaging information

1-1 and Table 1-2 show the resource scale and package information of Titan2 series FPGAs .

Table 1-1 Titan2 Number of FPGA resources

Resource name		PG2T390H
CLM	LUT6	243600
	logical unit	389760
	FF	487200
	Distributed ram (Kb)	4712
DRM (36Kbits/ pc)		480
APM(units)		840
PLLs	GPLLs	10
	PPLLs	10
ADC (dual core)	Dedicated analog channel (differential input pair)	1
	Multiplexed analog channels (differential input pair)	11
SERDES LANE (1)		16
PCIE GEN2×8 CORE		1

Notes: 1. 4 LANEs form a HSSTHP

Table 1-2 Titan2 FPGA package information and user IO quantity

Device / Package information	PG2T390H		
	SERDES LANE	HR_I/O	HP_I/O
FFBG900 (31mm×31mm , 1.0mm)	16	350	150
FFBG676 (27mm×27mm , 1.0mm)	8	250	150

1.3. Brief description of Titan2 series FPGA

1.3.1. CLM

CLM (Configurable Logic Module) is the basic logic unit of Titan2 series products, which is mainly composed of multi-function LUT6, registers and extended function selectors. CLM has two forms of CLMA and CLMS in Titan2 series products. Both CLMA and CLMS support logic function, arithmetic function, shift register function and ROM function, only CLMS supports distributed RAM function.

The main functional features of CLM are as follows:

- Adopt innovative LUT6 logic structure
- Each CLM contains 4 multi-function LUT6
- Each CLM contains 8 registers
- Support arithmetic function mode

- Support fast arithmetic carry logic
- Efficient realization of multiplexing function
- Can realize ROM function
- Support distributed RAM mode
- Support cascading chain

For detailed CLM features and usage methods, please refer to " UG050001_Titan2 Series FPGA Configurable Logic Module (CLM) User Guide".

1.3.2. DRM

A single DRM has a 36Kb storage unit, supports multiple operating modes, supports configurable data bit width, and is stored in DP RAM. Dual-port mixed data width is supported in SDP RAM mode. The main features of DRM are as follows:

- DRM storage capacity can be independently configured with two 18Kb or one 36Kb.
- The port data bit width of DP RAM is as high as 36 bits, and its two ports are completely independent except for sharing RAM contents, and support different clock domains.
- The port data bit width of SDP RAM is as high as 72 bits, and its two ports also support different clock domains, but one of its ports is limited to write operations, and the other port is limited to read operations.
- In ROM mode, the content of DRM is usually initialized during the process of downloading configuration data. Of course, other modes can also utilize programming configuration to initialize the content of the DRM. The port data bit width of ROM is up to 72 bits.
- In synchronous or asynchronous FIFO mode, one port is dedicated to FIFO data writing, the other port is dedicated to FIFO data reading, and the read and write ports can use different clocks.
- Supports 64-bit ECC in 36K memory mode, and supports user insertion errors.

For detailed DRM features and usage methods, please refer to "UG050002_Titan2 Series FPGA Dedicated RAM Module (DRM) User Guide".

1.3.3. APM

Each APM consists of I/O Unit, Preadder, Mult and Postadder functional units, supporting each level of register pipeline. Each APM can implement one 25*18 -bit multiplier or two 12*9 - bit multipliers, support pre-add function, support signed operation; can realize one 48 - bit or two 24 - bit add / subtract / accumulate operations. The APM of the Titan2 FPGA supports cascading, enabling filter and high bit-width multiplier applications. The main features of APM are as follows:

- Signed multiplier 25*18 bits; unsigned multiplication is achieved by assigning 0 to the high bit
- All calculations and output results are signed numbers, including the sign bit
- Supports one 48-bit add/subtract/accumulate operation or two 24-bit operations
- Pre-add is 25 bits
- Independently selectable CE and RST
- Support input cascade
- Support output cascade
- Control/Data Signal Pipelining
- Support dynamic mode switching
- Support rounding function

For detailed APM features and usage methods, please refer to "UG050003_Titan2 Series FPGA Arithmetic Processing Module (APM) User Guide".

1.3.4. Input/Output

- IOB

The I/O of the Titan2 FPGA is distributed according to banks, and each bank is powered by an independent I/O power supply. There are two types of IOBs, namely HR IOB and HP IOB. HR IOB supports 1.2V~3.3V voltage range; HP IOB supports 1.2V~1.8V voltage range to adapt to different application scenarios. All user I/Os are bidirectional and include IBUF, OBUF, and tri-state control TBUF. Titan2 FPGA's IOB is powerful and can flexibly configure interface standards, output drive strength, slew rate, input hysteresis, etc. For detailed IO features and usage methods, please refer to "UG050006_Titan2 Series FPGA Input Output Interface (IO) User Guide".

- IOL

The IOL module is located between the IOB and the Core, and manages the signals to be input to and output from the FPGA Core.

IOL supports various high-speed interfaces. In addition to supporting data direct input and output and IO register input and output modes, it also supports the following functions:

- ISERDES: For high-speed interface, it supports input Deserializer of 1:2, 1:4, 1:7, 1:8, etc.
- OSERDES: For high-speed interfaces, it supports 2:1, 4:1, 7:1, 8:1 and other output Serializers.
- TSERDES: support 2:1; 4:1; 8:1
- Built-in IO delay function, you can adjust the input/output delay dynamically/statically.

For detailed IO features and usage methods, please refer to "UG050006_Titan2 Series FPGA Input Output Interface (IO) User Guide".".

1.3.5. ADC

Titan2 FPGA integrates a dual-core analog-to-digital converter (Dual core ADC) with a resolution of 12 bits and a sampling rate of 1 MSPS. Each ADC has 12 pairs of differential channels, of which 11 pairs of analog input pins are multiplexed with GPIO, and the other pair uses dedicated analog input pins. The scanning mode of the 12 pairs of channels is completely controlled by the FPGA flexibly, and the user can decide through the logic user to finally share the ADC sampling rate of 1MSPS by several pairs of channels.

The ADC provides on-chip voltage and temperature monitoring. VCC, VCCA, and VCC_DRM can be detected; see Table 6-1 for detailed characteristic parameters. For detailed use of ADC, please refer to "UG050009_Titan2 Series FPGA Analog-to-Digital Conversion Module (ADC) User Guide".

1.3.6. Clock

Titan2 series products include three types of clocks, namely Global Clock, Regional Clock and I/O Clock. The global clock provides the clock for the synchronous logic units of each node of the chip. The global clock can be used as a synchronous clock for synchronous logic units in different clock regions. Regional clocks provide clocks to synchronous logic cells within a single clock region to which they belong. Two clock regions adjacent to the top and bottom can be driven synchronously. The I/O Clock provides a synchronous clock for I/O high-speed data.

In order to meet the user's needs for frequency change and phase adjustment, Titan2 series products also provide a wealth of PLL resources, GPLL provides more frequency division and functions than PPLL, and PPLL can provide clock for DDR, etc. Taking PG2T390H as an example, the overall clock resources of the chip are as follows:

- There are 32 global clocks, of which 16 global clocks come from the clocks in the upper half of the chip, and the other 16 global clocks come from the clocks in the lower half of the chip. The 32 global clocks can be sent to each clock region;
- In addition to the 4 clock regions where HSST is located, each clock region has 4 regional clock buffers (RCKB, Region Clock Buffer), a total of 40 regional clocks;
- Each area has 12 horizontal clock buffers (HCKB, Horizontal Clock Buffer), a total of 168 horizontal clocks;
- Each IO BANK has 4 I/O clock buffers (IOCKB, IO Clock Buffer), a total of 40 I/O clocks.

For the detailed features and usage of the clock, please refer to "UG050004_Titan2 Series FPGA Clock Resources (Clock) User Guide".

1.3.7. Configuration

Configuration is the process of programming the FPGA. Titan2 FPGA uses SRAM cells to store configuration data, which needs to be reconfigured after each power-on; configuration data can be actively obtained by the chip from external flash, or downloaded to the chip through an external processor/controller.

Titan2 FPGA supports multiple configuration modes, including JTAG mode, Master SPI mode, Slave Parallel mode, and Slave Serial mode. The configuration-related functions of the Titan2 FPGA are described below:

- JTAG mode, compliant with IEEE 1149.1, IEEE 1149.6 standards
- Master SPI mode, support data bit width 1/2/4/8 bits
- Slave Parallel mode, support data bit width 8/16/32 bits
- Slave Serial Mode
- Support configuration data stream compression, which can effectively reduce the size of the bit stream, save storage space and programming time
- Configure data stream encryption to prevent malicious plagiarism and effectively protect customer design intellectual property
- Support SHA-3 digest, RSA-2048 authentication, AES256-GCM self-authentication to digitally sign bit stream
- The key storage method supports eFuse and battery-powered RAM (BB-RAM) key storage, where BB-RAM can provide chip-level security protection
- Support security protection technology to prevent reverse bit stream reading
- Support JTAG security management, can permanently disable the JTAG function
- Support anti-DPA attack to prevent the encryption key from being cracked by hackers
- Support SEU 1-bit error correction and 2-bit error detection, SEU is not 100% coverage, see "UG042001_SEU_IP" for specific coverage
- Support watchdog timeout detection function
- In main SPI mode, support configuration bit stream version fallback function

- Support UID function

For the power supply requirements, detailed features and usage methods in different configuration modes, please refer to "UG050005_Titan2 Series FPGA Configuration (Configuration) User Guide".

1.3.8. High Speed Serial Transceiver HSSTHP

HSSTHP is a high-speed serial interface module built into the Titan2 family of products with data rates up to 12.5Gbps. In addition to PMA, HSSTHP integrates rich PCS functions, which can be flexibly applied to various serial protocol standards. Each HSSTHP supports one to four full-duplex transceiver lanes. Key features of HSSTHP include:

- Supported data rate: 0.6Gbps-12.5Gbps
- Flexible reference clock selection
- The data rate of transmit channel and receive channel can be configured independently
- Programmable output swing and de-emphasis
- Receiver adaptive equalizer
- PMA Tx/Rx supports spread spectrum
- Data channel supports 8bit only, 10bit only, 8b10b 8bit, 16bit only, 20bit only, 8b10b 16bit, 32bit only, 40bit only, 8b10b 32bit, 64bit only, 80bit only, 8b10b 64bit, 64b66b/64b67b 16bit, 32b66b/64b67b 128b130b and other modes.
- Flexible configurable PCS, can support PCI Express GEN1/2/3, XAUI, Gigabit Ethernet, CPRI, SRIO and other protocols
- Flexible byte boundary alignment function
- Support Rx Clock Slip function to ensure fixed receive delay
- Support protocol standard 8b10b, 64b66b/64b67b, 128b130b encoding and decoding
- Flexible CTC solution
- Support x2 and x4 channel bonding
- The configuration of HSSTHP supports dynamic modification
- Near-end loopback and far-end loopback modes

- Built-in PRBS function

For detailed features and usage of HSSTHP, please refer to "UG050008_Titan2 Series FPGA High Speed Serial Transceiver (HSSTHP) User Guide"

1.4. Titan2 series FPGA reference materials

Section 1.3 briefly describes each module of Titan2 FPGA, as well as the clock and configuration system. For detailed information about the corresponding modules, please refer to the Titan2 FPGA-related user guide documents, as shown in the table below..

Table 1-3 Titan2 Series FPGA User Guide Documentation

Document number	File name	Document content
UG050001	Titan2 Series FPGA Configurable Logic Module (CLM) User Guide	Titan2 series FPGA configurable logic module function description
UG050002	Titan2 Series FPGA Dedicated RAM Module (DRM) User Guide	Titan2 series FPGA dedicated RAM module function description
UG050003	Titan2 Series FPGA Arithmetic Processing Module (APM) User's Guide	Titan2 series FPGA arithmetic processing module function description
UG050004	Titan2 Series FPGA Clock Resources (Clock) User Guide	Titan2 series FPGA clock resources, including PLL functions with usage description
UG050005	Titan2 Series FPGA Configuration (configuration) User Guide	Titan2 series FPGA configuration interface, configuration mode, configuration description of process etc.
UG050006	Titan2 Series FPGA Input Output Interface (IO) User Guide	Titan2 series FPGA input and output interface function description
UG050007	GTP User Guide for Titan2 Series Products	Titan2 series FPGA GTP function description and usage guide
UG050008	Titan2 Series FPGA High Speed Serial Transceiver (HSSTHP) User Guide	Titan2 Series FPGA High Speed Serial Transceivers (HSSTHP) function description
UG050009	Titan2 Series FPGA Analog-to-Digital Conversion Module (ADC) User Guide	Titan2 series FPGA analog-to-digital converter function description
UG050012	Titan2 Single Board Hardware Design Guide	Titan2 Single Board Hardware Design Guide

1.5. Titan2 Series FPGA Ordering Information

1-1 shows the content and meaning of the serial numbers of the Titan2 series FPGA product models.

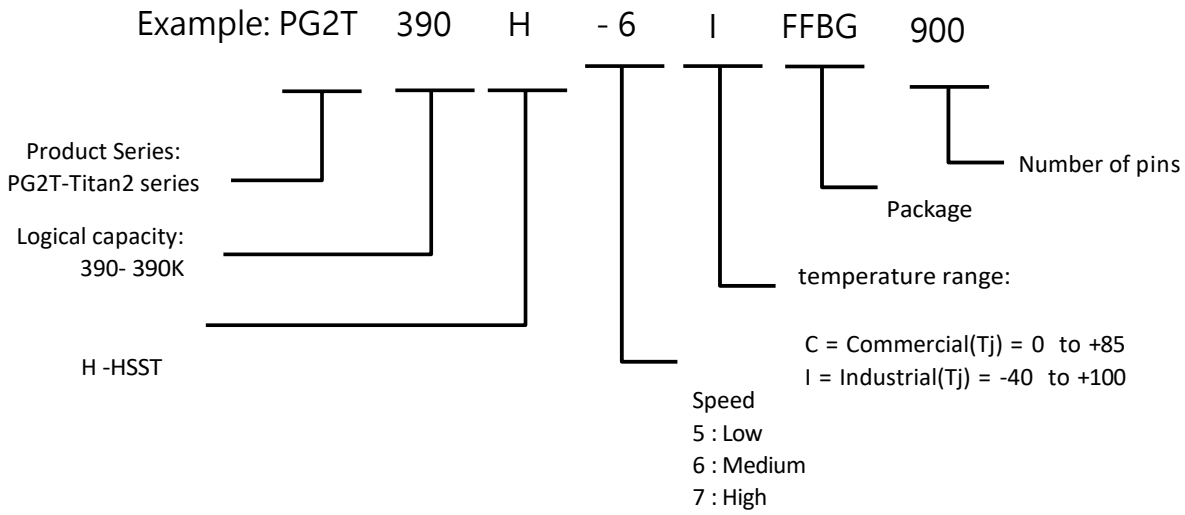

Figure 1-1 The content and meaning of the serial number of the Titan2 series FPGA product model

2. Working conditions

2.1. Device Absolute Limit Voltage

Table 2-1 Device Maximum Absolute Voltage Value

Name	Minimum	Maximum value	Unit	Description
VREF	- 0.5	2.0	V	Input reference voltage
VCCB	- 0.5	2.0	V	Key memory backup battery power supply voltage
VCC	- 0.5	1.1	V	Core logic power supply voltage
VCC_HP	- 0.5	1.1	V	HP IO logic power supply voltage
VCCA	- 0.5	2.0	V	Auxiliary power supply voltage
VCCIO	- 0.5	3.6	V	Supply voltage for output driver power supply (HR I/O)
	- 0.5	2.0	V	Supply voltage for output driver power supply (HP I/O)
VCC_DRM	- 0.5	1.1	V	DRM power supply voltage
VCCA_IO_G0	- 0.5	2.06	V	HP IO dedicated analog power supply
VIN	- 0.3	VCCIO+0.45	V	I/O input voltage
	- 0.3	2.525	V	VCCIO is 3.3V , VREF or differential I/O standard I/O input voltage, except TMDS_33 standard

Note: Exceeding the above limit ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

2.2. Device Recommended Operating Conditions

Table 2-2 Recommended working conditions

Name	Minimum	Typical value	Maximum value	Unit	Description
V_{CCB}	1.0	- -	1.89	V	Key memory backup battery power supply voltage
V_{CC} (1)	0.97	1.0	1.03	V	Core supply voltage
V_{CC_HP} (1)	0.97	1.0	1.03	V	HP IO supply voltage
V_{CCA} (2)	1.71	1.8	1.89	V	Auxiliary power supply voltage
V_{CCIO}	1.14	- -	3.465	V	Supply voltage for output driver power supply (HR I/O)
	1.14	- -	1.89	V	Supply voltage for output driver power supply (HP I/O)
V_{CC_DRM} (1)	0.97	1.0	1.03	V	DRM power supply voltage
$V_{CCA\_IO\_G0}$ (2)	1.71	1.8	1.89	V	HP IO Dedicated analog power supply (when voltage is set to 1.8V)
	1.94	2.0	2.06	V	HP IO Dedicated analog power supply (when voltage is set to 2.0V)
	- 0.2	- -	V_{CCIO} +0.2	V	I/O Input voltage

V_{IN}	- 0.2	- -	2.5	V	When V_{CCIO} is 3.3V, V_{REF} or I/O input voltage of differential I/O standard, except TMDS_33 standard
I_{IN}	- -	- -	10	mA	The maximum current allowed to flow through the forward-biased clamp diode of any PIN in a powered or unpowered Bank

Notes: 1. V_{CC}/V_{CC_HP} and V_{CC_DRM} can be connected to the same 1.0V power supply at the board level .

2. V_{CCA} and $V_{CCA\_IO\_G0}$ can be connected to the same 1.8V power supply at the board level .

3. All voltages are relative to ground.

4. For power-related design, please refer to " UG050012_Titan2 Board Hardware Design Guide".

5. V_{CCIO} voltage V_{CC} should be within 1.2V , 1.35V , 1.5V , 1.8V , 2.5V and 3.3V and ± 5% of each voltage, where 2.5V and 3.3V HR only I/O support.

6. V_{CCB} is only used when the bitstream is encrypted, and V_{CCB} is grounded or V_{CCA} when the key function is not used .

2.3. DC Characteristics at Recommended Device Operating Conditions

Table 2- 3 DC characteristics under recommended operating conditions

Name	Min	Typical (1)	Max	Description
V_{DRVCC}	0.75V	- -	- -	V_{CC} The configuration data hold voltage
V_{DRVCCA}	1.5V	- -	- -	V_{CCA} The configuration data hold voltage
I_L	- -	- -	60uA	pin input or output leakage current
I_{REF}	- -	- -	60uA	VREF _ pin leakage current
I_{PU}[2]	90uA	- -	390uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=3.3V)
	68uA	- -	370uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=2.5V)
	34uA	- -	300uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=1.8V)
	23uA	- -	200uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=1.5V)
	12uA	- -	150uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=1.2V)
I_{PD}	68uA	- -	330uA	PAD pull-down current (V_{IN}=3.3V)
	45uA	- -	300uA	PAD pull-down current (V_{IN}=1.8V)
I_{CCADC}	- -	- -	25mA	ADC power up mode current
I_{VCCB} (3)	- -	- -	150nA	V_{CCB} supply current
R_{INTERM}	22	40	65	Thevenin equivalent resistance of the programmable input terminal at VCCIO/2 voltage. (when set to 40Ω)
	28	50	75	Thevenin equivalent resistance of the programmable input terminal at VCCIO/2 voltage. (when set to 50Ω)
	35	60	95	Thevenin equivalent resistance of the programmable input terminal at VCCIO/2 voltage. (when set to 60Ω)
C_{IN} (4)	- -	- -	16pF	Package Pin Input Capacitance
n	- -	0.9988	- -	Ideality Factor for Temperature Diodes
r	- -	2.5Ω	- -	Serial Resistance of Temperature Diodes

Notes: 1. Typical values refer to atmospheric pressure, 25 ℃

2. Three temperature positive and negative bias 3%

3. maximum value here refers to the maximum value at 25 ℃.

4. The capacitance value refers to the capacitance value of the die and the package

2.4. Maximum allowable overshoot and undershoot voltage at V_{IN}

Table 2-4 HR I/O Maximum allowable overshoot and undershoot voltage at V_{IN}

Overshoot Voltage（V）	%UI (-40 ℃ ~100 ℃)	Undershoot Voltage（V）	%UI (-40 ℃ ~100 ℃)
V_{CCIO} + 0.45	100	- 0.30	100
		- 0.35	55.50
		- 0.40	23.20
		- 0.45	9.90
V_{CCIO} + 0.5	42	- 0.50	4.30
V_{CCIO} + 0.55	19.08	- 0.55	1.89
V_{CCIO} + 0.6	8.77	- 0.60	0.84
V_{CCIO} + 0.65	4.10	- 0.65	0.38
V_{CCIO} + 0.7	1.90	- 0.70	0.18
V_{CCIO} + 0.75	0.91	- 0.75	0.08
V_{CCIO} + 0.80	0.44	- 0.80	0.04
V_{CCIO} + 0.85	0.21	- 0.85	0.01

Notes: 1. The maximum current per bank does not exceed 200mA .

2. Overshoot or undershoot peak voltage, and at Vcco + 0.20 v above or gnd-0.20 v The following durations shall not exceed the values in this table.

Table 2- 5 HP I/O Maximum allowable overshoot and undershoot voltage at VIN

Overshoot Voltage (V)	%UI (-40 ℃ ~100 ℃)	Undershoot Voltage (V)	%UI (-40 ℃ ~100 ℃)
V_{CCIO} + 0.45	100	- 0.45	100
V_{CCIO} + 0.50	64.35	- 0.50	67.96
V_{CCIO} + 0.55	44.69	- 0.55	41.69
V_{CCIO} + 0.60	33.02	- 0.60	26.05
V_{CCIO} + 0.65	25.28	- 0.65	14.92
V_{CCIO} + 0.70	19.49	- 0.70	7.56
V_{CCIO} + 0.75	14.47	- 0.75	3.74
V_{CCIO} + 0.80	10.42	- 0.80	2.34
V_{CCIO} + 0.85	7.71	- 0.85	1.67
V_{CCIO} + 0.90	5.85	- 0.90	1.29
V_{CCIO} + 0.95	4.58	- 0.95	1.04

Notes: 1. The maximum current per bank does not exceed 200mA .

2. Overshoot or undershoot peak voltage, and at Vcco + 0.20 v or gnd-0.20 v The following durations shall not exceed the values in this table.

2.5. Quiescent Current

Table 2-6 Quiescent Current

Symbol	Device	Typical value (1)	Max (2)	Description
$I_{CCQ\_}$	PG2T390H	1665mA	4A	V_{CC} quiescent current
$I_{CC\_DRMQ\_}$	PG2T390H	30mA	75mA	V_{CC_DRM} quiescent current
I_{CCIOQ}	PG2T390H	40mA	50mA	V_{CCIO} quiescent current
I_{CCAQ}	PG2T390H	375mA	1.5A	V_{CCA} quiescent current
$I_{CCA\_IOQ\_}$	PG2T390H	1mA	2mA	$V_{CCA\_IO\_G0}$ quiescent current

Notes: 1. Typical values refer to constant voltage, 85 °C junction temperature and all single-ended I/Os ; devices in blank configuration with no output current load, no input pull-up resistors, all I/Os in tri-state and floating condition The current value obtained from the test below.

2. Maximum value refers to normal voltage, junction temperature of 100 degrees and all single-ended I/O ; the device in blank configuration and no output current load, no input pull-up resistor, all I/Os are in tri-state and the current value obtained by the floating test .

3. For static power evaluation under other specific conditions, please use the power evaluation tool integrated in the MCT.

2.6. Power up ramp-up time

Table 2-7 Power up ramp-up time

Symbol	Minimum	Maximum value	Unit	Description
T_{VCC}	0.2	50	ms	V_{CC} from GND Rise to 90% V_{CC} time
T_{VCC_DRM}	0.2	50	ms	V_{CC_DRM} from GND Rise to 90% V_{CC_DRM} time
T_{VCCIO}	0.2	50	ms	V_{CCIO} from GND Rise to 90% V_{CCIO} time
T_{VCCA}	0.2	50	ms	V_{CCA} from GND Rise to 90% V_{CCA} time
$T_{VCCIO2VCCA}$	-	100	ms	V_{CCIO} - V_{CCA} >2V time
$T_{HSSTAVCC}$	0.2	50	ms	HSSTAVCC from GND Rise to 90%HSSTAVCC time
$T_{HSSTAVCCPLL}$	0.2	50	ms	HSSTAVCCPLL from GND up to 90%HSSTAVCCPLL time
$T_{HSSTVCCA}$	0.2	50	ms	HSSTVCCA from GND Rise to 90%HSSTVCCA time

2.7. Minimum current required to start

Table 2-8 Minimum current required to start

Symbol	Device	Minimum	Unit	Description
I_{CCMIN}	PG2T390H	I_{CCQ} +1000	mA	V_{CC} Minimum current for power-up
I_{CC_DRMMIN}	PG2T390H	I_{CC_DRMQ} +50	mA	V_{CC_DRM} Minimum current for power-up
$I_{CCIOMIN}$	PG2T390H	I_{CCIOQ} +50	mA	V_{CCIO} Minimum current at power-up (per bank)
I_{CCAMIN}	PG2T390H	I_{CCAQ} +80 _	mA	V_{CCA} Minimum current for power-up

2.8. ESD（HBM , CDM）, Latch Up indicator

Table 2-9 ESD , Latch-Up indicators

Symbol	Value	Unit	Description
HBM_IO	±900	V	All I/O and power IO except configuration power IO (VCCIO_CFG) and configuration dedicated input I/O
HBM_CFG	±400	V	Configure the power supply V_{CCIO_CFG} and configure dedicated inputs I/O
CDM_IO	±300	V	All I/O except HSST dedicated IO
CDM_SERDES	±200	V	HSST Dedicated IO
Latch- up	±100	mA	Current injection method

For detailed I/O classification, please refer to "PK05001_PG2T390H_FFBG900"

2.9. eFUSE programming conditions

Table 2-10 eFUSE programming conditions

Symbol	Minimum	Maximum value	Unit	Description
I_{eFUSE}		188	mA	eFUSE V_{CCA} required for programming current
T_j	15	100	° C	

3. DC characteristics under typical operating conditions

3.2. Power on and power off

3.2.1. Power-on and power-off requirements

(1) V_{CC} must precede V_{CCA} at power-on, V_{CCA} is not allowed to precede V_{CC}, and V_{CC} is not earlier than V_{CCA} at power-off.

(2) When V_{CCIO} is powered on before V_{CCA} or V_{CCA} is powered off before V_{CCIO}, the duration of (V_{CCIO}-V_{CCA})>2V must be less than 100 milliseconds.

Note: It is forbidden to power on V_{CCIO} and V_{CCA} when V_{CC} is not powered on, and it is prohibited that V_{CCIO} and V_{CCA} are powered on after V_{CC} is powered off, otherwise the device may be damaged.

3.2.2. Logic power-on and power-off sequence

(1) The power-up sequence to ensure that the I/Os are tri-stated during power-up while reaching the minimum power-up current:

V_{CC}/V_{CC_HP}, V_{CC_DRM}, V_{CCA}/$V_{CCA\_IO\_G0}$, V_{CCIO}.

(2) The recommended power-off sequence is the reverse of the power-on sequence.

(3) The recommended power-on sequence is shown in Figure 3-1. According to the power-on sequence of (1), each power supply voltage must satisfy VCC/VCC_HP ≥ VCC_DRM ≥ VCCA/VCCA_IO_G0 ≥ VCCIO before reaching the typical voltage value.

(4) The recommended power-off sequence is shown in Figure 3-2. According to the power-off sequence

of (2), each power supply voltage must meet the requirements before power-off to zero voltage.

$V_{CCIO} \leq V_{CCA}/V_{CCA\_IO\_G0} \leq V_{CC\_DRM} \leq V_{CC}/V_{CC\_HP}$.

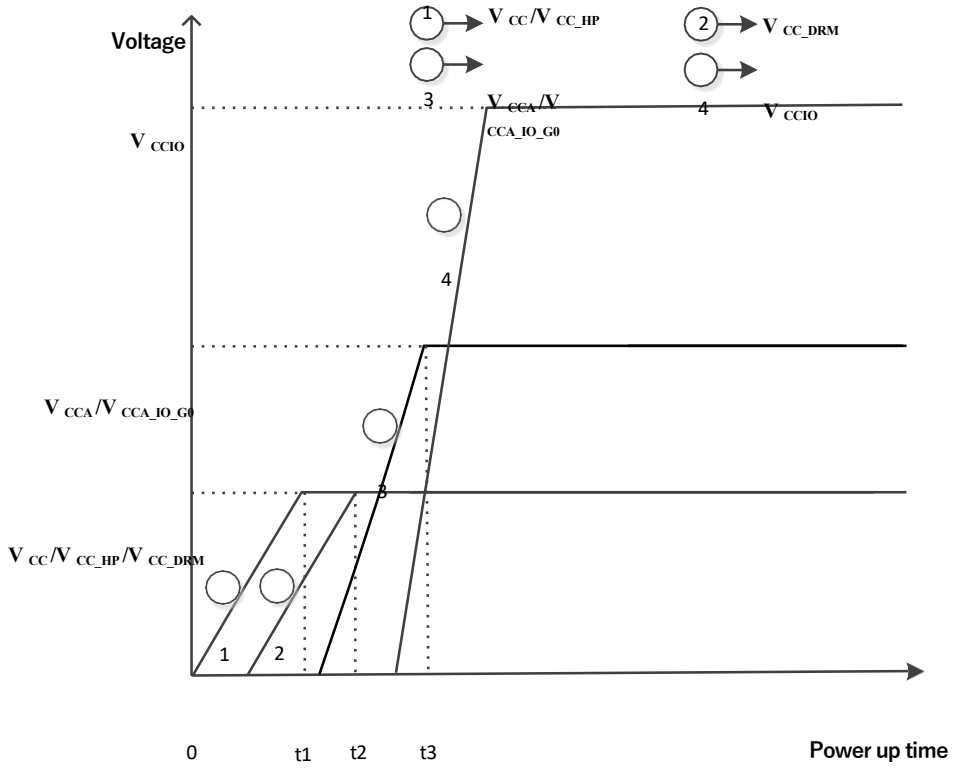

Figure 3-1 Power-on sequence diagram

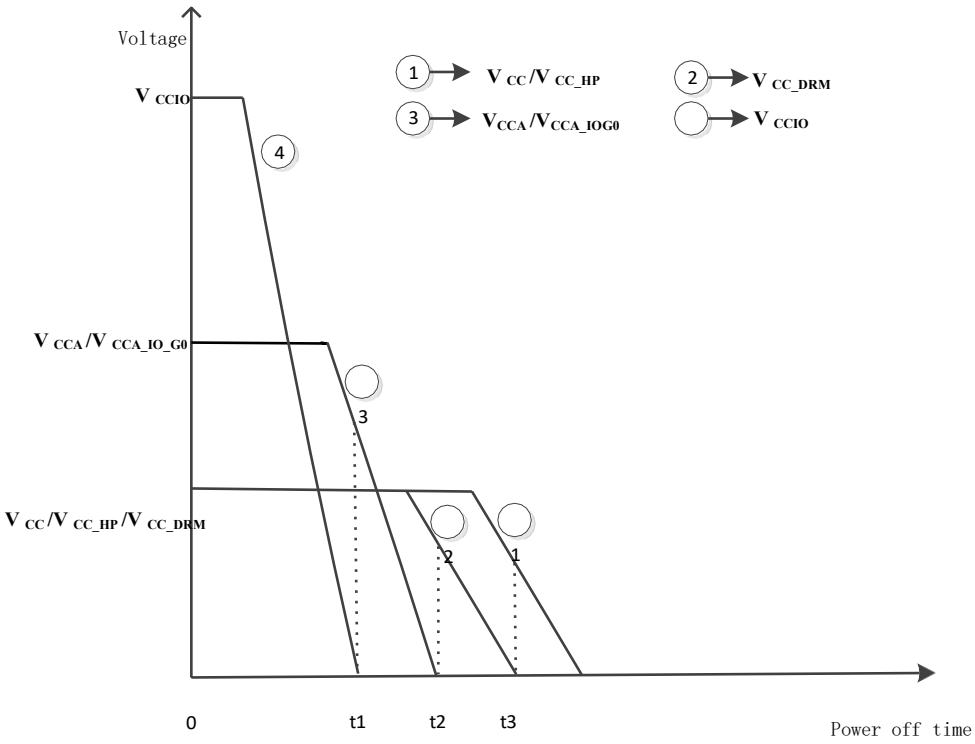

Figure 3-2 Power-off timing diagram

3.2.3. HSST power supply power-on and power-off sequence

After the initialization is completed (after the INIT_FLAG_N signal is pulled high), then power on the HSST. The recommended power-on sequence is shown in Figure 3-3 .

Ensure the minimum current during the power-on process; if the recommended power-on sequence is not followed, HSSTAVCC may have a maximum current of 1200mA before the INIT_FLAG_N signal is pulled high.

Figure 3-3 HSST power-up sequence

3.2.4. Overall power-on and power-off sequence

（1） It is recommended that the overall power-on sequence be logically powered on first (see Fig. 3-1) Power on the HSST power supply (see Figure 3-3 for details) .

（2） The recommended power-off sequence is the opposite of the recommended power-on sequence. Simultaneous power-off can be supported, but the hot-plug function is not guaranteed.

3.2.5. Power-on and power-off requirements that support hot swap

(1) Hot Swap Specifications

Table 3-1 Hot Swap Specifications

Symbol	Parameter Description	Maximum value
$I_{DK\_(DC)}$	DC Current , per I/O	1mA
$I_{DK\_(AC)}$	AC Current , per I/O	1mA

(2) 3.1.2 Power-on and power-off requirements must be met.

(3) The value of the pull-up resistor in the I2C bus usage scenario should be 1K~2K .

(4) BANK HR of L1 , L2 , L3 , L6 , L7 I/O supports hot-plugging, other IOs do not support hot-plugging.

(5) For the specific hot-plug situation, see the hot-plug report.

3.2. IO input and output DC characteristics (I/O Input & Output DC)

3.2.1. HR I/O DC Characteristics

HR BANK single-ended I/O level standard input and output voltage ranges are as follows

Table 3-2 HR BANK single-ended IO level standard input and output voltage range

Standard	V_{IL} (1)		V_{IH} (2)		V_{OL} (3) Max (v)	VOH (4) _ Min (v)	IOL _ (mA)	I_{OH} (mA)
	Min(v)	Max(v)	Min(v)	Max(v)				
PCI33	- 0.3	0.3V CCIO	0. 5V CCIO	V CCIO +0.5	0.1V CCIO	0.9V CCIO	1.5	- 0.5
LVCMOS33	- 0.3	0.8	2.0	3.465	0.4	V CCIO - 0.4	4 8 12 16	- 4 - 8 - 12 - 16
LVTTL33	- 0.3	0.8	2.0	3.465	0.4	2.4	4 8 12 16 twen ty four	- 4 - 8 - 12 - 16 - 24
LVCMOS25	- 0.3	0.7	1.7	V CCIO +0.3	0.4	V CCIO - 0.4	4 8 12 16	- 4 - 8 - 12 - 16
LVCMOS18	- 0.3	0.35V CCIO	0.65V CCIO	V CCIO +0.3	0.45	V CCIO - 0.45	4 8 12 16 twen ty four	- 4 - 8 - 12 - 16 - 24
LVCMOS15	- 0.3	0.35V CCIO	0.65V CCIO	V CCIO +0.3	0.4	V CCIO - 0.4	4 8 12 16	- 4 - 8 12 16
LVCMOS12	- 0.3	0.35V CCIO	0.65V CCIO	V CCIO +0.3	0.4	V CCIO - 0.4	4 8 12	- 4 - 8 - 12
SSTL18_I	- 0.3	Vref -	Vref+0.125	V CCIO	0.5V CCIO - 0.47	0.5V CCIO +0.47	8	- 8

		0.125		+0.3				
SSTL18_II	- 0.3	Vref - 0.125	Vref+0.125	V_{CCIO} +0.3	0.5V_{CCIO} - 0.6	0.5V_{CCIO} +0.6	13.4	- 13.4
SSTL15_I	- 0.3	Vref- 0.10	Vref+0.10	V_{CCIO} +0.3	0.5V_{CCIO} - 0.175	0.5V_{CCIO} +0.175	8.9	- 8.9
SSTL15_II	- 0.3	Vref- 0.10	Vref+0.10	V_{CCIO} +0.3	0.5V_{CCIO} - 0.175	0.5V_{CCIO} +0.175	13	- 13
HSUL12	- 0.3	Vref- 0.13	Vref+0.13	V_{CCIO} +0.3	0.2V_{CCIO}	0.8V_{CCIO}	0.1	- 0.1
HSTL18_I	- 0.3	Vref- 0.1	Vref+0.1	V_{CCIO} +0.3	0.40	V_{CCIO} - 0.40	8	- 8
HSTL18_II	- 0.3	Vref- 0.1	Vref+0.1	V_{CCIO} +0.3	0.40	V_{CCIO} - 0.40	16	- 16
HSTL15_I	- 0.3	Vref- 0.1	Vref+0.1	V_{CCIO} +0.3	0.40	V_{CCIO} - 0.40	8	- 8
HSTL15_II	- 0.3	Vref- 0.1	Vref+0.1	V_{CCIO} +0.3	0.40	V_{CCIO} - 0.40	16	- 16
SSTL135_I	- 0.3	Vref- 0.1	Vref+0.1	V_{CCIO} +0.3	0.5V_{CCIO} - 0.15	0.5V_{CCIO} +0.15	8.9	- 8.9
SSTL135_II	- 0.3	Vref- 0.1	Vref+0.1	V_{CCIO} +0.3	0.5V_{CCIO} - 0.15	0.5V_{CCIO} +0.15	13	- 13
LPDDR	- 0.3	0.2V_{CCIO}	0.8V_{CCIO}	V_{CCIO} +0.3	0.1V_{CCIO}	0.9V_{CCIO}	0.1	- 0.1

Notes: 1. V_{IL} is the input voltage that is single-ended and recognized as a low level.

2. V_{IH} is the input voltage that is single-ended and recognized as a high level .

3. V_{OL} is the voltage of the single-ended low-level output.

4. V_{OH} is the voltage of the single-ended high-level output.

The standard input and output voltage ranges of differential I/O levels are as follows:

Table 3-3 Parameter requirements of HR BANK differential input and output standards

I/O Standard	Vicm (1) (V)			Vid (2) (V)			Vocm (3) (V)			Vod (4) (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVDS	1.0	1.2	1.425	0.1	0.35	0.6	1	1.25	1.425	0.25	0.35	0.6
BLVDS	0.3	1.2	1.425	0.1	–	–	–	1.25	–	–		
MINI_LVDS	0.3	1.2	$V_{CCA\_IO\_G0}$	0.2	0.4	0.6	1	1.2	1.4	0.3	0.40	0.6
PPDS	0.2	0.9	$V_{CCA\_IO\_G0}$	0.1	0.25	0.4	0.5	1.0	1.4	0.1	0.3	0.45
RSDS	0.3	0.9	1.5	0.1	0.35	0.6	1	1.2	1.4	0.1	0.35	0.6
TMDS	2.7	2.965	3.23	0.15	0.675	1.2	V_{CCIO} - 0.405	V_{CCIO} - 0.3	V_{CCIO} - 0.19	0.4	0.6	0.8

Notes: 1. Vicm is the input common mode voltage.

2. Vid is the input differential mode voltage.

3. Vocm is the output common mode voltage.

4. Vod is the output differential mode voltage.

Table 3-4 Parameter requirements for HR BANK differential input and output standards

I/O standard	Vid(V)	Vicm（V）			V_{OL} (V)	V_{OH} (V)	IOL_（mA）	I_{OH}（mA）
	min	min	typ	max	max	min	max	min
HSUL12D	0.1	0.3	0.6	0.85	0.2V_{CCIO}	0.8V_{CCIO}	0.1	- 0.1
SSTL135D_I	0.1	0.3	0.675	1	0.5V_{CCIO} - 0.15	0.5V_{CCIO} +0.15	8.9	- 8.9
SSTL135D_II	0.1	0.3	0.675	1	0.5V_{CCIO} - 0.15	0.5V_{CCIO} +0.15	13	- 13
HSTL15D_I	0.1	0.3	0.75	1.125	0.4	V_{CCIO} - 0.4	8	- 8
HSTL15D_II	0.1	0.3	0.75	1.125	0.4	V_{CCIO} - 0.4	16	- 16
HSTL18D_I	0.1	0.3	0.9	1.425	0.4	V_{CCIO} - 0.4	8	- 8
HSTL18D_II	0.1	0.3	0.9	1.425	0.4	V_{CCIO} - 0.4	16	- 16
LPDDRD	0.1	0.3	0.9	1.425	0.1V_{CCIO}	0.9V_{CCIO}	0.1	- 0.1
SSTL15D_I	0.1	0.3	0.75	1.125	0.5V_{CCIO} - 0.175	0.5V_{CCIO} +0.175	0.89	-0.89
SSTL15D_II	0.1	0.3	0.75	1.125	0.5V_{CCIO} - 0.175	0.5V_{CCIO} +0.175	13	- 13
SSTL18D_I	0.1	0.3	0.9	1.425	0.5V_{CCIO} - 0.47	0.5V_{CCIO} +0.47	8	- 8
SSTL18D_II	0.1	0.3	0.9	1.425	0.5V_{CCIO} - 0.6	0.5V_{CCIO} +0.6	13.4	-13.4

3.2.2. HP I/O DC Characteristics

HP BANK single-ended I/O level standard input and output voltage ranges are as follows

Table 3- 5 HP BANK single-ended IO level standard input and output voltage range

Standard	V_{IL}		V_{IH}		V_{OL} Max (v)	V_{OH} Min (v)	I_{OL}_ (mA)	I_{OH} (mA)
	Min (v)	Max (v)	Min (v)	Max (v)				
LVCMOS18	- 0.3	0.35V_{CCIO}	0.65V_{CCIO}	V_{CCIO} +0.3	0.45	V_{CCIO} - 0.45	2 4 6 8 12 16	- 2 - 4 - 6 - 8 - 12 - 16
LVCMOS15	- 0.3	0.35V_{CCIO}	0.65V_{CCIO}	V_{CCIO} +0.3	0.4	V_{CCIO} - 0.4	2 4 6	- 2 - 4 - 6

standard	VIL		VIH		VOL _ Max (v)	VOH _ Min (v)	IOL _ (mA)	IOH (mA)
	Min (v)	Max (v)	Min (v)	Max (v)				
							8 12 16	- 8 - 12 - 16
LVCMOS12	- 0.3	0.35V CCIO	0.65V CCIO	V CCIO +0.3	0.4	V CCIO - 0.4	2 4 6 8	- 2 - 4 - 6 - 8
SSTL18_I	- 0.3	Vref - 0.125	Vref+0.125	V CCIO +0.3	0.5V CCIO - 0.47	0.5V CCIO +0.47	8	- 8
SSTL18_II	- 0.3	Vref - 0.125	Vref+0.125	V CCIO +0.3	0.5V CCIO - 0.55	0.5V CCIO +0.55	13.4	- 13.4
SSTL15_I	- 0.3	Vref- 0.10	Vref+0.10	V CCIO +0.3	0.5V CCIO - 0.175	0.5V CCIO +0.175	8.9	- 8.9
SSTL15_II	- 0.3	Vref- 0.10	Vref+0.10	V CCIO +0.3	0.5V CCIO - 0.175	0.5V CCIO +0.175	13	- 13
HSUL12	- 0.3	Vref- 0.13	Vref+0.13	V CCIO +0.3	0.2V CCIO	0.8V CCIO	0.1	- 0.1
HSTL18_I	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	0. 40	V CCIO - 0.40	8	- 8
HSTL18_II	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	0. 40	V CCIO - 0.40	16	- 16
HSTL15_I	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	0. 40	V CCIO - 0.40	8	- 8
HSTL15_II	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	0. 40	V CCIO - 0.40	16	- 16
SSTL135_I	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	0.5V CCIO - 0.15	0.5V CCIO +0.15	8.9	- 8.9
SSTL135_II	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	0.5V CCIO - 0.15	0.5V CCIO +0.15	13	- 13
POD12	- 0.3	Vref - 0.068	Vref+0.068	V CCIO +0.3	/	/	/	/
SSTL12	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	0.5V CCIO - 0.15	0.5V CCIO +0.15	14.25	- 14.25
HSTL_I_12	- 0.3	Vref- 0.1	Vref+0.1	V CCIO +0.3	25% V CCIO	75% V CCIO	6.3	- 6.3

HP BANK differential I/O level standard input and output voltage range is as follows

Table 3- 6 HP BANK Parameter requirements for differential input and output standards

I/O Standard	Vicm(V)			Vid(V)			Vocm(V)			Vod(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVDS	1.0	1.2	1.425	0.10	0.35	0.6	1.0	1.18	1.425	0.25	0.35	0.60

Table 3-7 HP Parameter requirements for BANK class differential input and output standards

IO standard	Vid(V)	Vicm（V）			VOL (V)	VOH (V)	IOL _ （mA）	IOH （mA）
	min	min	typ	max	max	min	max	min
HSUL12D	0.1	0.3	0.6	0.85	0.2V CCIO	0.8V CCIO	0.1	- 0.1
SSTL135D_I	0.1	0.3	0.675	1	0.5V CCIO - 0.15	0.5V CCIO +0.15	8.9	- 8.9
SSTL135D_II	0.1	0.3	0.675	1	0.5V CCIO - 0.15	0.5V CCIO +0.15	13	- 13
HSTL15D_I	0.1	0.3	0.75	1.125	0.4	V CCIO - 0.4	8	- 8
HSTL15D_II	0.1	0.3	0.75	1.125	0.4	V CCIO - 0.4	16	- 16
HSTL18D_I	0.1	0.3	0.9	1.425	0.4	V CCIO - 0.4	8	- 8
HSTL18D_II	0.1	0.3	0.9	1.425	0.4	V CCIO - 0.4	16	- 16
SSTL15D_I	0.1	0.3	0.75	1.125	0.5V CCIO - 0.175	0.5V CCIO +0.175	0.89	-0.89
SSTL15D_II	0.1	0.3	0.75	1.125	0.5V CCIO - 0.175	0.5V CCIO +0.175	13	- 13
SSTL18D_I	0.1	0.3	0.9	1.425	0.5V CCIO - 0.47	V CCIO +0.47	8	- 8
SSTL18D_II	0.1	0.3	0.9	1.425	0.5V CCIO - 0.6	V CCIO +0.6	13.4	-13.4

POD12D	0.16	0.76	0.84	0.92	/	/	/	/
SSTL12D	0.1	0.3	0.6	0.85	$0.5V_{CCIO}$ - 0.15	$0.5V_{CCIO}$ +0.15	14.25	- 14.25

4. AC Characteristics under Typical Operating Conditions

This chapter mainly lists the AC characteristics of each logic unit of the FPGA under typical operating conditions.

4.1. Configurable logic module CLM (Configurable Logic Module) AC characteristic parameters

Table 4- 1 CLM AC Characteristics

Name	Delay time			Unit	Description
	- 5	- 6	- 7		
logic delay					
Titoy6	TBD	0.216	TBD	ns,max	LUT6 Input Ax/Bx/Cx/Dx to Y0/Y1/Y2/Y3 delay
Titoy7	TBD	0.436	TBD	ns,max	LUT6 Input Ax/Bx/Cx/Dx to CR0/CR1 delay (LUT7)
Titoy8	TBD	0.367	TBD	ns,max	LUT6 Input Ax/Bx/Cx/Dx to CR2 delay to Y1 (LUT8)
Titoya	TBD	0.321	TBD	ns,max	LUTs input Ax Delay to CYA(CR0)
Titoyb	TBD	0.403	TBD	ns,max	LUTs input Bx Delay to CYB(CR1)
Titoyc	TBD	0.326	TBD	ns,max	LUTs input Cx Delay to CYC (CR2)
Titoyd	TBD	0.386	TBD	ns,max	LUTs input Dx Delay to CYD(CR3)
Tcintocout	TBD	0.092	TBD	ns,max	CIN input to COUT delay
Timing parameters					
Tco	TBD	0.198	TBD	ns,max	CLK Input relative to Q0/Q1/Q2/Q3 TCO _
Tctocr	TBD	0.218	TBD	ns,max	CLK Input relative to CR0/CR1/CR2/CR3 TCO _
Tsu/Thd	TBD	- 0.245/0.269	TBD	ns,min	Ax/Bx/Cx/Dx relative to DFF setup /hold
Tmck	TBD	- 0.245/0.269	TBD	ns,min	M relative to DFF setup /hold
Tceck	TBD	0.231/-0.066	TBD	ns,min	CE relative to DFF setup /hold
Trsck	TBD	0.231/-0.065	TBD	ns,min	RS relative to DFF setup /hold
Distributed RAM Timing parameters					
Tramck2y	TBD	0.430	TBD	ns,max	CLK -> Y0/Y1/Y2/Y3 mem read delay
Tramck2cr	TBD	0.534	TBD	ns,max	CLK -> CR0/CR1/CR2/CR3 mem read delay
Twe2ck	TBD	- 0.245/0.269	TBD	ns,min	CLK -> WE timing check, setup/hold
Tadr2ck	TBD	- 0.245/0.269	TBD	ns,min	CLK -> An address timing check, setup/hold
Twd2ck	TBD	- 0.245/0.269	TBD	ns,min	CLK -> AD/BD/CD/DD data timing check,setup/hold

Note: The timing parameters of specific usage scenarios are subject to the software timing report

4.2. Dedicated RAM module DRM (Dedicated RAM Module) AC characteristic parameters

Table 4-2 DRM Communication Features

Category	Numerical value			Unit	AC characteristic parameter description
	- 5	- 6	- 7		
T_{co_18K}	TBD	1.426	TBD	ns,max	CLKA/CLKB->QA/QB (output register disabled, 18K mode)
$T_{co\_18K\_reg}$	TBD	0.553	TBD	ns,max	CLKA/CLKB->QA/QB (output register enabled, 18K mode)

T_{co_36K}	TBD	1.426	TBD	ns,max	CLKA/CLKB->QA/QB (output register disabled, 36K mode)
$T_{co\_36K\_reg}$	TBD	0.553	TBD	ns,max	CLKA/CLKB->QA/QB (output register enabled, 36K mode)
T_{co_ecc}	TBD	1.585	TBD	ns,max	CLKB->QA/QB (output register disabled, ECC mode)
$T_{co\_ecc\_reg}$	TBD	0.652	TBD	ns,max	CLKB->QA/QB (output register enabled, ECC mode)
$T_{co\_ecc\_err}$	TBD	0.562	TBD	ns,max	CLKB->ECC_S/DBITERR (output register enabled, ECC mode)
$T_{co\_flag\_full}$	TBD	0.493	TBD	ns,max	CLKA->FULL(ALMOST_FULL) (18K/36K FIFO mode)
$T_{co\_flag\_empty}$	TBD	0.509	TBD	ns,max	CLKB->EMPTY(ALMOST_EMPTY) (18K/36K FIFO mode)
$T_{co\_ecc\_parity}$	TBD	0.542	TBD	ns,max	CLKA->ECC_PARITY (ECC encoding mode)
$T_{co\_ecc\_rdaddr}$	TBD	0.570	TBD	ns,max	CLKA->ECC_RDADDR (output register disabled, ECC mode)
$T_{co\_ecc\_rdaddr\_reg}$	TBD	0.597	TBD	ns,max	CLKA->ECC_RDADDR (output register enabled, ECC mode)
$T_{su\_18K\_ad}$ / $T_{hd\_18K\_ad}$	TBD	0.149/0.217	TBD	ns,min	Address input Setup/Hold time (18K mode)
$T_{su\_18K\_d}$ / $T_{hd\_18K\_d}$	TBD	0.184/0.1	TBD	ns,min	Data input Setup/Hold time (18K mode)
$T_{su\_18K\_ce}$ / $T_{hd\_18K\_ce}$	TBD	0.176/0.081	TBD	ns,min	CE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_we}$ / $T_{hd\_18K\_we}$	TBD	0.079/0.108	TBD	ns,min	WE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_be}$ / $T_{hd\_18K\_be}$	TBD	0.027/0.066	TBD	ns,min	BE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_oe}$ / $T_{hd\_18K\_oe}$	TBD	0.046/0.163	TBD	ns,min	OCE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_rst}$ / $T_{hd\_18K\_rst}$	TBD	0.027/0.170	TBD	ns,min	Synchronous reset input Setup/Hold time (18K mode)
$T_{su\_36K\_ad}$ / $T_{hd\_36K\_ad}$	TBD	0.127/0.217	TBD	ns,min	Address input Setup/Hold time (36K mode)
$T_{su\_36K\_d}$ / $T_{hd\_36K\_d}$	TBD	0.184/0.11	TBD	ns,min	Data input Setup/Hold time (36K mode)
$T_{su\_36K\_ce}$ / $T_{hd\_36K\_ce}$	TBD	0.147/0.081	TBD	ns,min	CE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_we}$ / $T_{hd\_36K\_we}$	TBD	0.027/0.108	TBD	ns,min	WE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_be}$ / $T_{hd\_36K\_be}$	TBD	0.082/0.066	TBD	ns,min	BWE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_oe}$ / $T_{hd\_36K\_oe}$	TBD	- 0.008/0.163	TBD	ns,min	OCE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_rst}$ / $T_{hd\_36K\_rst}$	TBD	0.013/0.170	TBD	ns,min	Synchronous reset input Setup/Hold time (36K mode)
$T_{su\_ecc\_d}$ / $T_{hd\_ecc\_d}$	TBD	0.116/0.11	TBD	ns,min	Data input Setup/Hold time (ECC mode)

$T_{su\_fifo\_wctl}$ / $T_{hd\_fifo\_wctl}$	TBD	0.068/0.075	TBD	ns,min	WREN Enter (Setup/Hold time) (18K/36K FIFO mode)
$T_{su\_fifo\_rctl}$ / $T_{hd\_fifo\_rctl}$	TBD	0.153/0.058	TBD	ns,min	RDEN Enter (Setup/Hold time (18K/36K FIFO mode)
$T_{su\_ecc\_injerr}$ / $T_{hd\_ecc\_injerr}$	TBD	0.222/0.017	TBD	ns,min	INJECT_S/DBITERR Enter Setup/Hold time (ECC mode)
T_{mpw_norm}	TBD	0.846	TBD	ns,min	CLKA/CLKB MPW (NW/TW mode)
T_{mpw_rbw}	TBD	0.969	TBD	ns,min	CLKA/CLKB MPW (RBW mode)
T_{mpw_fifo}	TBD	0.846	TBD	ns,min	CLKA/CLKB MPW (FIFO mode)
T_{mpw_ecc}	TBD	0.972	TBD	ns,min	CLKA/CLKB MPW (ECC mode)

Note: The timing parameters of specific usage scenarios are subject to the software timing report

4.3. APM（Arithmetic Process Module）AC characteristic parameters

Table 4- 3 APM AC Characteristics

AC characteristic parameter description	Pre-dder	Multiplier	Post-adder	Numerical value			one bit
				-5	-6	-7	
Setup and hold time from data/control Pin to input register clk							
H → preadd unit register CLK setup/hold	Yes	NA	NA	TBD	1.342/-0.175	TBD	ns
X → preadd unit register CLK setup/hold	Yes	NA	NA	TBD	1.383/-0.205	TBD	ns
X → input unit register CLK setup/hold	NA	NA	NA	TBD	0.477/-0.061	TBD	ns
Y → input unit register CLK setup/hold	NA	NA	NA	TBD	0.322/-0.072	TBD	ns
H → input unit register CLK setup/hold	NA	NA	NA	TBD	0.381/-0.049	TBD	ns
Z → input unit register CLK setup/hold	NA	NA	NA	TBD	0.215/-0.028	TBD	ns
INCTRL → input unit register CLK setup/hold	NA	NA	NA	TBD	0.306/-0.061	TBD	ns
MODEY → input unit register CLK setup/hold	NA	NA	NA	TBD	0.23/-0.068	TBD	ns
MODEZ → input unit register CLK setup/hold	NA	NA	NA	TBD	0.364/-0.077	TBD	ns
Setup and hold time from data Pin to pipeline register clk							
Y → Multiplier unit register CLK setup/hold	NA	Yes	No	TBD	1.434/-0.299	TBD	ns
X → Multiplier unit register CLK setup/hold	Yes	Yes	No	TBD	2.462/-0.415	TBD	ns
X → Multiplier unit register CLK setup/hold	No	Yes	No	TBD	1.562/-0.288	TBD	ns
H-> Multiplier unit register CLK setup/hold	Yes	Yes	No	TBD	2.422/-0.377	TBD	ns
Setup and hold time from data/control Pin to output register clk							

Y → postadd unit register CLK setup/hold	NA	Yes	Yes	TBD	2.486/-0.563	TBD	ns
X → postadd unit register CLK setup/hold	No	Yes	Yes	TBD	2.625/-0.557	TBD	ns
X → postadd unit register CLK setup/hold	Yes	Yes	Yes	TBD	3.530/-0.688	TBD	ns
H → postadd unit register CLK setup/hold	Yes	Yes	Yes	TBD	3.490/-0.633	TBD	ns
Z → postadd unit register CLK setup/hold	NA	NA	Yes	TBD	1.196/-0.253	TBD	ns
Y → postadd unit register CLK setup/hold	NA	No	Yes	TBD	1.296/-0.339	TBD	ns
X → postadd unit register CLK setup/hold	No	No	Yes	TBD	1.387/-0.284	TBD	ns
PI → postadd unit register CLK setup/hold	NA	NA	Yes	TBD	0.908/-0.163	TBD	ns
From register clk at all levels to APM output Pin time							
postadd unit register CLK → P output	NA	NA	NA	TBD	0.470	TBD	ns
Multiplier unit register CLK → Poutput	NA	NA	Yes	TBD	1.606	TBD	ns
Multiplier unit register CLK → Poutput	NA	NA	No	TBD	0.496	TBD	ns
pretadd unit register CLK → DPO output	Yes	Yes	Yes	TBD	2.637	TBD	ns
Z input unit register CLK → DPO output	NA	NA	Yes	TBD	1.532	TBD	ns
Combination logic delay from data/control pin to APM output pin							
Y → P output	NA	Yes	No	TBD	1.833	TBD	ns
Y → P output	NA	Yes	Yes	TBD	2.840	TBD	ns
Y → P output	NA	No	Yes	TBD	1.653	TBD	ns
X → P output	No	Yes	No	TBD	1.960	TBD	ns
X → P output	Yes	Yes	No	TBD	2.718	TBD	ns
X → P output	Yes	Yes	Yes	TBD	3.735	TBD	ns
X → P output	No	No	Yes	TBD	1.745	TBD	ns
H → P output	Yes	Yes	No	TBD	2.803	TBD	ns
H → P output	Yes	Yes	Yes	TBD	3.805	TBD	ns
Z → P output	NA	NA	Yes	TBD	1.547	TBD	ns
PI → P output	NA	NA	Yes	TBD	1.323	TBD	ns

Note: The timing parameters of specific usage scenarios are subject to the software timing report

4.4. GPLL AC Characteristics Parameters

Table 4-4 GPLL AC Characteristics

Index	Minimum	Maximum value	Unit	Description
F_{IN}	10	800	MHz	input clock frequency

F_{INJIT}	-- -	300	ps	Input Clock Period Jitter (F_{IN} < 200MHz)
	-- -	0.06	UI	Input Clock Period Jitter (F_{IN} ≥ 200MHz)
F_{INDT}	10-49MHz： 25% 50-199MHz： 30% 200-399MHz： 35% 400-499MHz： 40% 500-800MHz： 45%			Input clock duty cycle
F_{PFD}	10	450	MHz	PFD operating frequency range
F_{VCO}	600	1200	MHz	VCO operating frequency range
F_{OUT}	4.69	800	MHz	Output clock frequency range
F_{OUTCAS}	0.0366	800	MHz	Output Cascade Frequency Range
T_{PHO}	0.12		ns	Static phase offset
T_{OUTJIT}	180		ps	Output Clock Period Jitter (F_{OUT} ≥ 100MHz)
	0.018		UI	Output Clock Period Jitter (F_{OUT} < 100MHz)
$T_{OUTDUTY}$	50% ± 5%			Output Clock Duty Cycle Accuracy (50% Case)
F_{BW}	1	4	MHz	Loop bandwidth
T_{LOCK}	-- -	200	us	Lock time
F_{DPS_CLK}	0.01	450	MHz	Dynamic Phase Shift Clock Frequency
T_{RST}	10	-- -	ns	Reset signal width

4.5. PPLL AC characteristic parameters

Table 4-5 PPLL AC Characteristics

Index	Minimum	Maximum value	Unit	Description
F_{IN}	19	800	MHz	Input clock frequency
F_{INJIT}	-- -	200	ps	Input Clock Period Jitter (F_{IN} < 200MHz)
	-- -	0.04	UI	Input Clock Period Jitter (F_{IN} ≥ 200MHz)
F_{INDT}	10-49MHz： 25% 50-199MHz： 30% 200-399MHz： 35% 400-499MHz： 40% 500-800MHz： 45%			Input clock duty cycle
F_{PFD}	19	450	MHz	PFD operating frequency range
F_{VCO}	1330	2133	MHz	VCO operating frequency range
F_{OUT1}	10.39	2133	MHz	Output clock frequency range (CLKOUTPHY output)
F_{OUT2}	10.39	800	MHz	Output clock frequency range (CLKOUT0 etc. output)
T_{PHO}	0.12		ns	static phase offset
T_{OUTJTT}	180		ps	Output Clock Period Jitter (F_{OUT} ≥ 100MHz)
	0.018		UI	Output Clock Period Jitter (F_{OUT} < 100MHz)
T_{OUTDT}	50% ± 5%			Output Clock Duty Cycle Accuracy (50% Case)
F_{BW}	1	4	MHz	bandwidth
T_{LOCK}	-- -	120	us	lock time
T_{RST}	10	-- -	ns	Reset signal width

4.6. DQS AC characteristic parameters

DQS phase adjustment are as follows :

Table 4-6 HR IO DQS AC Characteristics

Category	Speed class	AC characteristic parameter description			Unit
		Minimum	Typical value	maximum value	
DQS	- 6	4	7	10	ps

Table 4-7 HP IO DQS AC Characteristics

Category	Speed class	AC characteristic parameter description			Unit
		minimum	Typical value	maximum value	
DQS	- 6	2.5	5.5	8.5	ps

4.7. Global Clock Network (Global Clock Network) AC characteristic parameters

Table 4-8 Global Clock Network AC Characteristics

Name	Maximum frequency	Unit	Description
	- 6		
GLOBAL CLK	710	MHz	global clock network

4.8. Regional clock network (Regional clock network) Clock Network) AC characteristic parameters

Table 4-9 Regional Clock Network AC Characteristics

Name	Maximum frequency	Unit	Description
	- 6		
REGIONAL CLK	540	MHz	regional clock network

Note: The maximum input frequency is 650 MHz

4.9. IO Clock Network（IO Clock Network）AC characteristic parameters

Table 4-10 IO Clock Network AC Characteristics

Name	Maximum frequency	Unit	Description
	- 6		
IO CLK	800	MHz	IO clock network

4.10. Configuration and Programming AC characteristic parameters

4.10.1. Power-up Timing feature

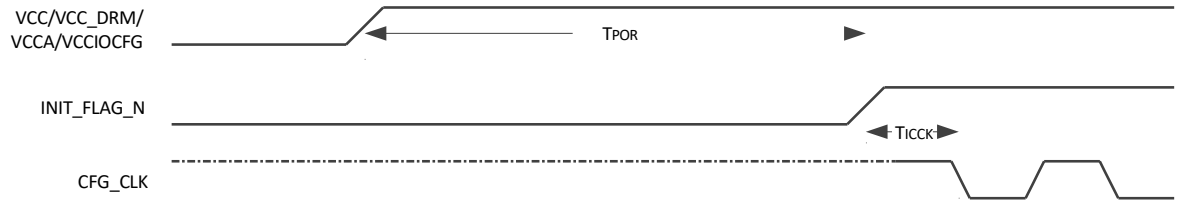

Figure 4-1 Device Power-up Timing feature

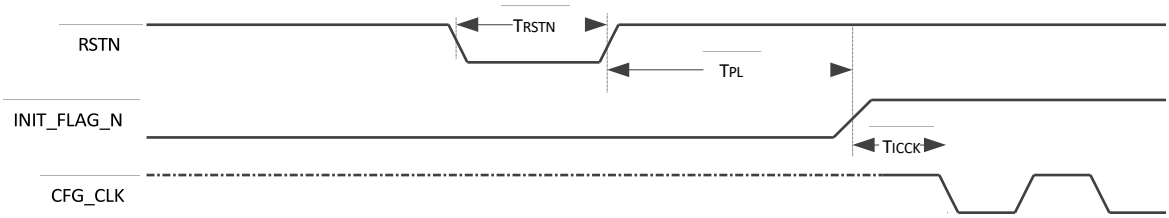

Figure 4-2 Device Reset Reconfiguration Timing Feature

Table 4-11 Power-up Timing

Name	Device	Value	Unit	Description
T_{PL}	PG2T390H	34	ms, Max	Program Latency
T_{POR}		30	ms, Min	Power-on-Reset
		94	ms, Max	
T_{ICCK}		400	ns,Min	CFG_CLK output delay
T_{RSTN}		240	ns,Min	RSTN low pulse width

Note: Refer to " UG050005_Titan2 Series FPGA Configuration (Configuration) User Guide" for detailed description .

4.10.2. Communication characteristics of each download mode

Table 4-12 AC Characteristics of Each Download Mode Supported by Titan2 Series FPGAs

Interface	Name	Description	Numerical value	Attributes
JTAG	F_{TCK}	TCK frequency	50M	maximum
	T_{TCKD}	TCK duty cycle	45%/55%	min / max
	T_{TCKH}	TCK high pulse width	10ns	minimum
	T_{TCKL}	TCK low pulse width	10ns	minimum
	T_{TMSSU}/T_{TDISU}	TMS/TDI setup time (rising edge of TCK)	3.5ns	minimum
	T_{TMSH}/T_{TDIH}	TMS/TDI hold time (TCK rising edge)	1.5ns	minimum
	$T_{TCK2TDO}$	TCK falling edge to TDO output valid	6ns	maximum
Master SPI mode	F_{MCLK}	CFG_CLK frequency	40M	maximum
		CFG_CLK frequency (low speed)	15.38M	maximum
		CFG_CLK frequency (daisy chain)	25M	maximum
	F_{MCLKS}	CFG_CLK frequency initial value	2.99M	typical
	F_{MCLKD}	CFG_CLK duty cycle	45%/55%	min / max
	$F_{MCLKTOL}$	CFG_CLK frequency deviation	50 %	maximum
	F_{EMCLK}	ECCLKIN frequency	66M	maximum
		ECCLKIN frequency (low speed)	33M	maximum
	F_{EMCLKD}	ECCLKIN duty cycle	45%/55%	min / max
	T_{MDSU}	D[7:0] setup time (CFG_CLK rising edge)	9.5ns	minimum
	T_{MDH}	D[7:0] hold time (CFG_CLK rising edge)	0ns	minimum
	T_{MDSUF}	D[7:0] setup time (CFG_CLK falling edge)	9.5ns	minimum
	T_{MDHF}	D[7:0] hold time (CFG_CLK falling edge)	0ns	minimum
	T_{MCLK2D}	CFG_CLK falling edge to D[0]/D[4] output valid	3.5ns	maximum
	$T_{MCLK2CS}$	CFG_CLK falling edge to FCS_N/FCS2_N output valid	4ns	maximum
	$T_{MCLK2DOUT}$	CFG_CLK falling edge to CSO_DOUT output valid	3.5ns	maximum
Slave Serial	F_{SSCLK}	CFG_CLK frequency	50M	maximum
	T_{SSCLKL}	CFG_CLK low pulse width	10ns	minimum
	T_{SSCLKH}	CFG_CLK high pulse width	10ns	minimum
	T_{SSDSU}	DI setup time (CFG_CLK rising edge)	3.5ns	minimum
	T_{SSDH}	DI hold time (CFG_CLK rising edge)	0ns	minimum
	T_{SSDSUF}	DI setup time (CFG_CLK falling edge)	3.5ns	minimum
	T_{SSDHF}	DI hold time (CFG_CLK falling edge)	0ns	minimum
	$T_{SSCLK2DOUT}$	CFG_CLK falling edge to CSO_DOUT output valid	2ns/7ns	min / max
Slave Parallel	F_{SPCLK}	CFG_CLK frequency	50M	maximum
	T_{SPCLKL}	CFG_CLK low pulse width	10ns	minimum
	T_{SPCLKH}	CFG_CLK high pulse width	10ns	minimum
	T_{SPDSU}	D[31:0] setup time (CFG_CLK rising edge)	5.5ns	minimum
	T_{SPDH}	D[31:0] hold time (CFG_CLK rising edge)	0.5ns	minimum
	T_{SPCRSU}	CS_N/RWSEL setup time (CFG_CLK rising edge)	4.5ns	minimum
	T_{SPCRH}	CS_N/RWSEL hold time (CFG_CLK rising edge)	0.5ns	minimum
	$T_{SPCLK2D}$	CFG_CLK rising edge to D[31:0] output valid	9ns	maximum
	$T_{SPCS2CSO}$	CS_N to CSO_DOUT output delay	8.5ns	maximum
	F_{IPCLK}	CLK frequency	50M	maximum
	T_{IPCLKL}	CLK low pulse width	10ns	minimum
	T_{IPCLKH}	CLK high pulse width	10ns	minimum
	T_{IPDSU}	CS_N/RW_SEL/DI[31:0] setup time (CLK rising edge)	2ns	minimum
	T_{IPDH}	CS_N/RW_SEL/DI[31:0] hold time (CLK rising edge)	1ns	minimum

Internal slave parallel interface	$T_{IPCLK2D}$	CLK rising edge to DO[31:0] output valid	4ns	maximum
	$T_{IPCLK2D1}$	CLK rising edge to RBCRC_VALID/ECC_VALID/DRCFG_OVER/PRCFG_ OVER output is valid	2ns	maximum
	$T_{IPCLK2D2}$	CLK rising edge to RBCRC_ERR/ECC_INDEX/SERROR/DERROR/SEU_FRAME_ADDR/SEU_FRAME_NADDR SEU_COLUMN_ADDR/SEU_COLUMN_NADDR SEU_REGION_ADDR/SEU_REGION_NADDR DRCFG_ERR/PRCFG_ERR output valid	0	maximum

4.11. IOB AC characteristic parameters

IOB are shown in the following table, where DO=>PAD is the delay from IOB port DO through OBUF to PAD ; PAD=>DIN is the delay from PAD through IBUF to IOB port DIN .

Table 4-13 IOB High Range(HR) AC characteristic parameters

I/O standard	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
LVCMOS33 STRENGTH "4" MODE "F"	2.802	0.915
LVCMOS33 STRENGTH "4" MODE"S"	3.905	0.915
LVCMOS33 STRENGTH "8" MODE"F"	2.247	0.915
LVCMOS33 STRENGTH "8" MODE"S"	2.990	0.915
LVCMOS33 STRENGTH"12" MODE"F"	1.851	0.915
LVCMOS33 STRENGTH"12" MODE"S"	2.646	0.915
LVCMOS33 STRENGTH"16" MODE"F"	1.575	0.915
LVCMOS33 STRENGTH"16" MODE"S"	2.184	0.915
LVTTL33 STRENGTH "4" MODE"F"	2.802	0.915
LVTTL33 STRENGTH "4" MODE"S"	3.905	0.915
LVTTL33 STRENGTH "8" MODE"F"	2.247	0.915

LVTTL33 STRENGTH "8" MODE"S"	2.990	0.915
LVTTL33 STRENGTH"12" MODE"F"	1.851	0.915
LVTTL33 STRENGTH"12" MODE"S"	2.646	0.915
LVTTL33 STRENGTH"16" MODE"F"	1.575	0.915
LVTTL33 STRENGTH"16" MODE"S"	2.184	0.915
LVTTL33 STRENGTH"24" MODE"F"	1.387	0.915
LVTTL33 STRENGTH"24" MODE"S"	2.096	0.915
LVCMOS25 STRENGTH"4" MODE"F"	2.482	0.984
LVCMOS25 STRENGTH"4" MODE"S"	3.425	0.984
LVCMOS25 STRENGTH"8" MODE"F"	1.935	0.984
LVCMOS25 STRENGTH"8" MODE"S"	2.695	0.984
LVCMOS25 STRENGTH"12" MODE"F"	1.677	0.984
LVCMOS25 STRENGTH "12" MODE "S"	2.384	0.984
LVCMOS25 STRENGTH"16"MODE"F"	1.546	0.984
LVCMOS25 STRENGTH"16" MODE"S"	2.147	0.984
LVCMOS18 STRENGTH"4"MODE"F"	1.755	1.091
LVCMOS18 STRENGTH "4" MODE "S"	2.094	1.091
LVCMOS18 STRENGTH"8"MODE"F"	1.163	1.091
LVCMOS18 STRENGTH"8"MODE"S"	1.414	1.091

LVCMOS18 STRENGTH"12"MODE"F"	0.982	1.091
LVCMOS18 STRENGTH "12" MODE "S"	1.054	1.091
LVCMOS18 STRENGTH"16"MODE"F"	0. 879	1.091
LVCMOS18 STRENGTH"16" MODE"S"	1.074	1.091
LVCMOS18 STRENGTH"24"MODE"F"	0.901	1.091
LVCMOS18 STRENGTH"24"MODE"S"	1.031	1.091
LVCMOS15 STRENGTH"4"MODE"F"	1.648	1.196
LVCMOS15 STRENGTH "4" MODE "S"	1.995	1.196
LVCMOS15 STRENGTH"8"MODE"F"	1.099	1.196
LVCMOS15 STRENGTH"8"MODE"S"	1.330	1.196
LVCMOS15 STRENGTH"12" MODE"F"	0.860	1.196
LVCMOS15 STRENGTH"12" MODE"S"	1.011	1.196
LVCMOS15 STRENGTH"16" MODE"F"	0.879	1.196
LVCMOS15 STRENGTH"16" MODE"S"	1.003	1.196
LVCMOS12 STRENGTH"4" MODE"F"	1.559	1.357
LVCMOS12 STRENGTH"4" MODE"S"	1.900	1.357
LVCMOS12 STRENGTH"8" MODE"F"	1.041	1.357
LVCMOS12 STRENGTH"8" MODE"S"	1.267	1.357
LVCMOS12 STRENGTH"12" MODE"F"	0.999	1.357

LVCMOS12 STRENGTH"12" MODE"S"	1.133	1.357
SSTL18_I STRENGTH"8" MODE"F"	1.163	0.954
SSTL18_I STRENGTH"8" MODE"S"	1.414	0.954
SSTL18_I STRENGTH"13.4" MODE"F"	0.710	0.954
SSTL18_I STRENGTH"13.4" MODE"S"	0.819	0.954
SSTL18_II STRENGTH"8"MODE"F"	1.163	0.954
SSTL18_II STRENGTH"8" MODE"S"	1.414	0.954
SSTL18_II STRENGTH"13.4" MODE"F"	0.710	0.954
SSTL18_II STRENGTH"13.4" MODE"S"	0.819	0.954
SSTL18D_I STRENGTH"8" MODE"F"	1.163	0.954
SSTL18D_I STRENGTH"8" MODE"S"	1.414	0.954
SSTL18D_I STRENGTH "13.4" MODE"F"	0.710	0.954
SSTL18D_I STRENGTH "13.4" MODE"S"	0.819	0.954
SSTL18D_II STRENGTH"8" MODE"F"	1.163	0.954
SSTL18D_II STRENGTH"8" MODE"S"	1.414	0.954
SSTL18D_II STRENGTH"13.4" MODE"F"	0.710	0.954
SSTL18D_II STRENGTH"13.4" MODE"S"	0.819	0.954
HSTL18_I STRENGTH"8" MODE"F"	1.163	0.954
HSTL18_I STRENGTH"8" MODE"S"	1.414	0.954

HSTL18_I STRENGTH"16" MODE"F"	0.710	0.954
HSTL18_I STRENGTH"16" MODE"S"	0.819	0.954
HSTL18_II STRENGTH"8" MODE"F"	1.163	0.954
HSTL18_II STRENGTH"8" MODE"S"	1.414	0.954
HSTL18_II STRENGTH"16" MODE"F"	0.710	0.954
HSTL18_II STRENGTH"16" MODE"S"	0.819	0.954
HSTL18D_I STRENGTH"8" MODE"F"	1.163	0.954
HSTL18D_I STRENGTH"8" MODE"S"	1.414	0.954
HSTL18D_I STRENGTH"16" MODE"F"	0.710	0.954
HSTL18D_I STRENGTH"16" MODE"S"	0.819	0.954
HSTL18D_II STRENGTH"8"MODE"F"	1.163	0.954
HSTL18D_II STRENGTH"8"MODE"S"	1.414	0.954
HSTL18D_II STRENGTH"16"MODE"F"	0.710	0.954
HSTL18D_II STRENGTH"16" MODE"S"	0.819	0.954
SSTL15_I STRENGTH "8.9" MODE "F"	0.798	1.039
SSTL15_I STRENGTH "8.9" MODE "S"	0.942	1.039
SSTL15_I STRENGTH "13" MODE "F"	0.799	1.039
SSTL15_I STRENGTH"13" MODE"S"	0.956	1.039
SSTL15_II STRENGTH "8.9" MODE "F"	0.798	1.039

SSTL15_II STRENGTH "8.9" MODE "S"	0.942	1.039
SSTL15_II STRENGTH "13" MODE "F"	0.799	1.039
SSTL15_II STRENGTH"13" MODE"S"	0.956	1.039
SSTL15D_I STRENGTH "8.9" MODE "F"	0.798	1.039
SSTL15D_I STRENGTH "8.9" MODE "S"	0.942	1.039
SSTL15D_I STRENGTH "13" MODE "F"	0.799	1.039
SSTL15D_I STRENGTH"13" MODE"S"	0.956	1.039
SSTL15D_II STRENGTH "8.9" MODE "F"	0.798	1.039
SSTL15D_II STRENGTH"8.9" MODE"S"	0.942	1.039
SSTL15D_II STRENGTH"13" MODE"F"	0.799	1.039
SSTL15D_II STRENGTH"13" MODE"S"	0.956	1.039
HSTL15_I STRENGTH"8" MODE"F"	0.798	1.039
HSTL15_I STRENGTH"8" MODE"S"	0.942	1.039
HSTL15_I STRENGTH"16" MODE"F"	0.799	1.039
HSTL15_I STRENGTH"16" MODE"S"	0.956	1.039
HSTL15_II STRENGTH"8" MODE"F"	0.798	1.039
HSTL15_II STRENGTH"8" MODE"S"	0.942	1.039
HSTL15_II STRENGTH"16" MODE"F"	0.799	1.039
HSTL15_II STRENGTH"16" MODE"S"	0.956	1.039

HSTL15D_I STRENGTH"8" MODE"F"	0.798	1.039
HSTL15D_I STRENGTH"8" MODE"S"	0.942	1.039
HSTL15D_I STRENGTH"16" MODE"F"	0.799	1.039
HSTL15D_I STRENGTH"16" MODE"S"	0.956	1.039
HSTL15D_II STRENGTH"8" MODE"F"	0.798	1.039
HSTL15D_II STRENGTH"8" MODE"S"	0.942	1.039
HSTL15D_II STRENGTH"16" MODE"F"	0.799	1.039
HSTL15D_II STRENGTH"16" MODE"S"	0.956	1.039
SSTL135_I STRENGTH"8.9" MODE"F"	0.817	1.174
SSTL135_I STRENGTH"8.9" MODE"S"	0.964	1.174
SSTL135_I STRENGTH"13" MODE"F"	0.771	1.174
SSTL135_I STRENGTH"13" MODE"S"	0.924	1.174
SSTL135_II STRENGTH"8.9" MODE"F"	0.817	1.174
SSTL135_II STRENGTH"8.9" MODE"S"	0.964	1.174
SSTL135_II STRENGTH"13" MODE"F"	0.771	1.174
SSTL135_II STRENGTH"13" MODE"S"	0.924	1.174
SSTL135D_I STRENGTH "8.9" MODE"F"	0.817	1.174
SSTL135D_I STRENGTH "8.9" MODE"S"	0.964	1.174
SSTL135D_I STRENGTH"13" MODE"F"	0.771	1.174

SSTL135D_I STRENGTH"13" MODE"S"	0.924	1.174
SSTL135D_II STRENGTH"8.9" MODE"F"	0.817	1.174
SSTL135D_II STRENGTH"8.9" MODE"S"	0.964	1.174
SSTL135D_II STRENGTH"13" MODE"F"	0.771	1.174
SSTL135D_II STRENGTH"13" MODE"S"	0.924	1.174
LPDDR MODE "F"	1.041	1.357
LPDDR MODE "S"	1.267	1.357
HSUL12 MODE "F"	1.041	1.357
HSUL12 MODE "S"	1.267	1.357
TMDS	1.056	1.039
LVDS25	1.056	1.039
MINI- LVDS	1.056	1.039
RSDS	0.99	1.039
PPDS	0.99	1.039

Note: The timing parameters of specific usage scenarios are subject to the software timing report

Table 4-14 IOB High Performance (HP) AC characteristic parameters

I/O standard	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
LVCMOS18 STRENGTH"2"MODE"F"	1.980	0.318
LVCMOS18 STRENGTH"2"MODE"M"	2.142	0.318
LVCMOS18 STRENGTH"2" MODE"S"	2.287	0.318
LVCMOS18 STRENGTH"4"MODE"F"	1.792	0.318

LVCMOS18 STRENGTH"4"MODE"M"	1.946	0.318
LVCMOS18 STRENGTH "4" MODE "S"	2.081	0.318
LVCMOS18 STRENGTH"6"MODE"F"	1.700	0.318
LVCMOS18 STRENGTH"6"MODE"M"	1.852	0.318
LVCMOS18 STRENGTH"6"MODE"S"	1.983	0.318
LVCMOS18 STRENGTH"8"MODE"F"	1.605	0.318
LVCMOS18 STRENGTH"8"MODE"M"	1.747	0.318
LVCMOS18 STRENGTH"8"MODE"S"	1.869	0.318
LVCMOS18 STRENGTH"12"MODE"F"	1.558	0.318
LVCMOS18 STRENGTH"12"MODE"M"	1.695	0.318
LVCMOS18 STRENGTH "12" MODE "S"	1.814	0.318
LVCMOS18 STRENGTH"16"MODE"F"	1.514	0.318
LVCMOS18 STRENGTH"16" MODE"M"	1.648	0.318
LVCMOS18 STRENGTH"16" MODE"S"	1.762	0.318
LVCMOS15 STRENGTH"2" MODE"F"	1.971	0.359
LVCMOS15 STRENGTH"2" MODE"M"	2.124	0.359
LVCMOS15 STRENGTH"2" MODE"S"	2.260	0.359
LVCMOS15 STRENGTH "4" MODE"F"	1.694	0.359
LVCMOS15 STRENGTH "4" MODE"M"	1.837	0.359

LVCMOS15 STRENGTH "4" MODE"S"	1.959	0.359
LVCMOS15 STRENGTH"6" MODE"F"	1.600	0.359
LVCMOS15 STRENGTH"6" MODE"M"	1.734	0.359
LVCMOS15 STRENGTH"6" MODE"S"	1.850	0.359
LVCMOS15 STRENGTH"8" MODE"F"	1.553	0.359
LVCMOS15 STRENGTH"8" MODE"M"	1.682	0.359
LVCMOS15 STRENGTH"8" MODE"S"	1.795	0.359
LVCMOS15 STRENGTH"12" MODE"F"	1.514	0.359
LVCMOS15 STRENGTH"12" MODE"M"	1.643	0.359
LVCMOS15 STRENGTH"12" MODE"S"	1.751	0.359
LVCMOS15 STRENGTH"16" MODE"F"	1.528	0.359
LVCMOS15 STRENGTH"16" MODE"M"	1.629	0.359
LVCMOS15 STRENGTH"16" MODE"S"	1.714	0.359
LVCMOS12 STRENGTH"2" MODE"F"	1.964	0.439
LVCMOS12 STRENGTH"2" MODE"M"	2.102	0.439
LVCMOS12 STRENGTH"2" MODE"S"	2.226	0.439
LVCMOS12 STRENGTH"4" MODE"F"	1.686	0.439
LVCMOS12 STRENGTH"4" MODE"M"	1.817	0.439
LVCMOS12 STRENGTH"4" MODE"S"	1.932	0.439

LVCMOS12 STRENGTH"6" MODE"F"	1.629	0.439
LVCMOS12 STRENGTH"6" MODE"M"	1.754	0.439
LVCMOS12 STRENGTH"6" MODE"S"	1.879	0.439
LVCMOS12 STRENGTH"8" MODE"F"	1.566	0.439
LVCMOS12 STRENGTH"8" MODE"M"	1.691	0.439
LVCMOS12 STRENGTH"8" MODE"S"	1.819	0.439
SSTL18_I STRENGTH"8" MODE"F"	1.563	0.576
SSTL18_I STRENGTH"8" MODE"M"	1.650	0.576
SSTL18_I STRENGTH"8" MODE"S"	1.717	0.576
SSTL18_II STRENGTH"13.4" MODE"F"	1.515	0.576
SSTL18_II STRENGTH"13.4" MODE"M"	1.585	0.576
SSTL18_II STRENGTH"13.4" MODE"S"	1.635	0.576
SSTL18D_I STRENGTH"8"MODE"F"	1.563	0.376
SSTL18D_I STRENGTH"8"MODE"M"	1.650	0.376
SSTL18D_I STRENGTH"8"MODE"S"	1.717	0.376
SSTL18D_II STRENGTH "13.4" MODE "F"	1.515	0.376
SSTL18D_II STRENGTH "13.4" MODE "M"	1.585	0.376
SSTL18D_II STRENGTH "13.4" MODE "S"	1.635	0.376
HSTL18_I STRENGTH"8"MODE"F"	1.589	0.576

HSTL18_I STRENGTH"8"MODE"M"	1.678	0.576
HSTL18_I STRENGTH"8"MODE"S"	1.747	0.576
HSTL18_II STRENGTH"16"MODE"F"	1.515	0.576
HSTL18_II STRENGTH"16"MODE"M"	1.585	0.576
HSTL18_II STRENGTH"16" MODE"S"	1.635	0.576
HSTL18D_I STRENGTH"8"MODE"F"	1.589	0.63
HSTL18D_I STRENGTH"8"MODE"M"	1.678	0.376
HSTL18D_I STRENGTH"8"MODE"S"	1.747	0.376
HSTL18D_II STRENGTH"16"MODE"F"	1.515	0.376
HSTL18D_II STRENGTH"16"MODE"M"	1.585	0.376
HSTL18D_II STRENGTH"16" MODE"S"	1.635	0.376
SSTL15_I STRENGTH"8.9" MODE"F"	1.585	0.525
SSTL15_I STRENGTH"8.9" MODE"M"	1.669	0.525
SSTL15_I STRENGTH"8.9" MODE"S"	1.734	0.525
SSTL15_II STRENGTH"13" MODE"F"	1.549	0.525
SSTL15_II STRENGTH"13" MODE"M"	1.615	0.525
SSTL15_II STRENGTH"13" MODE"S"	1.667	0.525
SSTL15D_I STRENGTH "8.9" MODE"F"	1.585	0.374
SSTL15D_I STRENGTH "8.9" MODE"M"	1.669	0.374

SSTL15D_I STRENGTH "8.9" MODE"S"	1.734	0.374
SSTL15D_II STRENGTH"13" MODE"F"	1.549	0.374
SSTL15D_II STRENGTH"13" MODE"M"	1.615	0.374
SSTL15D_II STRENGTH"13" MODE"S"	1.667	0.374
HSTL15_I STRENGTH"8" MODE"F"	1.558	0.525
HSTL15_I STRENGTH"8" MODE"M"	1.642	0.525
HSTL15_I STRENGTH"8" MODE"S"	1.705	0.525
HSTL15_II STRENGTH"16" MODE"F"	1.514	0.525
HSTL15_II STRENGTH"16" MODE"M"	1.580	0.525
HSTL15_II STRENGTH"16" MODE"S"	1.629	0.525
HSTL15D_I STRENGTH"8" MODE"F"	1.558	0.374
HSTL15D_I STRENGTH"8" MODE"M"	1.642	0.374
HSTL15D_I STRENGTH"8" MODE"S"	1.705	0.374
HSTL15D_II STRENGTH"16" MODE"F"	1.514	0.374
HSTL15D_II STRENGTH"16" MODE"M"	1.580	0.374
HSTL15D_II STRENGTH"16" MODE"S"	1.629	0.374
SSTL135_I STRENGTH"8.9" MODE"F"	1.556	0.495
SSTL135_I STRENGTH"8.9" MODE"M"	1.636	0.495
SSTL135_I STRENGTH"8.9" MODE"S"	1.697	0.495

SSTL135_II STRENGTH"13" MODE"F"	1.519	0.495
SSTL135_II STRENGTH"13" MODE"M"	1.599	0.495
SSTL135_II STRENGTH"13" MODE"S"	1.660	0.495
SSTL135D_I STRENGTH "8.9" MODE"F"	1.556	0.374
SSTL135D_I STRENGTH "8.9" MODE"M"	1.636	0.374
SSTL135D_I STRENGTH "8.9" MODE"S"	1.697	0.374
SSTL135D_II STRENGTH"13" MODE"F"	1.519	0.374
SSTL135D_II STRENGTH"13" MODE"M"	1.599	0.374
SSTL135D_II STRENGTH"13" MODE"S"	1.660	0.374
SSTL12 STRENGTH"14.25" MODE"F"	1.540	0.477
SSTL12 STRENGTH"14.25" MODE"M"	1.598	0.477
SSTL12 STRENGTH"14.25" MODE"S"	1.651	0.477
SSTL12D STRENGTH "14.25" MODE "F"	1.540	0.374
SSTL12D STRENGTH"14.25" MODE"M"	1.598	0.374
SSTL12D STRENGTH"14.25" MODE"S"	1.651	0.374
HSUL12 STRENGTH "0.1" MODE "F"	1.615	0.477
HSUL12 STRENGTH "0.1" MODE "M"	1.694	0.477
HSUL12 STRENGTH "0.1" MODE "S"	1.754	0.477
HSUL12D STRENGTH "0.1" MODE "F"	1.615	0.374
HSUL12D STRENGTH "0.1" MODE "M"	1.694	0.374
HSUL12D STRENGTH "0.1" MODE "S"	1.754	0.374
POD12 MODE"F"	1.562	0.477
POD12 MODE"M"	1.632	0.477
POD12 MODE"S"	1.697	0.477

POD12D MODE"F"	1.562	0.374
POD12D MODE"M"	1.632	0.374
POD12D MODE"S"	1.697	0.374
HSTL12_I STRENGTH"6.3" MODE"F"	1.535	0.477
HSTL12_I STRENGTH"6.3" MODE"M"	1.609	0.477
HSTL12_I STRENGTH"6.3" MODE"S"	1.670	0.477
HSTL12D_I STRENGTH"6.3" MODE"F"	1.46	0.374
HSTL12D_I STRENGTH"6.3" MODE"M"	1.51	0.374
HSTL12D_I STRENGTH"6.3" MODE"S"	1.56	0.374
LVDS_18	1.061	0.376
LVCAL_15, MODE"F"	1.600	0.359
LVCAL_15, MODE"M"	1.734	0.359
LVCAL_15, MODE"S"	1.850	0.359
LVCAL_18, MODE"F"	1.605	0.318
LVCAL_18, MODE"M"	1.747	0.318
LVCAL_18, MODE"S"	1.869	0.318
HSLVCAL_15, MODE"F"	1.585	0.525
HSLVCAL_15, MODE"M"	1.669	0.525
HSLVCAL_15, MODE"S"	1.734	0.525
HSLVCAL_18, MODE"F"	1.589	0.576
HSLVCAL_18, MODE"M"	1.678	0.576
HSLVCAL_18, MODE"S"	1.747	0.576
SSTL18_I_CAL STRENGTH"8" MODE"F"	1.563	0.576
SSTL18_I_CAL STRENGTH"8" MODE"M"	1.650	0.576
SSTL18_I_CAL STRENGTH"8" MODE"S"	1.717	0.576
SSTL18_II_CAL STRENGTH"13.4" MODE"F"	1.515	0.576
SSTL18_II_CAL STRENGTH"13.4" MODE"M"	1.585	0.576
SSTL18_II_CAL STRENGTH"13.4" MODE"S"	1.635	0.576
SSTL18D_I_CAL STRENGTH"8" MODE"F"	1.563	0.376
SSTL18D_I_CAL STRENGTH"8" MODE"M"	1.650	0.376
SSTL18D_I_CAL STRENGTH"8"MODE"S"	1.717	0.376
SSTL18D_II_CAL STRENGTH "13.4" MODE "F"	1.515	0.376
SSTL18D_II_CAL STRENGTH "13.4" MODE "M"	1.585	0.376
SSTL18D_II_CAL STRENGTH "13.4" MODE "S"	1.635	0.376
HSTL18_I_CAL STRENGTH"8" MODE"F"	1.589	0.576

HSTL18_I_CAL STRENGTH"8"MODE"M"	1.678	0.576
HSTL18_I_CAL STRENGTH"8"MODE"S"	1.747	0.576
HSTL18_II_CAL STRENGTH"16"MODE"F"	1.515	0.576
HSTL18_II_CAL STRENGTH"16"MODE"M"	1.585	0.576
HSTL18_II_CAL STRENGTH"16" MODE"S"	1.635	0.576
HSTL18D_I_CAL STRENGTH"8"MODE"F"	1.589	0.376
HSTL18D_I_CAL STRENGTH"8"MODE"M"	1.678	0.376
HSTL18D_I_CAL STRENGTH"8"MODE"S"	1.747	0.376
HSTL18D_II_CAL STRENGTH"16"MODE"F"	1.515	0.376
HSTL18D_II_CAL STRENGTH"16"MODE"M"	1.585	0.376
HSTL18D_II_CAL STRENGTH"16" MODE"S"	1.635	0.376
SSTL15_I_CAL STRENGTH "8.9" MODE "F"	1.585	0.525
SSTL15_I_CAL STRENGTH"8.9"MODE"M"	1.669	0.525
SSTL15_I_CAL STRENGTH "8.9" MODE "S"	1.734	0.525
SSTL15_II_CAL STRENGTH "13" MODE "F"	1.549	0.525
SSTL15_II_CAL STRENGTH"13"MODE"M"	1.615	0.525
SSTL15_II_CAL STRENGTH"13" MODE"S"	1.667	0.525
SSTL15D_I_CAL STRENGTH "8.9" MODE "F"	1.585	0.374
SSTL15D_I_CAL STRENGTH "8.9" MODE"M"	1.669	0.374
SSTL15D_I_CAL STRENGTH "8.9" MODE"S"	1.734	0.374
SSTL15D_II_CAL STRENGTH"13" MODE"F"	1.549	0.374
SSTL15D_II_CAL STRENGTH"13" MODE"M"	1.615	0.374
SSTL15D_II_CAL STRENGTH"13" MODE"S"	1.667	0.374
HSTL15_I_CAL STRENGTH"8" MODE"F"	1.558	0.525
HSTL15_I_CAL STRENGTH"8" MODE"M"	1.642	0.525
HSTL15_I_CAL STRENGTH"8" MODE"S"	1.705	0.525
HSTL15_II_CAL STRENGTH"16" MODE"F"	1.514	0.525
HSTL15_II_CAL STRENGTH"16" MODE"M"	1.580	0.525
HSTL15_II_CAL STRENGTH"16" MODE"S"	1.629	0.525

HSTL15D_I_CAL STRENGTH"8" MODE"F"	1.558	0.374
HSTL15D_I_CAL STRENGTH"8" MODE"M"	1.642	0.374
HSTL15D_I_CAL STRENGTH"8" MODE"S"	1.705	0.374
HSTL15D_II_CAL STRENGTH"16" MODE"F"	1.514	0.374
HSTL15D_II_CAL STRENGTH"16" MODE"M"	1.580	0.374
HSTL15D_II_CAL STRENGTH"16" MODE"S"	1.629	0.374
SSTL135_I_CAL STRENGTH "8.9" MODE"F"	1.556	0.495
SSTL135_I_CAL STRENGTH"8.9" MODE"M"	1.636	0.495
SSTL135_I_CAL STRENGTH "8.9" MODE"S"	1.697	0.495
SSTL135_II_CAL STRENGTH"13" MODE"F"	1.519	0.495
SSTL135_II_CAL STRENGTH"13" MODE"M"	1.599	0.495
SSTL135_II_CAL STRENGTH"13" MODE"S"	1.660	0.495
SSTL135D_I_CAL STRENGTH "8.9" MODE"F"	1.556	0.374
SSTL135D_I_CAL STRENGTH "8.9" MODE"M"	1.636	0.374
SSTL135D_I_CAL STRENGTH "8.9" MODE"S"	1.697	0.374
SSTL135D_II_CAL STRENGTH"13" MODE"F"	1.519	0.374
SSTL135D_II_CAL STRENGTH"13" MODE"M"	1.599	0.374
SSTL135D_II_CAL STRENGTH"13" MODE"S"	1.660	0.374
SSTL12_CAL STRENGTH"14.25" MODE"F"	1.540	0.477
SSTL12_CAL STRENGTH"14.25" MODE"M"	1.598	0.477
SSTL12_CAL STRENGTH"14.25" MODE"S"	1.651	0.477
SSTL12D_CAL STRENGTH "14.25" MODE"F"	1.540	0.374

SSTL12D_CAL STRENGTH "14.25" MODE"M"	1.598	0.374
SSTL12D_CAL STRENGTH "14.25" MODE"S"	1.651	0.374
HSUL12_CAL STRENGTH"0.1" MODE"F"	1.615	0.477
HSUL12_CAL STRENGTH"0.1" MODE"M"	1.694	0.477
HSUL12_CAL STRENGTH"0.1" MODE"S"	1.754	0.477
HSUL12D_CAL STRENGTH "0.1" MODE "F"	1.615	0.374
HSUL12D_CAL STRENGTH "0.1" MODE "M"	1.694	0.374
HSUL12D_CAL STRENGTH "0.1" MODE "S"	1.754	0.374
POD12_CAL MODE"F"	1.562	0.479
POD12_CAL MODE"M"	1.632	0.479
POD12_CAL MODE"S"	1.697	0.479
POD12D_CAL MODE"F"	1.562	0.374
POD12D_CAL MODE "M"	1.632	0.374
POD12D_CAL MODE"S"	1.697	0.374
HSTL12_I_CAL, STRENGTH "6.3" MODE "F"	1.46	0.56
HSTL12_I_CAL, STRENGTH"6.3"MODE"M"	1.51	0.56
HSTL12_I_CAL, STRENGTH"6.3" MODE"S"	1.56	0.56
HSTL12D_I_CAL, STRENGTH"6.3" MODE"F"	1.46	0.374
HSTL12D_I_CAL, STRENGTH"6.3" MODE"M"	1.51	0.374
HSTL12D_I_CAL, STRENGTH"6.3" MODE"S"	1.56	0.374

Note: The timing parameters of specific usage scenarios are subject to the software timing report

5. Performance parameters under typical working conditions (Fabric Performance)

This chapter lists the performance characteristics that implement common applications of Titan2 series FPGAs .

5.1. LVDS performance parameters（LVDS Performance）

Table 5-1 HR I /O LVDS highest performance

Description	Maximum rate	Unit	IO resource
	- 2		
SDR LVDS Transmitter	500	Mbps	OSERDES(DATA _WIDTH =4 TO 8)
DDR LVDS Transmitter	1000	Mbps	OSERDES(DATA _WIDTH =4 TO 8)
SDR LVDS Receiver	500	Mbps	ISERDES(DATA _WIDTH =4 TO 8)
DDR LVDS Receiver	1000	Mbps	ISERDES(DATA _WIDTH =4 TO 8)

Table 5- 2 HP I/O LVDS highest performance

Description	Maximum rate	Unit	IO resource
	- 2		
SDR LVDS Transmitter	700	Mbps	OSERDES(DATA _WIDTH =4 TO 8)
DDR LVDS Transmitter	1400	Mbps	OSERDES(DATA _WIDTH =4 TO 8)
SDR LVDS Receiver	700	Mbps	ISERDES(DATA _WIDTH =4 TO 8)
DDR LVDS Receiver	1400	Mbps	ISERDES(DATA _WIDTH =4 TO 8)

5.2. Memory interface performance parameters（Memory Interface Performance）

Table 5-3 HPI/O Storage Interface Maximum Performance

Description	Maximum rate	Unit
	- 2	
DDR4	1866	Mbps
DDR3	TBD	Mbps
DDR3L	TBD	Mbps
DDR2	TBD	Mbps
QDRII+	TBD	MHz
RLDRAM3	TBD	MHz
RLDRAM	TBD	MHz

Table 5-4 HR I/O Storage Interface Highest Performance

Description	Maximum rate	Unit
	- 2	
DDR3	TBD	Mbps
DDR3L	TBD	Mbps
DDR2	TBD	Mbps
LPDDR	TBD	Mbps
QDRII+	TBD	MHz
RLDRAM2	TBD	MHz

5.3. DRM（Dedicated RAM Module）performance parameters

Table 5-5 DRM highest performance

Pattern	Maximum frequency (MHz)
	- 2
DRM(NW mode & read register enable)	450
DRM(TW mode & read register enable)	500
DRM (RBW mode & read register enable)	430
DRM (synchronous FIFO mode & read register enable)	450
DRM (ECC mode)	380

5.4. APM（Arithmetic Process Module）performance parameters

Table 5- 6 APM highest performance

Condition	Maximum frequency (MHz)
	- 2
All registers used (uses the registers of each level of the APM)	460
Only use INREG and PREG (use only APM's input and output registers)	190

6. Analog-to-Digital Converter (ADC) Characteristics

This chapter mainly introduces the characteristic parameters of the ADC hard core of Titan2 series FPGA , as shown in the following table.

Table 6-1 ADC Hard Core Features

Parameter	Minimum	Typical value	Maximum value	Unit	Description / condition	
VCCADC = 1.8V ±5%, VREFADC_P= 1.255V, VREFADC_N= 0V, ADC_CLK_OUT = 26 MHz, Tj:–40°C ~125°C, dedicated channel; Typical values at Tj=+40°C Vinp -p=-0.45dB Full Scale ;						
VCCADC	1.71	1.8	1.89	V	Analog supply voltage	
Resolution	12	- -	- -	Bits	Resolution	
Sample Rate	- -	- -	1	MSPS	Sampling Rate	
Channel	- -	- -	12		aisle	
Voltage Reference	1.205	1.255	1.305	V	External reference voltage	
	1.230	1.255	1.280	V	Internal reference voltage	Ground VREFADC_P pin to AGND, –40°C≤ Tj ≤125°C
Offset Error	- -	- -	±4	LSB	Bipolar	–40°C≤ Tj <125°C
	- -	- -	±12	LSB	Unipolar	–40°C≤ Tj ≤125°C
Gain Error	- -	±1	- -	%FS	Gain error Gain error after calibration	
DNL	- -	- -	- 1<DNL<5	LSB	Differential Nonlinear ; Nomissing codes	
INL	- -	- -	±4	LSB	Integeral Nonlinear	–40°C≤ T_j ≤125°C
SNR_1		58	- -	dB	Signal to Noise Ratio	F_{SAMPLE} = 500KS/s, F_{IN} = 20kHz dedicated channel

SNR_2		58		dB	Signal to Noise Ratio	F_{SAMPLE} = 500KS/s, F_{IN} = 20kHz Auxiliary channel
THD_1	--	64		dB	2nd – to 7th – total harmonic distortion	F_{SAMPLE} = 500KS/s, F_{IN} = 20kHz dedicated channel
THD_2	--	62		dB	2nd – to 7th – total	F_{SAMPLE} = 500KS/s, F_{IN} = 20 kHz Auxiliary channel
Temperature Sensor Accuracy	--	--	±4	°C	Temperature detection accuracy	–40°C≤ Tj ≤100°C
	--	--	±6	°C		100°C< Tj ≤125°C

Note: 1. The typical data in the table above are the test results of different bias voltages at room temperature;
2. The ADC samples the auxiliary IO channel, and the auxiliary IO needs to be constrained in the 1.8V power domain;

7. High Speed Serial Transceiver (HSSTHP) features

This chapter mainly introduces the characteristics of the HSSTHP hard core of the Titan2 series FPGA , including the absolute limit rated voltage / current, recommended operating conditions, AC / DC characteristics, and the characteristics that support typical protocol operating modes.

7.1. HSSTHP hard core absolute limit voltage, current rating

Table 7-1 HSSTHP absolute limit voltage, current rating

Name	Minimum	Maximum value	Unit	Description
HSSTAVCC	–0.5	1.1	V	HSST analog power supply 1.0V voltage
HSSTAVCCPLL	–0.5	1.32	V	HSST PLL analog power supply 1.2V voltage
HSSTVCCA	–0.5	1.935	V	HPLL auxiliary analog power supply voltage for HSST

Note: Exceeding the above limit ratings may cause permanent damage to the device.

7.2. HSSTHP Hardcore Recommended Operating Conditions

The following table lists the recommended operating voltage of the HSSTHP hard core for Titan2 series FPGAs.

Table 7-2 HSSTHP Hardcore Recommended Operating Conditions

Name	Minimum	Typical value	Maximum value	Unit	Description
Voltage value					
HSSTAVCC (1)	0.97	1.0	1.03	V	Analog supply voltage for HSST transmit and receive circuits (HSSTHP HPLL VCO frequency less than or equal to 10.3125Ghz)
	1.02	1.05	1.08	V	Analog supply voltage for HSST transmit and receive circuits (HPLL of HSSTHP VCO frequency greater than 10.3125Ghz)
HSSTAVCCPLL	1.17	1.2	1.23	V	HSST PLL analog power supply 1.2V voltage
HSSTVCCA	1.75	1.8	1.85	V	HPLL auxiliary analog power supply voltage for HSST

7.3. HSSTHP hard core DC characteristic parameters

Table 7-3 HSSTHP hard core DC characteristics

Name	Min	Typical	Max	Unit	Condition	Description
Input and output signal DC characteristics						
HSST_V DINPP	180	-	1000	mV	External AC Coupling	Differential input peak-to-peak voltage
HSST_V DOUTPP	900	-	-	mV	Swing setting max	Differential output peak-to-peak power pressure
HSST_V OUTCMDC	HSSTAVCC–HSST_V DOUTPP /4			mV	The DC common mode output voltage is the case when the transmitting end is floating	
HSST_V OUTCMAC	1/2 HSSTAVCC			mV	Common Mode Output Voltage Value: External AC Coupling	
HSST_R DIN	-	100	-	Ω	Differential input resistance	
HSST_R DOUT	-	100	-	Ω	Differential output resistance	
HSST_TX SKEW	-	-	14	ps	P -side and N -side skew of Tx output	
HSST_C DEXT	-	100	-	nF	Recommended External AC Coupling Capacitor Values	
Reference Clock Input DC Characteristics						
HSST_V RCLKPP	400	-	2000	mV	Differential input peak-to-peak voltage	
HSST_R RCLK	150	220	400	Ω	Differential input resistance	
HSST_C RCLKEXT	-	100	-	nF	Recommended External AC Coupling Capacitor Values	

7.4. AC Characteristics of High Speed Serial Transceiver HSSTHP

HSSTHP hard core are shown in Table 7-4 to Table 7-9 .

Table 7-4 HSST hard core performance parameters

Name	Numerical value			Unit	Description
	-5	-6	-7		
HSST_Fmax	TBD	12.5	TBD	Gbps	HSST maximum data rate
HSST_Fmin	TBD	0.6	TBD	Gbps	HSST minimum data rate
HSST_Fhpllmax	TBD	8	TBD	GHz	HSST Maximum frequency of HPLL
HSST_Fhpllmin	TBD	4.5	TBD	GHz	HSST Minimum frequency of HPLL
HSST_Flpllmax	TBD	6.6	TBD	GHz	HSST Maximum frequency of LPLL
HSST_Flpllmin	TBD	1.6	TBD	GHz	HSST Minimum frequency of LPLL

The HSSTHP reference clock switching characteristics are shown in the table below .

Table 7-5 HSSTHP Hard Reference Clock Switching Characteristics

Name	Numerical value			Unit	Condition	Description
	Min	Typical value	Max			
HSST_F REFCLK	60	-	800	MHz	Reference clock frequency range	
HSST_TRCLK	-	225	-	ps	20%-80%	Reference Clock Rise Time

HSST_T_{FCLK}	-	225	-	ps	80%-20%	Reference clock fall time
HSST_T_{RATIO}	45	50	55	%	PLL	Reference clock duty cycle

Table 7- 6 HSSTHP hard core PLL/Lock lock time characteristics

Name	Numerical value			Unit	Condition	Description
	Min	Typical value	Max			
HSST_$T_{PLLLOCK}$	-	-	2.5	ms		PLL lock time, time from reset release to lock
HSST_$T_{CDRLOCK}$	-	60,000	2,500,000	UI [1]	After the PLL is locked to the reference clock, and after switching to the external input data, the time for the CDR to lock	CDR lock time

Note: 1.UI : Unit Interval unit time interval

HSST hard core user clock switch characteristics are shown in the following table

Table 7-7 HSSTHP Hard User Clock Switch Features

Name	Frequency		Unit	Description
Data Interface Clock Switch Characteristics				
HSST_F_{T2C}	412.5	MHz	Maximum frequency of P_CLK2CORE_TX	
HSST_F_{R2C}	412.5	MHz	Maximum frequency of P_CLK2CORE_RX	
HSST_F_{TFC}	412.5	MHz	Maximum frequency of P_TX_CLK_FR_CORE	
HSST_F_{RFC}	412.5	MHz	Maximum frequency of P_RX_CLK_FR_CORE	
APB Dynamic configuration interface clock switch characteristics				
HSST_F_{APB}	100	MHz	APB CLK maximum frequency	

The characteristics of the HSST hard-core Transmitter transmit side switch are shown in the table below.

Table 7-8 HSSTHP hard core Transmitter transmit side switch characteristics

Name	Min	Typical	Max	Unit	Condition	Description
HSST_T_{TXR}	-	40	-	ps	20%-80%	TX Rise Time
HSST_T_{TXF}	-	40	-	ps	80%-20%	TX fall time
HSST_T_{CHSKEW} (1)	-	-	500	ps	-	TX Skew between channels
HSST_$V_{TXIDLEAMP}$	-	-	25	mV	-	Electrical idle Amplitude
HSST_$V_{TXIDLETIME}$	-	-	250	ns	-	Electrical idle transition time

HSST_TJ 0.6G（LPLL）(2)	-	-	0.10	UI	0.6Gbps	Total Jitter
HSST_DJ 0.6G (LPLL) (2)	-	-	0.03	UI		Deterministic Jitter
HSST_TJ 1.25G (HPLL) (3)	-	-	0.15	UI	1.25Gbps	Total Jitter
HSST_DJ 1.25G (HPLL) (3)	-	-	0.06	UI		Deterministic Jitter
HSST_TJ 2.5G (HPLL) (3)	-	-	0.20	UI	2.5Gbps	Total Jitter
HSST_DJ 2.5G (HPLL) (3)	-	-	0.08	UI		Deterministic Jitter
HSST_TJ 3.125G (HPLL) (3)	-	-	0.32	UI	3.125Gbps	Total Jitter
HSST_DJ 3.125G (HPLL) (3)	-	-	0.16	UI		Deterministic Jitter
HSST_TJ 5.0G (HPLL) (3)	-	-	0.3	UI	5.0Gbps	Total Jitter
HSST_DJ 5.0G(HPLL) (3)	-	-	0.15	UI		Deterministic Jitter
HSST_TJ 8G (HPLL) (3)	-		0.32	UI	8Gbps	Total Jitter
HSST_DJ 8G (HPLL) (3)	-		0.17	UI		Deterministic Jitter
HSST_TJ 10.3125G (HPLL) (3)	-		0.28	UI	10.3125Gbps	Total Jitter
HSST_DJ 10.3125G (HPLL) (3)	-		0.17	UI		Deterministic Jitter
HSST_TJ 12.5G (HPLL) (3)	-		0.32	UI	12.5Gbps	Total Jitter
HSST_DJ 12.5G (HPLL) 3)	-		0.17	UI		Deterministic Jitter

Notes: 1. Channels use the same input reference clock, enable channel bonding function;

2. The 0.6Gbps test condition is LPLL feedback frequency division ratio =16 ;

3. Other code rate test conditions are HPLL feedback divider ratio =64 .

The switch characteristics on the receiving side of the HSST hard-core Receiver are shown in the following table.

Table 7-9 Receiver side switch characteristics of HSSTHP hard core Receiver

Name	Minimum	Typical	Maximum	Unit	Description
HSST_RX TRACK	-5000	-	5000	ppm	Receiver spread spectrum follow, modulation frequency 33kHz
HSST_RX LENGTH	-	-	512	UI	Support RX continuous long 0 or long 1 length
HSST_RX TOLERANCE	-1000	-	1000	ppm	Frequency offset tolerance of data / reference clock
Sinusoidal Jitter Tolerance					
HSST_SJ 2.5（LPLL）	0.45	-	-	UI	Sinusoidal Jitter (1), 2.5Gbps
HSST_SJ 3.2（LPLL）	0.45	-	-	UI	Sinusoidal Jitter (1), 3.2Gbps
HSST_SJ 3.75（LPLL）	0.44	-	-	UI	Sinusoidal Jitter (1), 3.75Gbps
HSST_SJ 4.25（LPLL）	0.44	-	-	UI	Sinusoidal Jitter (1), 4.25Gbps
HSST_SJ 5.0（LPLL）	0.35	-	-	UI	Sinusoidal Jitter (1), 5.0Gbps
HSST_SJ 6.6（LPLL）	0.44	-	-	UI	Sinusoidal Jitter (1), 6.6Gbps

HSST_SJ $_{6.6\ (HPLL)}$	0.35	-	-	UI	Sinusoidal Jitter (1), 6.6Gbps
HSST_SJ $_{8.0\ (HPLL)}$	0.44	-	-	UI	Sinusoidal Jitter (1), 8.0Gbps
HSST_SJ $_{9.8\ (HPLL)}$	0.3	-	-	UI	Sinusoidal Jitter (1), 9.8Gbps
HSST_SJ $_{9.98\ (HPLL)}$	0.3	-	-	UI	Sinusoidal Jitter (1), 9.98Gbps
HSST_SJ $_{10.3125\ (HPLL)}$	0.3	-	-	UI	Sinusoidal Jitter (1), 10.3125Gbps
HSST_SJ $_{11.18\ (HPLL)}$	0.3	-	-	UI	Sinusoidal Jitter (1), 11.18Gbps
HSST_SJ $_{12.5\ (HPLL)}$	0.3	-	-	UI	Sinusoidal Jitter (1), 12.5Gbps

Note: The frequency of the injected sinusoidal jitter is 80MHz , and the test pattern is PRBS31

8. PCIe Hard Core Features

Table 8-1 PCIe performance parameters

Name	Numerical value	unit	Description
Fpclk	250	MHz	PCIe core maximum clock frequency
Fpclk_div2	125	MHz	HSST interface maximum clock frequency
Fuserclk	125	MHz	User interface maximum clock frequency