1000BASE-T Copper Transceiver
Small Form Pluggable (SFP), 3.3V
1.25Gbps Gigabit Ethernet

Features

- Hot-pluggable SFP Footprint
- Fully Metallic Enclosure for Low EMI
- Low Power Dissipation
- Compact RJ-45 Connector Assembly
- Detailed Product Information in EEPROM
- +3.3V Single Power Supply
- Access to Physical Layer IC via 2-wire serial bus
- Support 10/100/1000 BASE-T with SGMII Interface
- Compliant with SFP MSA
- Compliant with IEEE Std 802.3-2002
- Compliant with FCC 47 CFR Part 15, Class B
- Compliant with RoHs.
- Temperature range: 0°C to +70°C or -40°C to +85°C

Application

- 10/100/1000Mbps Ethernet over Category 5 Cable
- Distributed multi-processing
- High speed I/O for file server or high-end workstation
- Switch/Router to Switch/Router Link

Description

The Copper SFP Transceiver 10/100/1000Base-T or 1000Base-T only SFP Copper Transceiver named as ASFPT is high performance, cost effective module, compliant with the Gigabit Ethernet and 1000BASE-T standards as specified in IEEE 802.3-2002 and IEEE 802.3ab, which supports 1000Mb/s data-rate up to 100 meters reach over twisted-pair category 5 cable. ASFPT supports 1000Mb/s full duplex data-links with 5-level Pulse Amplitude Modulation (PAM) signals. All four pairs in the cable are used with symbol rate at 250Mb/s on each pair.

In addition, ASFPT provides standard serial ID information compliant with SFP MSA, which can be accessed with address of A0H via the 2-wire serial CMOS EEPROM protocol. The physical IC can also be accessed via 2-wire serial bus at address ACH. The address of the PHY IC is 1010110x, where x represents the read or write bit.

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Ordering Information

PART NUMBER	MAC Interface	Speed / Mode / Temperature
ASFPT-T1C	1.25Gbps SerDes	1000 Mbps only, LOS Enable, 0°C to +70°C
ASFPT-T2C	1.25Gbps SerDes	1000 Mbps only, LOS Disable, 0°C to +70°C
ASFPT-T3C	SGMII without clock	10/100/1000 Mbps, LOS Enable, 0°C to +70°C
ASFPT-T4C	SGMII without clock	10/100/1000 Mbps, LOS Disable, 0°C to +70°C
ASFPT-T1C-I	1.25Gbps SerDes	1000 Mbps only, LOS Enable, -40°C to +85°C
ASFPT-T2C-I	1.25Gbps SerDes	1000 Mbps only, LOS Disable, -40°C to +85°C
ASFPT-T3C-I	SGMII without clock	10/100/1000 Mbps, LOS Enable, -40°C to +85°C
ASFPT-T4C-I	SGMII without clock	10/100/1000 Mbps, LOS Disable, -40°C to +85°C

Notes:

ASFPT-T3C, ASFPT-T4C, ASFPT-T3C-I and ASFPT-T4C-I 10/100/1000 Mbps operation requires the host system to have an SGMII interface without clocks, and auto-negotiation advertise all capabilities 10/100/1000 Mbps

ASFPT-T1C, ASFPT-T2C, ASFPT-T1C-I and ASFPT-T2C-I 1000 Mbps with a SerDes interface that does not support SGMII, the module will operate at 1000 Mbps only.

SGMII is a mode of communication between the MAC and PHY to allow for 10/100/1000BASE-T operation. In 100BASE-TX mode, the MAC still transmits to the PHY at 1.25 Gb/sec, but each byte is repeated 10 times. The PHY then converts this repeated data to 100BASE-TX format. The process is the same in 10BASE-T mode but each byte is repeated 100 times.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature (Ambient)	*Ts*	-45	90	°C	
Storage Humidity	*Hs*	5	95	%	

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Operating Temperature (Case)	T_C	0	70	°C	ASFPT-TxC
Operating Temperature (Case)	T_I	-40	85	°C	ASFPT-TxC-I
Operating Humidity	*Ho*	10	85	%	
Supply Voltage	V_{CC}	3.14	3.47	V	Typ. 3.3V
Power Consumption	*P*	-	1.2	W	
Supply Current	I_{CC}	-	375	mA	
Surge Current	I_{surge}	-	30	mA	Hot Plug

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General Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Distance	C_L	-	100	m	Category 5 UTP, BER <10^{-12}
Data Rate	*BR*	10	1000	Mbps	

Electrical Characteristics

V_{CC} = 3.3 V, T = -40 °C to +85 °C

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Transmitter						
Data Input Swing (Single ended)	$V_{D,TX}$	250	-	1200	mV	1
Differential Input Impedance	Z_{TX}	-	100	-	Ohm	
Transmitter Disable Input-High	V_{DISH}	2.0	-	V_{cc}+0.3	V	2
Transmitter Disable Input-Low	V_{DISL}	0	-	0.8	V	2
Receiver						
Data Output Swing (Single ended)	$V_{D,RX}$	300	-	800	mV	1
Differential Output Impedance	Z_{RX}	-	100	-	Ohm	
Data Output Rise/Fall Time	$T_{R,RX}/T_{F,RX}$	100	175	200	ps	3
LOS Output Voltage – High	V_{SDHL}	V_{cc}-0.5	-	V_{cc}+0.3	V	2
LOS Output Voltage – Low	V_{SDL}	0	-	0.5	V	2

Note:
1) Internally AC coupled, but requires a 100 Ohms differential termination at MAC side.
2) Pull up to V_{CC} with a 4.7K – 10K Ohms resistor on host Board
3) 20% ~ 80% values

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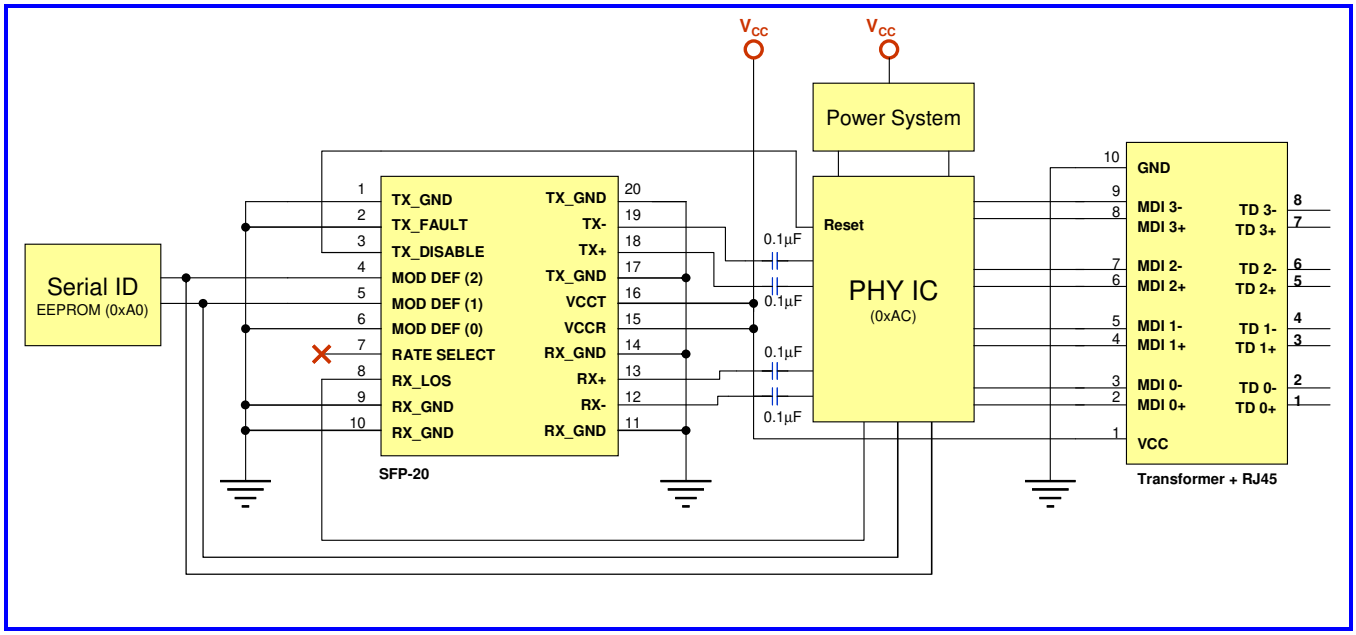
Block Diagram of Transceiver



LOS Function

The SFP MSA specification defines a pin called LOS to indicate loss of signal to the motherboard. This should be pulled up with a 4.7K to 10K resistor. Pull up voltage between 2.0V and Vcc-T/R+0.3V. When high, this output indicates link fail. Low indicates normal operation. In the low state, the output will be pulled to <0.8V.

Termination Circuits

Inputs to the transceiver are AC coupled and internally terminated through 50 Ohms. These modules can operate with PECL or ECL logic levels. The input signal must have at least a 250mV peak-to-peak (single ended) signal swing. Output from the receiver section of the module is also AC coupled and is expected to drive a 50 Ohms load. Different termination strategies may be required depending on the particular Serializer/Deserializer chip set used. The transceiver is designed with AC coupled data inputs and outputs to provide the following advantages:

Close positioning of SerDes with respect to transceiver; allows for shorter line lengths and at Gigabit speeds reduces EMI. It has minimum number of external components. Internal termination reduces the potential for un-terminated stubs which would otherwise increase jitter and reduce transmission margin.

Subsequently, this affords the customer the ability to optimally locate the SerDes as close to the transceiver as possible and save valuable real estate. At Gigabit rates this can provide a significant advantage resulting in better transmission performance and accordingly better signal integrity.

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Power Coupling

A suggested layout for power and ground connections is given in Figure 1 below. Connections are made via separate voltage and ground planes. The mounting posts are at case ground and should not be connected to circuit ground. The ferrite bead should provide a real impedance of 50 to 100 Ohms at 100 to 1000 MHz. Bypass capacitors should be placed as close to the 20 pin connector as possible.

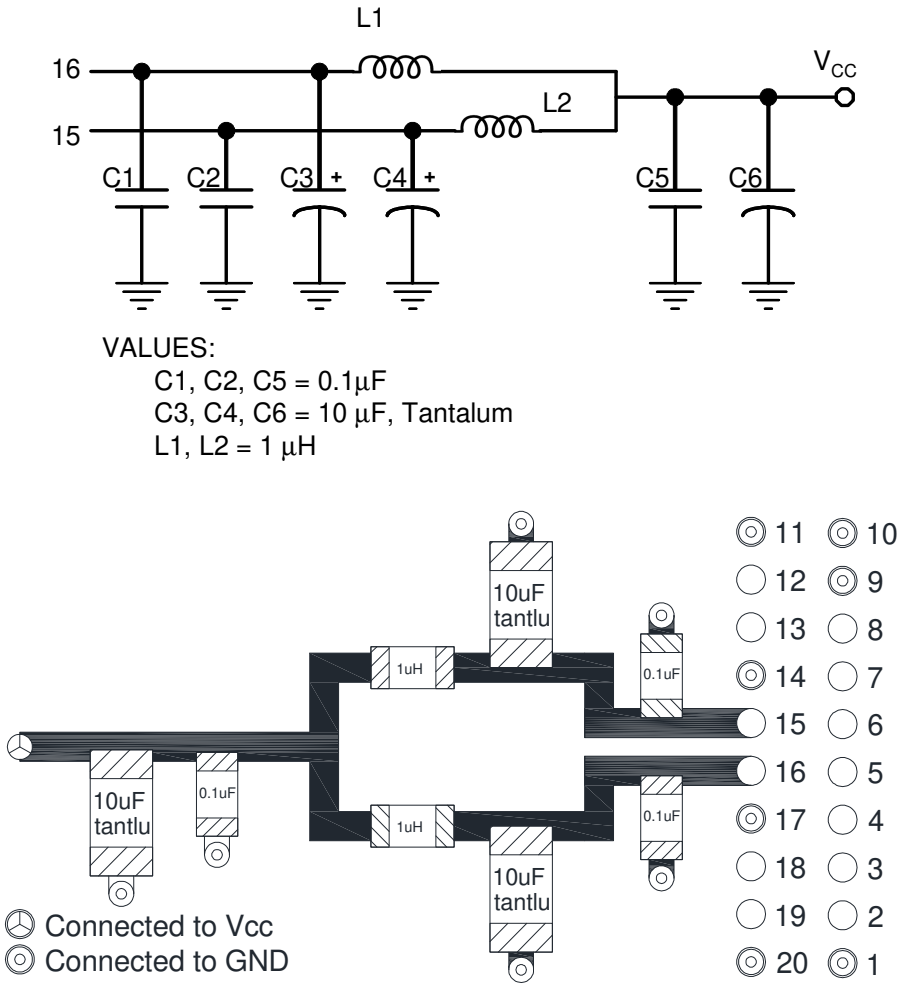

Figure 1: Suggested Power Coupling

Serial Communication Protocol

ASFPT-TxC supports the 2-wire serial communication protocol defined in the SFP MSA and uses a 256-byte EEPROM with an address of A0H to store Table 1 data. The PHY IC can also be accessed via the 2-wire serial bus at address ACH.

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EEPROM Serial ID Memory Contents

Accessing Serial ID Memory uses the 2 wire address 10100000 (A0H). Memory Contents of Serial ID are shown in Table 1.

Table 1 Serial ID Memory Contents

Addr.	Size (Bytes)	Name of Field	Hex	Description
0	1	identifier	03	SFP or SFP+
1	1	Ext.Identifier	04	GBIC/SFP function is defined by two-wire interface ID only
2	1	Connector	22	RJ45
3-10	8	Transceiver	00 00 00 08 00 00 00 00	Transceiver Code
11	1	Encoding	01	8B/10B
12	1	BR(Nominal)	0D	1300Mbps
13	1	Rate Identifier	00	Unspecified
14	1	Length(SMFm)-km	00	N/A
15	1	Length(SMF)	00	N/A
16	1	Length(50μm)	00	N/A
17	1	Length(62.5μm)	00	N/A
18	1	Length(cable)	64	100(units of meters)
19	1	Length(OM3)	00	N/A
20-35	16	Vendor name	XX XX XX XX XX XX XX 20 20 20 20 20 20 20 20 20	Vendor name (ASCII)
36	1	Transceiver	00	Unallocated
37-39	3	Vendor OUI	XX XX XX	Vendor OUI
40-55	16	Vendor PN	XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX	Transceiver part number
56-59	4	Vendor rev	XX XX XX XX	Vendor rev
60-61	2	Wavelength	00	0nm
62	1	Unallocated	00	Unallocated
63	1	CC_BASE	Check Sum (Variable)	Check code for Base ID Fields
64-65	2	Options	00 12	TX_Disable and LOS implemented
66	1	BR	00	max
67	1	BR	00	min
68-83	16	Vendor SN	41 34 32 30 33 30 30 34 20 20 20 20 20 20 20 20	Serial Number of transceiver (ASCII). For example“A4203004”.
84-91	8	Date code	XX XX XX XX XX XX XX XX	Manufacture date code
92	1	Diagnostic Monitoring Type	00	N/A
93	1	Enhanced Options	00	N/A
94	1	SFF-8472 Compliance	00	Digital diagnostic function not included or undefined
95	1	CC_EXT	Check Sum (Variable)	Check sum for Extended ID Field.
96-127	32	Vendor Specific	Read only	Depends on customer information

Note: The “XX” byte should be filled in according to practical case. For more information, please refer to the related document of SFP Multi-Source Agreement (MSA).

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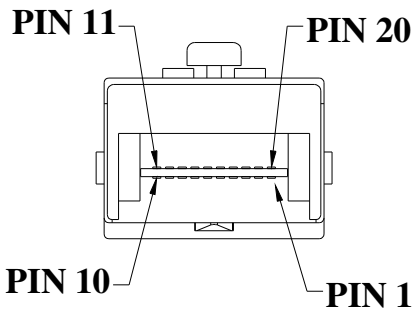
Connection Diagram

Pin-Out



Pin	Signal Name	Function	Descript	Notes
1	VeeT	Transmitter Ground	VeeT and VeeR are connected in SFP.	7
2	TX_FAULT	Transmitter Fault Indication	Not supported.	1
3	TX_DISABLE	Transmitter Disable	Module disables on high or open	2
4	MOD DEF (2)	Module Definition 2	Data Line (SDA) for Serial ID.	3
5	MOD DEF (1)	Module Definition 1	Clock Line (SCL) for Serial ID.	3
6	MOD DEF (0)	Module Definition 0	Grounded within the module	3
7	RATE SELECT	Not Implemented	No connection required.	
8	LOS	Loss of Signal	See LOS option.	
9	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
10	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
11	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
12	RD-	Inverted Received Data out	AC coupled 100 ohm differential high speed data lines.	4
13	RD+	Non-Inverted Received Data out	AC coupled 100 ohm differential high speed data lines.	4
14	VeeR	Receiver Ground	VeeT and VeeR are connected in SFP.	7
15	VccR	Receiver Power	VccR and VccT are connected in SFP.	5
16	VccT	Transmitter Power	VccR and VccT are connected in SFP.	5
17	VeeT	Transmitter Ground	VeeT and VeeR are connected in SFP.	7
18	TD+	Non-inverted Data In	AC coupled 100 ohm differential high speed data lines.	6
19	TD-	Inverted Data In	AC coupled 100 ohm differential high speed data lines	6
20	VeeT	Transmitter Ground	Veet and VeeR are connected in SFP	7

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Notes:

1. TX Fault is not used and is always tied to ground.
2. TX disable is an input that is used to reset the chip of Gigabit Ethernet PHY inside the copper SFP. It is pulled up within the module with a 4.7-10 K Ohms resistor. Disable (PHY IC Disabled) >2V or open, Enable (PHY IC on) < 0.8V.
3. Mod-Def 0, 1, 2 are the module definition pins. They should be pulled up with a 4.7-10K Ohms resistor on the host board to a supply between 2V and 3.6V.
4. RD-/+: These are the differential receiver outputs. They are ac coupled 100 Ohms differential lines which should be terminated with 100 ohm differential at the user SerDes. The ac coupling is done inside the module and is thus not required on the host board. The voltage swing levels are compatible with CML and LVPECL voltage swings.
5. VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.3 V ± 5% at the SFP connector pin.
6. TD-/+: These are the differential transmitter inputs. They are ac coupled differential lines with 100 Ohms differential termination inside the module. The ac coupling is done inside the module and is thus not required on the host board. The inputs levels are compatible with CML and LVPECL voltage swings.
7. Circuit ground is connected to chassis ground.

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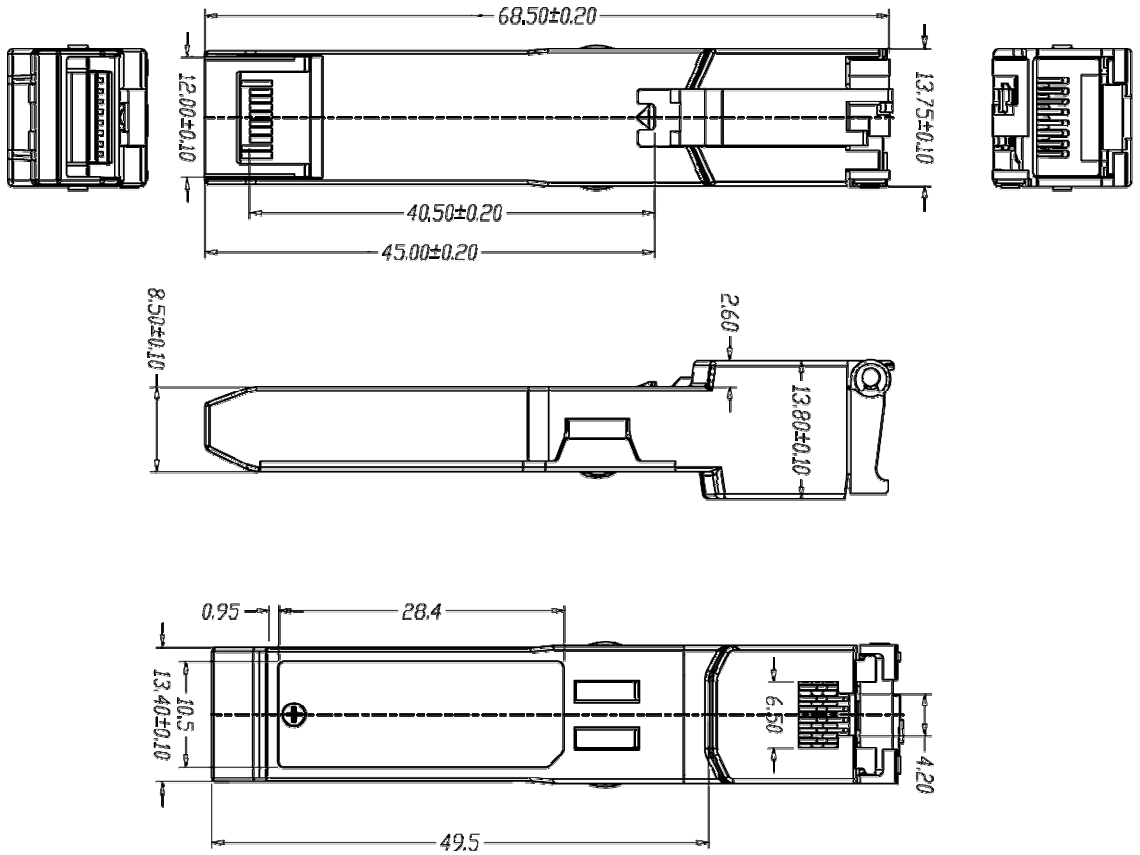
Drawing Dimensions



UNIT: mm

Mating of SFP Transceiver to SFP Host Board Connector

The pads on the PCB of the SFP transceiver shall be designed for a sequenced mating as follows: First mate: Ground contacts. Second mate: Power contacts. Third mate: Signal contacts The SFP MSA specification for a typical contact pad plating for the PCB is 0.38 micrometers minimum hard gold over 1.27 micrometers minimum thick nickel. To ensure the long term reliability performance after a minimum of 50 insertion removal cycles, the contact plating of the transceiver is 0.762 micron (30 micro-inches) over 3.81 micron (150 micro-inches) of Ni on Cu contact pads.

RJ45 Connector

RJ45 connector shall support shielded and unshielded cables. Also, the connector is mechanically robust enough and designed to prevent loss of link, when the cable is positioned or moves in different angles. The connector shall pass the “wiggle” RJ45 connector operational stress test. During the test, after the cable is plugged in, the cable is moved in circle to cover all 360 deg in the vertical plane, while the data traffic is on. There shall be no link or data loss.

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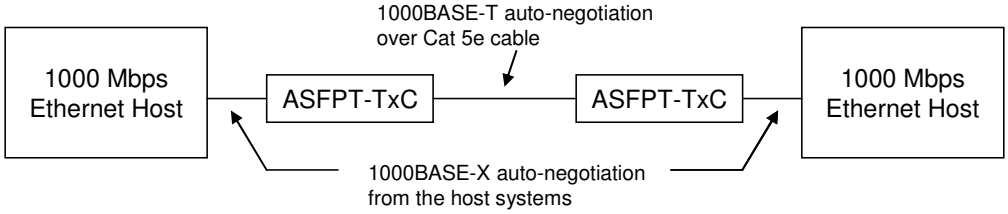
References

1. IEEE standard 802.3, IEEE Standard Department, 2002.
2. Small Form Factor Pluggable (SFP) Transceiver Multi-Source Agreement (MSA), September 2000.
3. Marvell Corporation – Alaska Ultra 88E1111 Integrated 10/100/1000 Gigabit Ethernet Transceiver.

Appendix:

Host machine can directly access PHY register to change the ASFPT operation mode via 2-wire serial bus. The PHY slave address is 0xAC. Some configurations are listed as the following table.



1. 10/100/1000BASE-T Enable (SGMII interface setting)

Register Address	Write Data	Description
0x1B	0x9084	Enable SGMII mode
0x09	0x0F00	Advertise 1000BASE-T Full/Half-Duplex
0x00	0x8140	Apply Software Reset
0x04	0x0DE1	Advertise 100/10BASE-T Full/Half-Duplex
0x00	0x9140	Apply Software Reset and enable auto-negotiation

2. 1000Base-X Disable

Register Address	Write Data	Description
0x1B	0x808C	Change HWCFG_MODE to non-GBIC
0x00	0x8140	Apply Software Reset and disable auto-negotiation

3. 1000Base-X Enable (SerDes interface setting)

Register Address	Write Data	Description
0x1B	0x9088	Change HWCFG_MODE to GBIC
0x00	0x8140	Apply Software Reset and disable auto-negotiation

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4. 1000Base-T Disable

Register Address	Write Data	Description
0x16	0x0001	Select Fiber Register Bank
0x00	0x8140	Disable Auto-negotiation
0x16	0x0000	Return to Copper Register Bank

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