MMY DDR4   4GB-2133 / 2400 / 2666 / 2933 / 3200   SO-DIMM

GENERAL DESCRIPTION

This chapter gives an overview of the 260–pin SO DDR4 Dual-In-Line memory modules product family and describes its main characteristics.

FEATURES

1. 260-Pin SO-DIMM (Lead-Free) DDR4 SDRAM Memory Module.
2. Data transfer rates: . PC4-17000/19200/21300/23400/25600.
3. Power supply: V_{DD}: 1.20V ± 0.06V
4. Module organization: 512Meg × 64.
   Chip organization: 512M × 8.
5. Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
6. Low-power auto self refresh (LPASR)
7. Data bus inversion (DBI) for data bus
8. On-die VREFDQ generation and calibration
9. On-board I^2 serial presence-detect (SPD) EEPROM
10. 16 internal banks; 4 groups of 4 banks each
11. Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
12. Selectable BC4 or BL8 on-the-fly (OTF)
13. Fly-by topology
14. Terminated control command and address bus
15. Operating Temperature : 0 ºC ~ 85 ºC
16. Storage Temperature : -55 ºC ~ 100 ºC

Ordering Information for Compliant Products

Product Type	Compliance Code	Description	DRAM Organisation	# of SDRAMs
MM4S4GC3PG-2133C-A00	4GB, PC4 - 17000, 15-15-15	1 Rank, Non-ECC	512Mx8	8
MM4S4GC3PG-2400C-A00	4GB, PC4 - 19200, 17-17-17	1 Rank, Non-ECC	512Mx8	8
MM4S4GC3PG-2666C-A00	4GB, PC4 - 21300, 19-19-19	1 Rank, Non-ECC	512Mx8	8
MM4S4GC3PG-2933C-A00	4GB, PC4 - 23400, 21-21-21	1 Rank, Non-ECC	512Mx8	8
MM4S4GC3PG-3200C-A00	4GB, PC4 - 25600, 22-22-22	1 Rank, Non-ECC	512Mx8	8

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Pinout

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	67	DQ29	133	A1	199	DM5_n/ DBI5_n	2	V_{SS}	68	V_{SS}	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	V_{SS}	135	V_{DD}	201	V_{SS}	4	DQ4	70	DQ24	136	V_{DD}	202	V_{SS}
5	V_{SS}	71	DQ25	137	CK0_t	203	DQ46	6	V_{SS}	72	V_{SS}	138	CK1_t/NF	204	DQ47
7	DQ1	73	V_{SS}	139	CK0_c	205	V_{SS}	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	V_{SS}
9	V_{SS}	75	DM3_n/ DBI3_n	141	V_{DD}	207	DQ42	10	V_{SS}	76	DQS3_t	142	V_{DD}	208	DQ43
11	DQS0_c	77	V_{SS}	143	PARITY	209	V_{SS}	12	DM0_n/ DBI0_n	78	V_{SS}	144	A0	210	V_{SS}
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	V_{SS}	80	DQ31	146	A10/AP	212	DQ53
15	V_{SS}	81	V_{SS}	147	V_{DD}	213	V_{SS}	16	DQ6	82	V_{SS}	148	V_{DD}	214	V_{SS}
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	V_{SS}	84	DQ27	150	BA0	216	DQ48
19	V_{SS}	85	V_{SS}	151	WE_n/ A14	217	V_{SS}	20	DQ2	86	V_{SS}	152	RAS_n/ A16	218	V_{SS}
21	DQ3	87	CB5/NC	153	V_{DD}	219	DQS6_c	22	V_{SS}	88	CB4/NC	154	V_{DD}	220	DM6_n/ DBI6_n
23	V_{SS}	89	V_{SS}	155	ODT0	221	DQS6_t	24	DQ12	90	V_{SS}	156	CAS_n/ A15	222	V_{SS}
25	DQ13	91	CB1/NC	157	CS1_n	223	V_{SS}	26	V_{SS}	92	CB0/NC	158	A13	224	DQ54
27	V_{SS}	93	V_{SS}	159	V_{DD}	225	DQ55	28	DQ8	94	V_{SS}	160	V_{DD}	226	V_{SS}
29	DQ9	95	DQS8_c	161	ODT1	227	V_{SS}	30	V_{SS}	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/NC	228	DQ50
31	V_{SS}	97	DQS8_t	163	V_{DD}	229	DQ51	32	DQS1_c	98	V_{SS}	164	V_{REFCA}	230	V_{SS}
33	DM1_n/ DBI_n	99	V_{SS}	165	C1, CS3_n, NC	231	V_{SS}	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	V_{SS}	101	CB2/NC	167	V_{SS}	233	DQ61	36	V_{SS}	102	V_{SS}	168	V_{SS}	234	V_{SS}
37	DQ15	103	V_{SS}	169	DQ37	235	V_{SS}	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	V_{SS}	105	CB3/NC	171	V_{SS}	237	DQ56	40	V_{SS}	106	V_{SS}	172	V_{SS}	238	V_{SS}
41	DQ10	107	V_{SS}	173	DQ33	239	V_{SS}	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	V_{SS}	109	CKE0	175	V_{SS}	241	DM7_n/ DBI7_n	44	V_{SS}	110	CKE1	176	V_{SS}	242	DQS7_t
45	DQ21	111	V_{DD}	177	DQS4_c	243	V_{SS}	46	DQ20	112	V_{DD}	178	DM4_n/ DBI4_n	244	V_{SS}
47	V_{SS}	113	BG1	179	DQS4_t	245	DQ62	48	V_{SS}	114	ACT_n	180	V_{SS}	246	DQ63
49	DQ17	115	BG0	181	V_{SS}	247	V_{SS}	50	DQ16	116	ALERT_n	182	DQ39	248	V_{SS}
51	V_{SS}	117	V_{DD}	183	DQ38	249	DQ58	52	V_{SS}	118	V_{DD}	184	V_{SS}	250	DQ59
53	DQS2_c	119	A12	185	V_{SS}	251	V_{SS}	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	V_{SS}
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	V_{SS}	122	A7	188	V_{SS}	254	SDA
57	V_{SS}	123	V_{DD}	189	V_{SS}	255	V_{DDSPD}	58	DQ22	124	V_{DD}	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	V_{PP}	60	V_{SS}	126	A5	192	V_{SS}	258	V_{TT}
61	V_{SS}	127	A6	193	V_{SS}	259	V_{PP}	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	V_{DD}	195	DQ40	–	–	64	V_{SS}	130	V_{DD}	196	V_{SS}	–	–
65	V_{SS}	131	A3	197	V_{SS}	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A17[1]	SDRAM address bus	SCL	I^2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0-SA2	I^2C slave address select for SPD-TSE
RAS_n[2]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM I/OO and core power supply
WE_n[4]	SDRAM write enable	C0, C1, C2	Chip ID lines
CS0_n, CS1_n,	DIMM Rank Select Lines	12V	Optional power Supply on socket but not used on UDIMM
CKE0, CEK1	SDRAM clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.		
DQS0_t-DQS8_t	SDRAM data strobes (positive line of differential pair)		
DQS0_c-DQS8_c	SDRAM data strobes (negative line of differential pair)	RESET_n	Set DRAMs to a Known State
DM0_n-DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inersion (x8-based x72 DIMMs)	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	SDRAM clock (positive line of differen- tial pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	SDRAM clock (positive line of differen- tial pair)	RFU	Reserved for future use

- Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs, this connection pin is NC.
- RAS_n is a multiplexed function with A16.
- CAS_n is a multiplexed function with A15.
- WE_n is a multiplexed function with A14.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at hese or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times
5. Overshoot area above 1.5V is specified in DDR4 Device Operation.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

NOTE:
1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications Will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

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Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

NOTE:
◆ Under all conditions VDDQ must be less than or equal to VDD.
◆ VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
◆ DC bandwidth is limited to 20MHz. Recommended DC Operating Conditions

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Physical Dimensions

Front

Side

Back

Detail - A
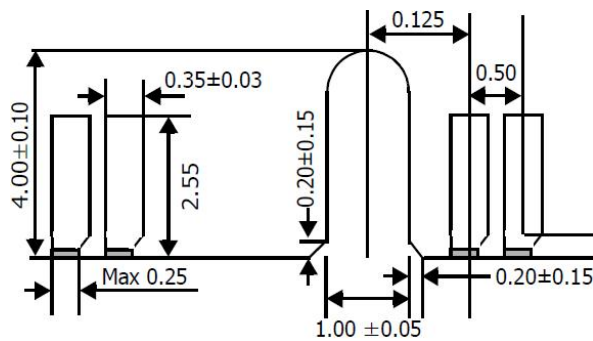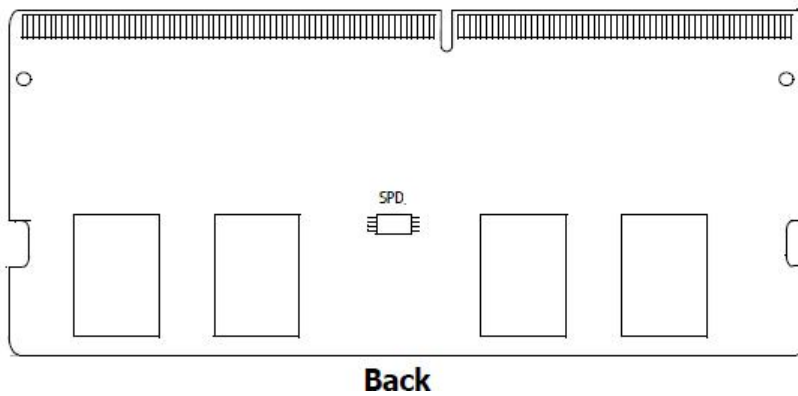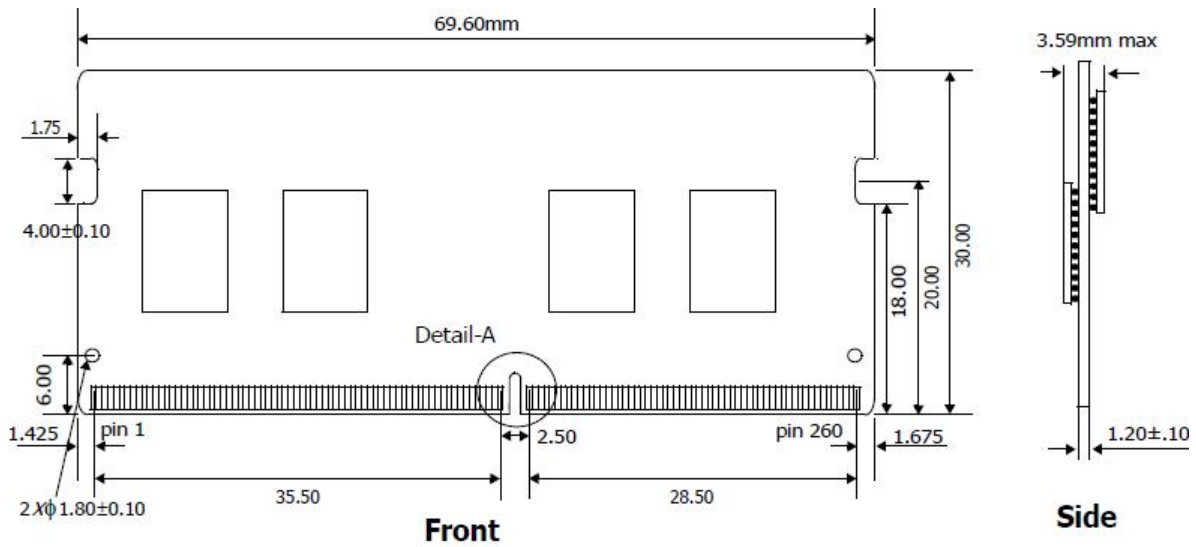
Units : Millimeters

Note: 1. Tolerances on all dimensions ±0.15 unless otherwise specified.
2. The dimensional diagram is for reference only.

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