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RFC350X-AYH-DNN

SPECIFICATION

CUSTOMER:

APPROVED BY

PCB VERSION

DATE

FOR CUSTOMER USE ONLY

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
Release DATE:			

TFT Display Inspection Specification: <u>https://www.raystar-optronics.com/download/products.htm</u> Precaution in use of TFT module: <u>https://www.raystar-optronics.com/download/declaration.htm</u>



Revision History

VERSION	DATE	REVISED PAGE NO.	Note
0	2019/07/29		First issue
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[®]RAYSTAR 1.Module Classification Information

R	F	С	35	0X	-	Α	Y	Н	-	D	Ν	Ν
1	2	3	4	5	-	6	7	8	-	9	10	11

ltem	Description								
1	R : Raystar Optronics Inc.								
2	Display Type : $F \rightarrow TFT$ Type, J \rightarrow Custom TFT								
	Solution: A: 128	x160 B:320x234	C:320x240	D:480x234	E:480x272				
2	F:800x	480 G:640x480	H:1024x600	I:320x480	J:240x320				
3	K:1280)x800 L:240x400	M:1024x768	N:128x128	O:480x800				
	P:640x	(320 Q:800x600	S:480x128	T:800x320					
4	Display Size : 3	5.5" TFT							
5	Version Code.								
	Model Type:								
	A:TFT LCD		6	: TFT+FR					
	E : TFT+FR+C	ONTROL BOARD	н	: TFT+D/V B	OARD				
6	J:TFT+FR+A/I	D BOARD		TFT+FR+D/V	BOARD				
	N : TFT+FR+A/	D BOARD+CONTROI	BOARD B	: TFT+POWEF	R BD				
	S : TFT+FR+P(OWER BOARD (DC	TO DC)						
	1 : TFT+CONT	ROL BOARD	ROL BOARD						
	Polorizor	I→Transmissive, W.	T, 6:00 ; C-	→Transmissive,	N. T, 6:00				
	Fulanzei	L→Transmissive, W	T,12:00; F-	→Transmissive	, N.T,12:00				
7	Type, Tomporaturo	Y→Transmissive,W.	T, IPS TFT ;						
1	rango	A→Transmissive, N.	T, IPS TFT						
	View direction	Z→Transmissive, W	.T, O-TFT						
	view direction	R→Transmissive, S	uper W.T, O-T	FT					
		N→Transmissive, S	uper W.T, 6:00);					
		Q→Transmissive, S	uper W.T, 12:0	00					
		V→Transmissive, Sι	uper W.T, VA ⁻	ΓFT					
0		W:LED, White	H : LE	D, High Light V	Vhite				
8	Backlight	F : CCFL, White							
9	Driver Method	D: Digital A: Ana	log L : LVD	S M:MIPI					
10	lunta effection	N: without control b	oard A : 8	Bit B:16	Bit				
10	Interface	S:SPI Interface R	: RS232 U	USB I: 120	C				
		N : Without TS	S: resistive t	ouch panel					
11	TS	C : capacitive touch	panel capacit	ive touch pane	l (G-F-F)				
		G : capacitive touch	panel(G-G)						



2.Summary

TFT 3.5" is a IPS transmissive type color active matrix TFT liquid crystal display that use amorphous silicon TFT as switching devices. This module is a composed of a TFT_LCD module, It is usually designed for industrial application and this module follows RoHs.



3.General Specifications

- Size: 3.5 inch
- Dot Matrix: 320 x RGBx240(TFT) dots
- Module dimension: 76.84(W) x 63.84(H) x 3.27(D) mm
- Active area: 70.08 x 52.56 mm
- Dot pitch: 0.073 x 0.219 mm
- LCD type: TFT, Normally black, Transmissive
- View Direction: Wide View
- Driver IC: ST7272A or equivalent
- Interface : 24-bit RGB
- Aspect Ratio: 4:3
- Backlight Type: LED,Normally White
- With /Without TP: Without TP
- Surface: Glare

*Color tone slight changed by temperature and driving voltage.



4.1. LCM PIN Definition

Pin	Symbol	Function	Remark
1	LED-	Power for LED backlight cathode	
2	LED-	Power for LED backlight cathode	
3	LED+	Power for LED backlight anode	\mathbf{A}
4	LED+	Power for LED backlight anode	
5	NC(YU)	No connect	
6	NC(XL)	No connect	
7	NC(SPI_IIC_SEL)	No connect	
8	/RESET	Hardware reset	
9	NC(CS)	No connect	
10	NC(SDA)	No connect	
11	NC(SCL)	No connect	
12	B0	Data bus	
13	B1	Data bus	
14	B2	Data bus	
15	B3	Data bus	
16	B4	Data bus	
17	B5	Data bus	
18	B6	Data bus	
19	B7	Data bus	
20	GO	Data bus	
21	G1	Data bus	
22	G2	Data bus	
23	G3	Data bus	
24	G4	Data bus	
25	G5	Data bus	
26	G6	Data bus	
27	G7	Data bus	
28	R0	Data bus	
29	R1	Data bus	



30	R2	Data bus	
31	R3	Data bus	
32	R4	Data bus	
33	R5	Data bus	
34	R6	Data bus	
35	R7	Data bus	
36	HSYNC	Horizontal sync signal, default is negative polarity.	$\overline{}$
37	VSYNC	Vertical sync signal, default is negative polarity.)`
38	DCLK	Dot-clock signal and oscillator source	
39	NC(HDIR)	No connect	
40	NC(VDIR)	No connect	
41	VCC	Power Supply	
42	VCC	Power Supply	
43	NC(YD)	No connect	
44	NC(XR)	No connect	
45	NC(PARA_SERI)	No connect	
46	NC(BIST_EN)	No connect	
47	NC(ENPROG)	No connect	
48	NC	No connect	
49	NC	No connect	
50	NC	No connect	
51	NC(DISP)	No connect	
52	DE	Data input enable. Display access is enabled when DE is "H".	
53	GND	Ground	
54	GND	Ground	



5.Contour Drawing







6.Block Diagram





7.Absolute Maximum Ratings

ltem	Symbol	Min	Тур	Max	Unit
Operating Temperature	TOP	-20	—	+70	°C
Storage Temperature	TST	-30	_	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. $\leq 60^{\circ}$ C, 90% RH MAX. Temp. $> 60^{\circ}$ C, Absolute humidity shall be less than 90% RH at 60° C



8.Electrical Characteristics 8.1. Operating conditions:

ltem	Symbol	Min	Тур	Max	Unit	Remark
Supply Voltage For LCM	VCC	3.0	3.3	4.2	V	-
Supply Current For LCM	ICC		20	30	mA	Note 1

Note 1 : This value is test for VCC =3.3V , Ta=25 $\ ^{\circ}\!\!\! C$ only

8.2. LED driving conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Remark
LED current	-	-	40	-	mA	-
Power Consumption	-	540	600	660	mW	-
LED voltage	LED+	13.5	15	16.5	V	Note 1
LED Life Time	-	-	50,000	× ·	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



Note 2 : Ta = 25 ℃

Note 3 : Brightness to be decreased to 50% of the initial value

Note 4 : The single LED lamp case



9.AC Characteristics

9.1. System Operation AC Characteristics

ltem	Symbol	Min.	Тур.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
						Output settled within
SD Output Stable Time	Tst	-	-	12	us	+20mV Loading =
						6.8k+28.2pF.
CD Output Pise and Fall Time	Tast			6	116	Output settled (5%~95%),
	rysi	-	-	υ	us	Loading = 4.7k+29.8pF

9.2. System Bus Timing for I₂C Interface

System bus mining for ize interface								
SDA (In) SGL SGL SDA (Out) Trever trev								
ltem	Symbol	Min.	Тур.	Max.	Unit	Conditions		
SCL Clock Frequency	FSCL	-	-	400	KHz			
SCL Clock Low Period	TLOW	1300	-	-	ns			
SCL Clock High Period	THIGH	600	-	-	ns			
Signal Rise Time	Tr	20+0.1Cb	-	300	ns			
Signal Fall Time	Tf	20+0.1Cb	-	300	ns			
Start Condition Setup Time	TSU;STA	600	-	-	ns			
Start Condition Hold Time	THD;STA	600	-	-	ns			
Data Setup Time	TSU;DAT	100	-	-	ns			
Data Hold Time	THD;DAT	0	-	900	ns			
Setup Time for STOP Condition	TSU;STO	600	-	-	ns			
Bus Free Time Between a STOP	TRUE	100			ns			
and START	TBOI	100	-	-				
Capacitive load represented by		Cb		400	рF			
each bus line		00		100	P'			



9.3. System Bus Timing for 3-Wire SPI Interface



ltem	Symbol	Min.	Тур.	Max.	Unit	Conditions
CS Input Setup Time	Ts0	50	-	-	ns	
Serial Data Input Setup Time	Ts1	50	-	-	ns	
CS Input Hold Time	Th0	50	-	-	ns	
Serial Data Input Hold Time	Th1	50	-	-	ns	
SCL Write Pulse High Width	Twh1	50	-	-	ns	
SCL Write Pulse Low Width	Twl1	50	-	-	ns	
SCL Read Pulse High Width	Trh1	300			ns	
SCL Read Pulse Low Width	Trl1	300			ns	
CS Pulse High Width	Tw2	400	-	-	ns	





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Item	Symbol	Min.	Тур.	Max.	Unit	Conditions
CLK Pulse Duty	Tclk	40	50	60	%	
HSYNC Width	Thw	2	-	-	DCLK	
VSYNC Setup Time	Tvst	12	-	-	ns	
VSYNC Hold Time	Tvhd	12	-	-	ns	
HSYNC Setup Time	Thst	12	-	-	ns	
HSYNC Hold Time	Thhd	12	-	-	ns	
Data Setup Time	Tdsu	12	-	-	ns	
Data Hold Time	Tdhd	12	-	-	ns	
DE Setup Time	Tdest	12	-	-	ns	
DE Hold Time	Tdehd	12	-	-	ns	



10.Communication Interface 10.1. 3-wire Serial Interface



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before then rising edge of CS pulse are valid data.

f. Serial block operates with the SCL clock

g. Serial data can be accepted in the power save mode.

h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.



10.2. I2C Interface

The I2C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

Driver		HOST
SPL_PC_SEL	GND	
		SCL
		SDA



1. Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.



2. START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.





3. System Configuration



The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.



4.Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledgerelated clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated as follows.





5. I2C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I2C Interface, the device which should respond is addressed first. The default slave address is 0111100b and the three times I2C address could be OTP programing.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.





10.3. RGB Interface

1.Pin Assignment for RGB Interface

	Din	F	arallel RG	В	Serial RGB		
	F III	888	666	565	888	666	565
VSVNC	SYNC Mode	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
VOTING	DE Mode	x	x	x	x	x	x
HSVNC	SYNC Mode	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
Horne	DE Mode	x	x	x	x	x	x
DE	SYNC Mode	x	x	x	x	x	x
DE	DE Mode	DE	DE	DE	DE	DE	DE
(CLK	CLK	CLK	CLK	CLK	CLK	CLK
	DR0	R0	x	x	x	x	x
[DR1	R1	x	x	x	x	x
[DR2	R2	R0	x	x	x	x
	DR3	R3	R1	R0	x	x	x
(DR4	R4	R2	R1	x	x	x
(DR5	R5	R3	R2	x	x	x
(DR6	R6	R4	R3	x	x	x
(DR7	R7	R5	R4	x	x	x
[DG0	G0	x	x	D0	x	x
[DG1	G1	x	x	D1	x	x
[)G2	G2	G0	G0	D2	D0	D0
[DG3	G3	G1	G1	D3	D1	D1
[DG4	G4	G2	G2	D4	D2	D2
[DG5	G5	G3	G3	D5	D3	D3
[DG6	G6	G4	G4	D6	D4	D4
[DG7	G7	G5	G5	D7	D5	D5
	DB0	B0	x	x	x	x	x
[DB1	B1	x	x	x	x	x
[DB2	B2	B0	x	x	x	x
[DB3	B3	B1	B0	x	x	x
I	DB4	B4	B2	B1	x	x	x
[DB5	B5	B3	B2	x	x	x
[DB6	B6	B4	B3	x	x	x
	DB7	B7	B5	B4	x	x	x

RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC - DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: "Input" means these signals are driven by host side



2. Parallel RGB SYNC Mode





3. Serial RGB SYNC Mode





4. Parallel RGB SYNC-DE Mode





5. Serial RGB SYNC-DE Mode





6. Parallel RGB DE Mode





7. Serial RGB DE Mode





8. Parallel RGB Input Timing Table

Parallel 24-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25 C)

	Parallel 24-bit RGB Input Timing Table											
	ltem	Symbol	Min.	Тур.	Max.	Unit	Note					
DCLK	Frequency	Fclk	5	6	8	MHz						
DC	LK Period	Tclk	125	167	200	ns						
	Period Time	Th	325	371	438	DCLK						
	Display Period	Thdisp		320		DCLK						
HSYNC	Back Porch	Thbp	3	43	43	DCLK	SYNC mode back porch control by H_BLANKING[7:0] setting Thbp= H_BLANKING[7:0]					
	Front Porch	Thfp	2	8	75	DCLK						
	Pulse Width	Thw	2	4	43	DCLK						
	Period Time	Τv	244	260	289	HSYNC						
	Display Period	Tvdisp		240		HSYNC						
VSYNC	Back Porch	Tvbp	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING[7:0] setting Tvbp= V_BLANKING[7:0]					
	Front Porch	Tvfp	2	8	37	HSYNC						
	Pulse Width	Tvw	2	4	12	HSYNC						

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.



9. Serial RGB Input Timing Table

Serial 8-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25 C)

	Serial 8-bit RGB Input Timing Table										
	Item	Symbol	Min.	Тур.	Max.	Unit	Remark				
DCLK	Frequency	Fclk	15	18	21	MHz					
DC	LK Period	Tclk	47	55	66	ns					
	Period Time	Th	965	1011	1078	DCLK					
	Display Period	Thdisp		960		DCLK					
							SYNC mode back porch control				
HSYNC	Back Porch	Thbp	3	43	43	DCLK	by H_BLANKING[7:0] setting				
							Thbp= H_BLANKING[7:0]				
	Front Porch	Thfp	2	8	75	DCLK					
	Pulse Width	Thw	2	4	43	DCLK					
	Period Time	Τv	244	260	289	HSYNC					
	Display Period	Tvdisp		240		HSYNC					
							SYNC mode back porch control				
VSYNC	Back Porch	Tvbp	2	12	12	HSYNC	by V_BLANKING[7:0] setting				
							Tvbp= V_BLANKING[7:0]				
	Front Porch	Tvfp	2	8	37	HSYNC					
	Pulse Width	Tvw	2	4	12	HSYNC					

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.



11.Optical Characteristics

Item		Symbol	Condition.	Min	Тур.	Max.	Unit	Remark
Response tim	е	Tr+ Tf	θ=0° 、Φ=0°	-	30	40	ms	Note 3
Contrast ratio)	CR	At optimized viewing angle	640	800	-	-	Note 4
Color Chromaticity	\//bita	Wx	ፀ-0° 、	0.26	0.31	0.36	-	Note
Color Chromaticity	vvriite	Wy	0-0 • 0-0	0.30	0.35	0.40		2,6,7
	Hor	ΘR		70	80	-	Deg.	
Viewing angle	Hor.	ΘL		70	80	-		Note 1
viewing angle	Vor	ΦT	CR≦10	70	80	-		
	ver.	ΦВ		70	80	-		
Brightness		-	-	1000	-) -	cd/m	Center of display
Uniformity		(U)	-	75	')	-	%	Note 5

Ta=25±2℃, IL=40mA

Note 1: Definition of viewing angle range



Fig. 11.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.





Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90% to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10% to 90%



Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

Contrast ratio (CR) = $\frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$



Note 5: Definition of Luminance Uniformity Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area. Luminance Uniformity (U) = Lmin/Lmax x100% L = Active area length W = Active area width



Note 6: Definition of color chromaticity (CIE 1931) Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



12.Reliability

Content of Reliability Test (Wide temperature, $-20^{\circ}C \sim 70^{\circ}C$)

Envir	onmental	Test

Test Item	Content of Test	Test Condition	Note
High Temperature	Endurance test applying the high storage temperature	80 ℃	2
storage	for a long time.	200hrs	
Low Temperature	Endurance test applying the low storage temperature	-30 ℃	1,2
storage	for a long time.	200hrs	
High Temperature	Endurance test applying the electric stress (Voltage &	70° ℃	
Operation	Current) and the thermal stress to the element for a long time.	200hrs	
Low Temperature	Endurance test applying the electric stress under low	-20°C	1
Operation	temperature for a long time.	200hrs	
High Temperature/	The module should be allowed to stand at	60°C,90%RH	1,2
Humidity Operation	60℃,90%RH max	96hrs	
Thermal shock	The sample should be allowed stand the following 10	-20℃/70℃	
resistance	cycles of	10 cycles	
	operation		
	-20°C 25°C 70°C		
	30min 5min 30min		
Vibration test	Endurance test applying the vibration during	Total fixed amplitude :	3
	transportation and using.	1.5mm	-
	in an open control of the second	Vibration Frequency :	
		10~55Hz	
		One cycle 60	
		seconds to 3	
		directions of X,Y,Z for	
		Each 15 minutes	
Static electricity test	Endurance test applying the electric stress to the	VS=±600V(contact)	
	terminal.	.±800v(air).	
		RS=3300	
		CS=150pF	
		10 times	

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

13.檢驗規範(Inspection Specification)

- 1. 範圍(Scope): 適用於本公司 TFT-LCD 模塊(The document shall be applied to TFT-LCD Module)
- 2. 檢驗標準(Inspection Standard): MIL-STD-105E 正常單次抽樣水平 II(MIL-STD-105E Table Normal Inspection Single Sampling Level II)
- 3. 缺陷水平(Defect Level):主要缺陷 AQL:0.65;次要缺陷 AQL:2.5(Major Defect AQL:0.65;Minor Defect AQL:2.5)
- 4. 檢驗條件(Test conditions):
 - (1)溫度(Temperature):15℃~25℃;溼度(Humidity):55±15%
 - (2)外觀檢驗(Visual inspection):光照強度:500 Lux 以上;檢查距離:20cm~30cm (Illumination: More than 500 Lux; Inspection Distance: 20cm~30cm)
 - (3)電性檢驗(Electrical inspection):光照強度:100Lux~300Lux;檢查距離:20cm~30cm(Illumination: 100Lux~300Lux; Inspection Distance: 20cm~30cm)
 - (4)目視角度(Visual angle):檢查目視的角度是法線方法的 45 °(The test direction is base on about around 45° of Vertical line)



IN I	0.	Б	IX	0	D	IX.	0	D	Dot Delect	
R	G	в	R	G	в	R	G	В	Adjacent Dot Defect	
R	G	B	R	G	B	R	G	В	Cluster	

- Note 1:If pixel or partial sub-pixel defects exceed 50% of the affected pixel or sub-pixel area, it shall be considered as1 defect.
- Note 2: There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

項次 (No)	檢驗項目(Inspection item)	檢驗標準(Inspection Standard)	缺陷等級 (Defect Level
1	PACKING &INDICATE	 1.1.不可有混入其他型號產品的現象(Mixde product types). 1.2.不可有產品漏工序的現象(The part number is inconsistent with work order of production). 1.3.不可有部件裝反方向的現象(Assembled in inverse direction). 1.4.不可有數量與實際要求不一致的現象(The quantity is inconsistent with work order of production). 	主缺 (Maj)
2	尺寸(Size)	产品尺寸和结构必须符合结构图(Product size and structure must meet the structure diagram)	主缺 (Maj)
3	玻璃裂纹(The crack of glass)	X:破裂長度(Symbols) Y:破裂寬度(The width of crack). Z:破裂厚度(The thickness of crack). W:出電極區寬度(Terminal length) T:玻璃厚度(The thickness of glass). a:LCD 側面長度(LCD side length). 3.1.一般玻璃被損(General glass chip): 3.1.一般玻璃表面或上、下玻璃組合縫隙之間破損(Chip on panel surface and crack between panels); Image: Seal width Image: Seal wi	次缺 (Min)

項次	檢驗項目(Inspection	檢驗標準(Inspection Standard)	缺陷等級
(No)	item)		(Defect Level)
項次 (No)	檢驗項目(Inspection item)	検驗標準(Inspection Standard) X Y Z ≤1/5a 裂紋進人 VA 區(Crack can't enter viewing area) ≤1/2t ≤1/5a 裂紋超過 SP++的寬度(Crack can't enter can't exceed the half of SP width) 1/2t < Z ≤ 2t	缺陷等級 (Defect Level)
		X Y Z ≤1/3a ≤W ≤t 備註(Note): 如果破碎部分触及 ITO 電極則不可超過 ITO 電極寬 度的 1/3,且必須進行通電測試,不可影響顯示效果 (If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications). 3.2.3.玻璃破損(Glass remain) : X Y Z X Y Z ≤a ≤1/3W ≤t	

	項次 (No)	檢驗項目(Inspection item)	on 檢驗標準(Inspection Standard)					andard)	缺陷等級 (Defect Level)			
	(110)	四點、 台 點晃物	4.	1 Round								
	4	(Black or white dot)Round type $X \downarrow Y$		尺寸 (Size)	判定相	問定標準(Judging standard) ① ≤0.25mm ① 欠收數量 (Acceptance(Q'ty)) ②略不計(Ignore)		允收數量 (Acceptance(Q'ty)) 忽略不計(Ignore)	次缺			
				1.44″ ~4.9"	0.25	25mm < D ≤ 0.5mm		N≦3	(Min)			
						D > 0.5mm		$N \leq 0$				
		Ť	_	distance >=5mm			ance >=5mm					
		刮痕、線狀異物	5.	5.1 Line type(Non-display or display):								
				尺寸 (Size)	判定相	標準(Judging standard)		允收數量 (Acceptance(O'ty))				
		(scratch		1.44" ~7.0"		W	L					
	5	contamination) Line type \overrightarrow{I}^{W}			$W{\leq}$	0.05mm	_	忽略不計(Ignore)	次缺 (Min)			
					0.05m 0.	m <w≦ .1mm</w≦ 	$L \leq 5mm$	N≦3				
					W >	> 0.1mm	L > 5mm	$N \leq 0$				
			distance >=5mm									
	6	POL 氣泡(Polarizer Bubble)		視區(area)		判定標 star	準(Judging ndard)	允收數量 (Acceptance(Q'ty))				
						D <	<mark>0.2</mark> mm	忽略不計(Ignore)				
				A區(Vi	iewing	$\frac{0.2 \text{mm} < \text{D} \leq 0.3 \text{mm}}{2}$		N≦3				
				are	a)	0.3 mm < D ≤ 0.5 mm		$N \leq 1$	-火缺 (Min)			
						0.5n	nm <d< td=""><td>$N \leq 0$</td><td></td></d<>	$N \leq 0$				
				B 區(Outside of viewing area)			_	忽略不計(Ignore)				
	項次 (No)	檢驗項目(Inspection item)			缺陷等級 (Defect Level)							
	7	POL 折痕&分層(The folding and peeled offin polarizer)	偏光片不可有折痕和分層(脫膠)的現象(The folding and peeled offin polarizer are not acceptable).						次缺 (Min)			
	8	輝度及均匀性、色度 (Brightness and uniformity、Chroma)	應符合規範或圖紙要求規格(Shall be in accordance with the drawings and specification requirements specifications).					主缺 (Maj)				
	9	MURA	(5	(5% ND Filter)灰階 50%								

	10	電性測試(Electrical 3 Testing) 4	 1.顯示缺畫(Missing line character and icon). 2.無功能與無顯示(No function or no display). 3.顯示故障(Display malfunction). 4.LCD 視角缺陷(LCD viewing angle defect). 5.消耗電流超出規格(Current consumption exceeds product specifications). 						
	11	亮點、暗點(Bright dot、Dark dot)On-display Pixel: 3 dot in 1 pixel	尺寸 (Size)	Item	判定標準(Judging standard)	允收數量 (Acceptance(Q'ty))			
				Bright dot	$D \leq 1/2$ Pixel	忽略不計(Ignore)			
					$1/2$ Pixel $\leq D \leq 1$ Pixel	N≦1	次缺		
			1.44"~ 4.9"	Dark	$D \leq 1/2$ Pixel	忽略不計(Ignore)	(Min)		
				dot	$1/2$ Pixel $\leq D \leq 1$ Pixel	$N \leq 2$			
					Total	N≦3			
			distance >=5mm						

	LCM Sample	e Estimate Feedback Sheet			
Module Number :					
1 · Panel Specification :					
1. Panel Type:	Pass	□ NG ,			
2. View Direction :	Pass	□ NG ,			
3. Numbers of Dots :	□ Pass	□ NG ,			
4. View Area :	□ Pass	□ NG ,			
5. Active Area :	□ Pass	□ NG ,			
6.Operating Temperature :	□ Pass	□ NG ,			
7.Storage Temperature :	□ Pass	□ NG ,			
8.Others :		·			
2 · Mechanical Specification :					
1. PCB Size :	□ Pass	□ NG ,			
2.Frame Size :	□ Pass	□ NG ,			
3.Materal of Frame :	Pass	□ NG ,			
4.Connector Position :	Pass	□ NG ,			
5.Fix Hole Position :	Pass	□ NG ,			
6.Backlight Position :	□ Pass	□ NG ,			
7. Thickness of PCB :	Pass	□ NG ,			
8. Height of Frame to PCB :	□ Pass	□ NG ,			
9.Height of Module :	□ Pass	□ NG ,			
10.Others :	□ Pass	□ NG ,			
3 × <u>Relative Hole Size</u> :					
1.Pitch of Connector :	□ Pass	□ NG ,			
2.Hole size of Connector :	Pass	□ NG ,			
3.Mounting Hole size :	□ Pass	□ NG ,			
4.Mounting Hole Type :	Pass	□ NG ,			
5.Others :	□ Pass	□ NG ,			
4 · Backlight Specification					
1.B/L Type:	□ Pass	□ NG ,			
2.B/L Color :	□ Pass	□ NG ,			
3.B/L Driving Voltage (Reference for LED Type) : □ Pass □ NG ,					
4.B/L Driving Current :	□ Pass	□ NG ,			
5.Brightness of B/L :	Pass	□ NG ,			
6.B/L Solder Method :	Pass	□ NG ,			
7.Others :	□ Pass	□ NG ,			

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Module Number :				
5 · Electronic Characteristics of Module				
1.Input Voltage:	Pass	□ NG ,		
2.Supply Current :	Pass	□ NG ,		
3.Driving Voltage for LCD:	Pass	□ NG ,		
4.Contrast for LCD :	Pass	□ NG ,		
5.B/L Driving Method :	Pass	□ NG ,		
6.Negative Voltage Output :	Pass	□ NG ,		
7.Interface Function :	□ Pass	□ NG ,		
8.LCD Uniformity :	Pass	□ NG ,		
9.ESD test :	Pass	□ NG ,		
10.Others :	Pass	□ NG ,		

6 ∖ <u>Summary</u> :

Sales signature :				
Customer Signature :	Date :	/	1	_

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