SDR Series
CR-P401D / CR-P501D
User Manual

info@cruetech.ru www.cruetech.ru

Version Records:

Date	Version	Description
2025.10.8	V1.0	initial version

This tutorial will be continuously revised, optimized, and expanded based on practical experience. Our goal is to provide you with more and better demos to aid your development as a field expert.

If you find any errors or have suggestions, please contact us.

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Content

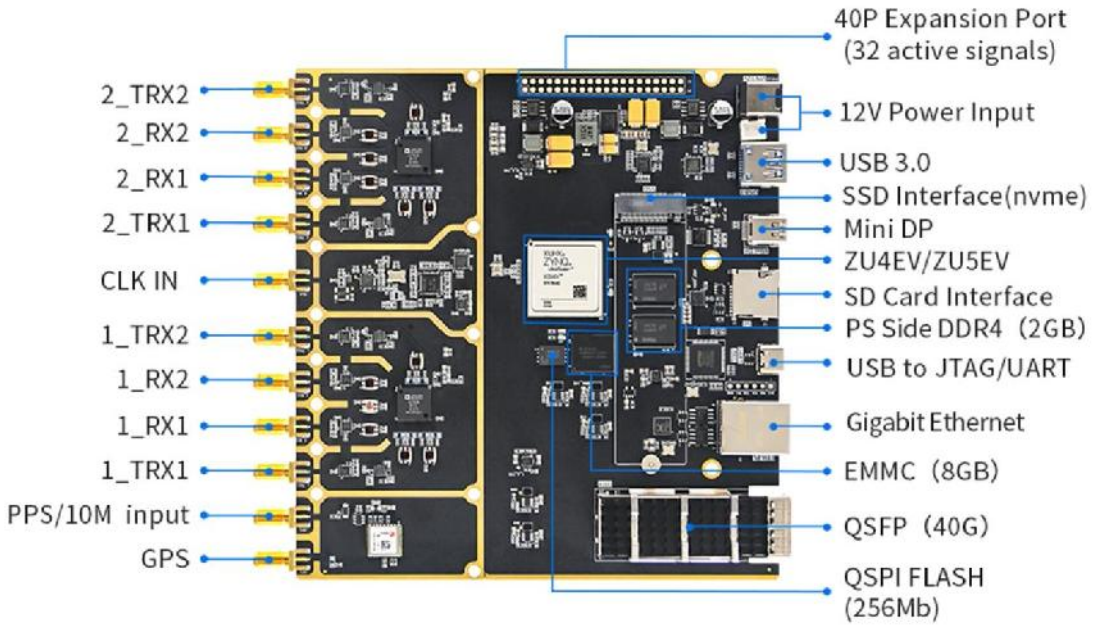
Part 1:CR-P401D /CR-P501D Overview

1.1 CR-P401D /CR-P501D Introduction

The Software Defined Radio encompasses a diverse range of products. This document introduces the CR-P401D / CR-P501D, which utilizes XILINX's XCZU4EV-2SFVC784I/XCZU5EV-2SFVC784I as its main controller and integrates two ADI AD9361BBCZ RF transceivers to form its core architecture. Equipped with multiple RF and peripheral interfaces, the CR-P401D / CR-P501D offers rich resources and user-friendly operation. The product's internal resource structure is illustrated below.

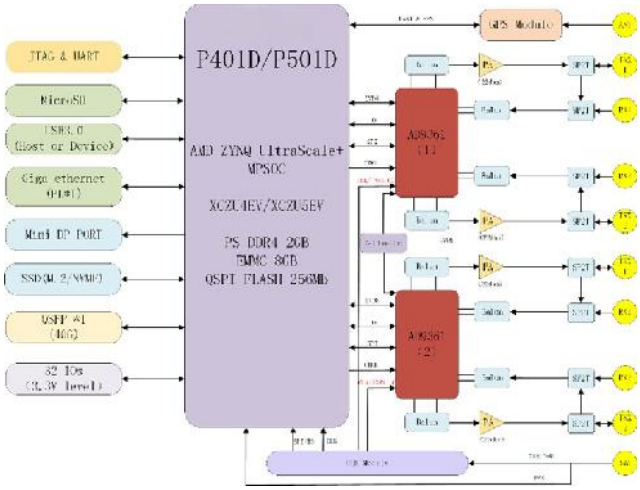
The PCB dimensions of the CR-P401D / CR-P501D are 160mm (length) × 150mm (width). The PCB reserves multiple mounting holes for easy integration into user equipment. Additionally, it comes with a sleek enclosure for heat dissipation, ensuring stable product operation.

Industrial-grade designed, the CR-P401D / CR-P501D operates within a temperature range of -40℃ to 85℃. It uses a high-precision clock, with all interfaces featuring ESD (Electrostatic Discharge) protection.



1.2 CR-P401D /CR-P501D Block Diagram

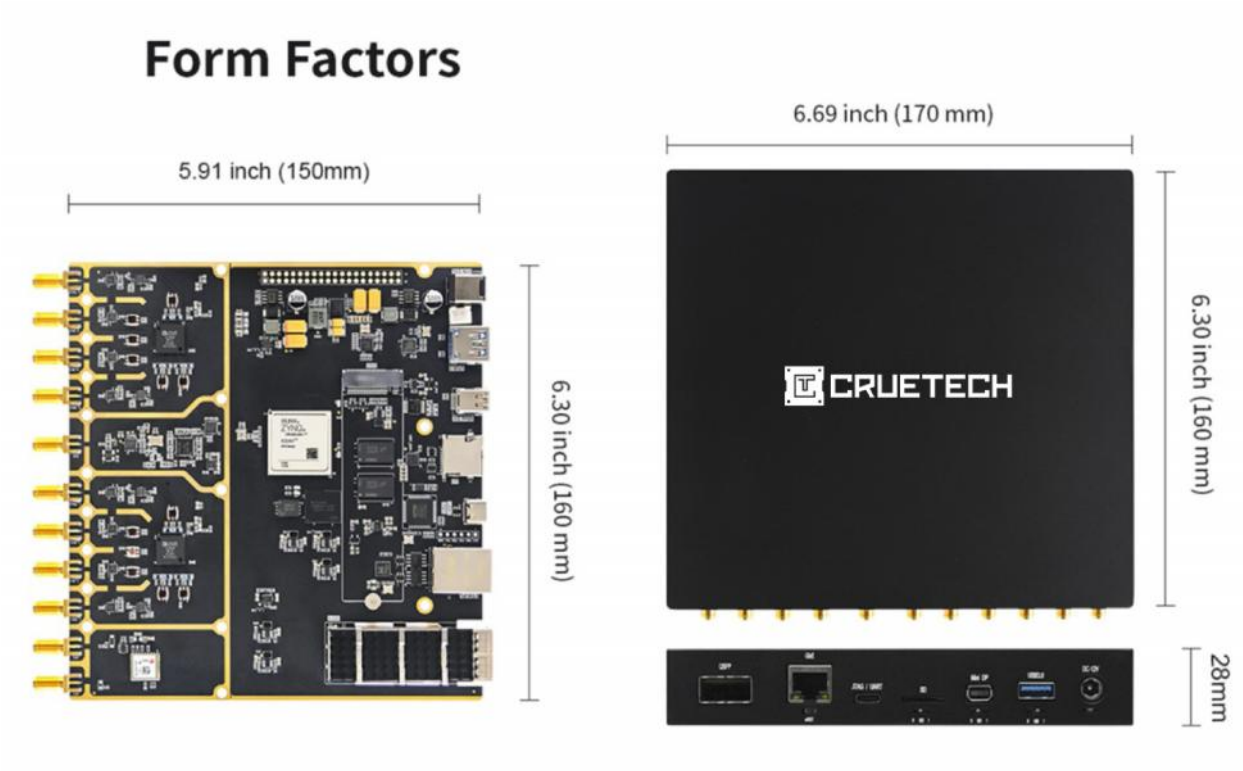
In this section, we will show the configuration details of the product in detail through the product block diagram, as shown below.



1.3 CR-P401D /CR-P501D Form Factors

The figure below illustrates the dimensions of the carrier board and enclosure respectively：PCBA Board form factors is 160mm * 150mm (6.30inch * 5.91inch), and the customized shell form factor is 170mm * 160mm (6.69inch * 6.30inch).

Note:Enclosure logo customization is supported—users only need to provide the logo file to get an exclusive customized logo.



Part 2:Hardware User Manual

In this part, we will systematically introduce the various hardware functions of CR-P401D / CR-P501D to help users get started quickly. The two products differ only in the main chip, and all other parts are identical.

2.1 CR-P401D /CR-P501D Framework Overview

The table below outlines the CR-P401D / CR-P501D carrier board's specifications and external resources. It integrates two AD9361BBCZ chips, enabling 4T/4R RF channels and multiple high-speed data transmission interfaces to realize full RF link transmit-receive functionality.

For additional details, refer to the company-provided drawings.

SDR Module	CR-P401D	CR-P501D
FPGA Chip	XCZU4EV-2SFVC784I	XCZU5EV-2SFVC784I
Processor Core	4 x Cortex-A53-1.3GMhz	2 x Cortex-R5-533Mhz
Speed Grade	2	
Chip Level	Industrial Grade(-40°C~+85°C)	
Logic Cells	192K	256K
Lookup Tables	176000	234000
Flip-Flops	88000	117000
DSP Slices	728	1248
BLOCK RAM	4.5Mb	5.1Mb
RF Chip	AD9361BBCZ	
Frequency range	70M-6Ghz	
Signal Bandwidths	200K-56Mhz	
Power Amplifier	22dbm	
DDR4	PS Side 2GB	
QSPI FLASH	256Mb	
RF Clock	40 MHz VCTCXO(0.1PPM)/External Input	
Gigabit Ethernet	PL Side 1 Gigabit Ethernet	
USB 3.0	1	
UART	1	
JTAG	1	
SD Card Slot	1	
GPS	1	
PPS/10M input	1	
External Clock Input	1	
Expansion Port IOs	40-pin 2.54mm pitch connector (Including 5V/3.3V power supplies, 32 signal lines)	
Form Factors	Board: 150mm x 160mm (5.91 inch x 6.30 inch) with Shell: 170mm x 160mm x 28mm	
Protection Class	All External Interfaces are Protected against Static Electricity, Clock/RF are Shielde	
Power Supply	12V/3A	

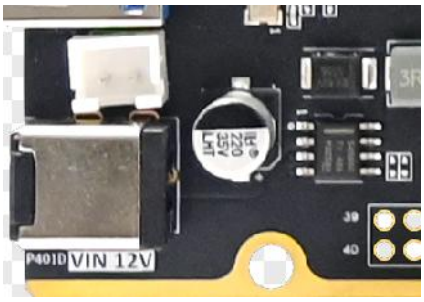
2.2 Power Supply

The CR-P401D / CR-P501D supports two power supply options: XH2.54 and DC-007B interfaces, accommodating customer power needs across different usage scenarios.

XH2.54 Interface: For integration into user equipment, power is supplied via this interface with a 12V/3A specification.

DC-007B Interface: This interface connects to 12V/3A power adapter for power, featuring a plug-and-play design.

Note: The DC-007B and XH2.54 connectors are interconnected. For safety reasons, please connect only one power source to either of them at a time to prevent mutual interference between the two power supplies.



2.3 Clock Section

The CR-P401D / CR-P501D carrier board features multiple clock channels to meet diverse functional requirements. For additional details, refer to the company-provided drawings.

(1) The PS side incorporates a 33.33 MHz clock input, with input pin PS_REF_CLK located at R16. This clock serves as the ARM-side clock source.

(2) The PL side is supplied with a 200 MHz clock, with input pins IO_L12P_GC_65/IO_L12N_GC_65 mapped to locations L3/L2. This clock acts as the PL-side clock source.

(3) The MGT section has two dedicated clock channels: 125 MHz and 156.25 MHz, with the following pin mappings:

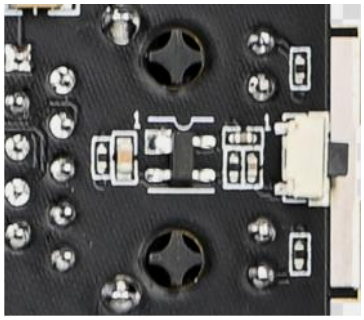
- 125 MHz clock: MGT_REF_CLK_P0_224/ MGT_REF_CLK_N0_224 (pin locations: Y6/Y5)
- 156.25 MHz clock: MGT_REF_CLK_P1_224/ MGT_REF_CLK_N1_224 (pin locations: V6/V5)

(4) The GTR section is equipped with three clock channels (26 MHz, 27 MHz, 100 MHz), allocated respectively to the USB 3.0, Mini DP, and SSD peripheral interfaces.

(5) The RF circuit is configured with a dedicated clock chip, which delivers multiple clock channels and external local oscillator circuits to enable synchronous operation of the multi-RF-chip architecture.

2.4 Resetkey

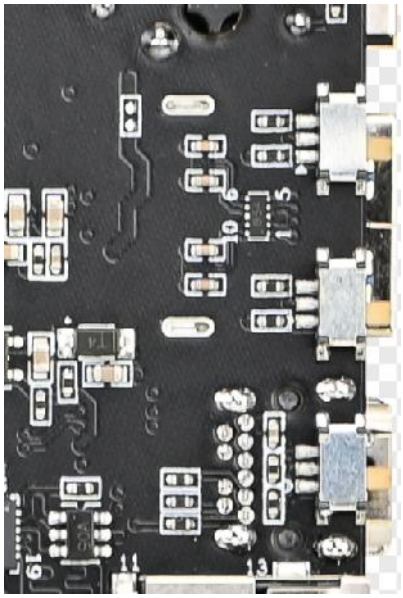
The CR-P401D / CR-P501D carrier board features an nGST reset key at the board edge, serving as the active-low system reset. The nGST pin connects to PS_POR_B (P16) on the PS side and IO_T1U_66（D2）on the PL side respectively.



2.5 Main Controller Boot Modes

The CR-P401D / CR-P501D carrier board supports four boot modes: JTAG, QSPI Flash, EMMC, and SD card. Boot mode selection is via board-edge DIP switches. Three DIP selector switches (M2/M1/M0) are shown below, with corresponding boot modes selected per the boot truth table.

BOOT MODE	M2	M1	M0
JTAG	0	0	0
QSPI FLASH	0	1	0
SD1 CARD	1	0	1
EMMC	1	1	0



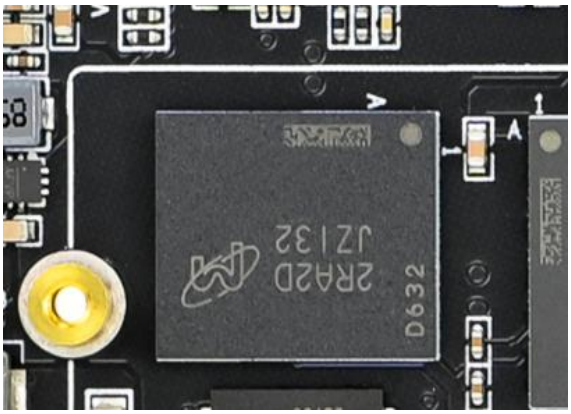
2.6 DDR4 Introduction

The CR-P401D / CR-P501D carrier board's PS side integrates two industrial-grade DDR4 chips, each with 1 GB capacity for a total of 2 GB. PS-side DDR4 pin assignment supports direct use of the system default configuration, or refer to the company-provided demo.

2.7 EMMC Introduction

The CR-P401D / CR-P501D are equipped with an 8GB EMMC storage module, for users to store boot files and user data. Pin definitions are detailed in the table below.

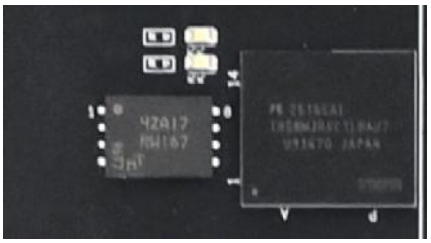
EMMC	Pin Name	Pin Position
EMMC_DATA0	MIO13	AH18
EMMC_DATA1	MIO14	AG18
EMMC_DATA2	MIO15	AE18
EMMC_DATA3	MIO16	AF18
EMMC_DATA4	MIO17	AC18
EMMC_DATA5	MIO18	AC19
EMMC_DATA6	MIO19	AE19
EMMC_DATA7	MIO20	AD19
EMMC_CLK	MIO22	AB20
EMMC_CMD	MIO21	AC21
EMMC_nRST	MIO23	AB18



2.8 QSPIFLASH Introduction

The CR-P401D / CR-P501D integrates one 256 Mb QSPI FLASH chip, which is used for storing boot files and user files. Pin definitions are detailed in the table below.

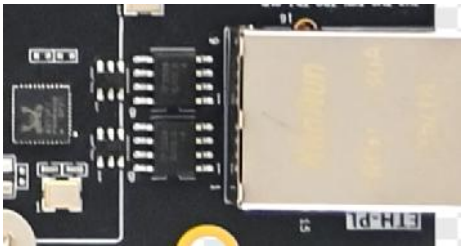
QSPIO FLASH	Pin Name	Pin Position
QSPIO_DQ0	MIO4	AH16
QSPIO_DQ1	MIO1	AG16
QSPIO_DQ2	MIO2	AF15
QSPIO_DQ3	MIO3	AH15
QSPIO_CS	MIO5	AD16
QSPIO_CLK	MIO0	AG15



2.9 Gigabit Ethernet

The CR-P401D / CR-P501D carrier board's PL side integrates a Gigabit Ethernet chip, which connects to the ZYNQ via the RGMII interface. Corresponding pins are detailed in the table below. The PHY address is configured as PHY_AD[2:0] = 001.

RGMII Signal	Pin Name	Pin Position
GPHY_GTX_CLK	IO_L11P_T1U_N8_GC_64	AF7
GPHY_TXD0	IO_L21N_T3L_N5_AD8N_64	AF3
GPHY_TXD1	IO_L8N_T1L_N3_AD5N_64	AG8
GPHY_TXD2	IO_L9P_T1L_N4_AD12P_64	AH8
GPHY_TXD3	IO_L7N_T1L_N1_QBC_AD13N_64	AH9
GPHY_TX_EN	IO_L4N_T0U_N7_DBC_AD7N_64	AE7
GPHY_RX_CLK	IO_L12P_T1U_N10_GC_64	AE5
GPHY_RXD0	IO_L22P_T3U_N6_DBC_AD0P_64	AE2
GPHY_RXD1	IO_L21P_T3L_N4_AD8P_64	AE3
GPHY_RXD2	IO_L22N_T3U_N7_DBC_AD0N_64	AF2
GPHY_RXD3	IO_L11N_T1U_N9_GC_64	AF6
GPHY_RX_DV	IO_L24P_T3U_N10_64	AF1
GPHY_MDC	IO_L7P_T1L_N0_QBC_AD13P_64	AG9
GPHY_MDIO	IO_L2N_T0L_N3_64	AE8



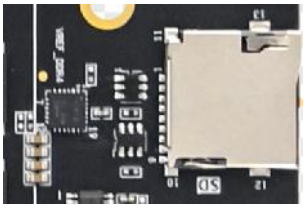
2.10 SD Card Slot Interface

The CR-P401D / CR-P501D carrier board features an SD card slot connected to BANK501 on the PS side. With BANK501 operating at 1.8 V and the SD card's data interface at 3.3 V, the TXS02612RTWR chip is used for level shifting.

SD card pin assignments are detailed below. For detailed circuit design, refer to the schematic.

SD card	Pin Name	Pin Position
SD_CLK	MIO51	L21
SD_CMD	MIO50	M19
SD_DATA0	MIO46	L20

SD_DATA1	MIO47	H21
SD_DATA2	MIO48	J21
SD_DATA3	MIO49	M18

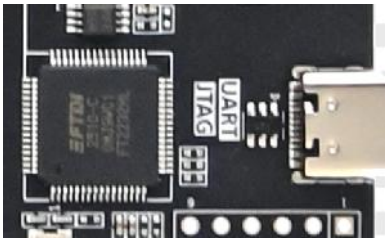


2.11 USB to JTAG and UART

The CR-P401D / CR-P501D carrier board features a USB-to-JTAG/UART interface: the JTAG segment connects to the main control chip's JTAG interface, while the UART segment connects to the chip's UART1 pins.

UART1 pin assignments are detailed below. For detailed circuit design, refer to the schematic.

UART1	Pin Name	Pin Position
UART1_TX	MIO40	K18
UART1_RX	MIO41	J19



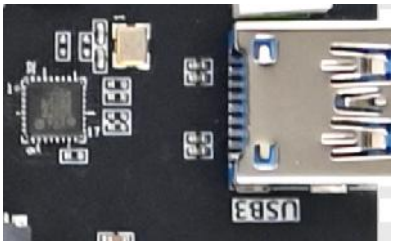
2.12 USB 3.0

The CR-P401D / CR-P501D carrier board features a USB 3.0 (Type-A) interface, configurable as either Host or Device mode.

The mapping between the USB PHY and main control chip is detailed in the table below. For additional details, refer to the carrier board schematic.

USB signalpins	Pin Name	Pin Position
USBPHY_DATA0	MIO56	C16
USBPHY_DATA1	MIO57	A16
USBPHY_DATA2	MIO54	F17
USBPHY_DATA3	MIO59	E17
USBPHY_DATA4	MIO60	C17
USBPHY_DATA5	MIO61	D17
USBPHY_DATA6	MIO62	A17
USBPHY_DATA7	MIO63	E18
USBPHY_STP	MIO58	F18
USBPHY_NXT	MIO55	B16
USBPHY_DIR	MIO53	D16

USBPHY_CLKOUT	MIO52	G18
USBPHY_nRSET	MIO64	E19
GT2_USB3_SSTXP	PS_MGTRTXP2_505	C25
GT2_USB3_SSTXN	PS_MGTRTXN2_505	C26
GT2_USB3_SSRXP	PS_MGTRRXP2_505	B27
GT2_USB3_SSRXN	PS_MGTRRXN2_505	B28
CLK_FPGA_26M_P	MGT_505_TX_P2	C21
CLK_FPGA_26M_N	MGT_505_TX_N2	C22

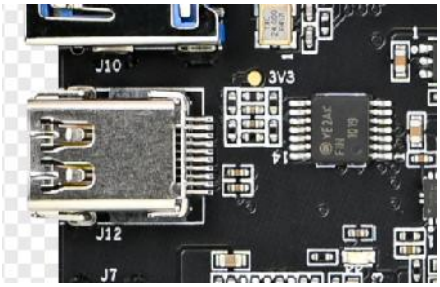


2.13 Mini DP

The CR-P401D / CR-P501D carrier board integrates a Mini DP output interface, whose interface signals connect to FPGA BANK46/BANK505. For details, refer to the schematic.

Mini DP interface pin assignments are listed below; refer to the development board schematic for detailed circuit implementation.

MiniDP	Pin Name	Pin Position
GT3_DP_LINE_P0	MGT_505_TX_P3	B23
GT3_DP_LINE_N0	MGT_505_TX_N3	B24
DP_HPD	IO_L8P_HDGC_AD4P_46	F15
DP_AUX_OUT	IO_L5P_HDGC_AD7P_46	D15
DP_OE	IO_L8N_HDGC_AD4N_46	E15
DP_AUX_IN	IO_L9P_AD3P_46	G15
DP_CLK_P_27M	MGT_505_CLK_P3	A21
DP_CLK_N_27M	MGT_505_CLK_N3	A22

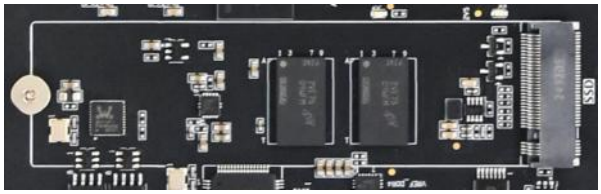


2.14 SSD interface

The CR-P401D / CR-P501D carrier board integrates an SSD interface (x2 mode) on its PS side, featuring an M.2 form factor and NVMe protocol compliance.

SSD interface pin locations are detailed in the table below; refer to the development board schematic for specific circuit implementation.

SSD interface	Pin Name	Pin Position
SSD_nRST	MIO70	C19
CLK_FPGA_100M_P	MGT_505_CLK_P0	F23
CLK_FPGA_100M_N	MGT_505_CLK_N0	F24
GT0_SSD_TX_P0	MGT_505_TX_P0	E25
GT0_SSD_TX_N0	MGT_505_TX_N0	E26
GT0_SSD_RX_P0	MGT_505_RX_P0	F27
GT0_SSD_RX_N0	MGT_505_RX_N0	F28
GT1_SSD_TX_P1	MGT_505_TX_P1	D23
GT1_SSD_TX_N1	MGT_505_TX_N1	D24
GT1_SSD_RX_P1	MGT_505_RX_P1	D27
GT1_SSD_RX_N1	MGT_505_RX_N1	D28



2.15 QSFP Interface

The CR-P401D / CR-P501D carrier board integrates a QSFP+ interface supporting data rates up to 40G. The interface signals are connected to the MPSoC's BANK224. For specific connection details, please refer to the schematic.

The pin assignments for the QSFP+ interface are provided in the table below. For the detailed circuit implementation, consult the carrier board schematic.

QSFP	Pin Name	Pin Position
QSFP_TX_P0	MGT_TX_P1_224	U4
QSFP_TX_N0	MGT_TX_N1_224	U3
QSFP_TX_P1	MGT_TX_P3_224	N4
QSFP_TX_N1	MGT_TX_N3_224	N3
QSFP_TX_P2	MGT_TX_P0_224	W4
QSFP_TX_N2	MGT_TX_N0_224	W3
QSFP_TX_P3	MGT_TX_P2_224	R4
QSFP_TX_N3	MGT_TX_N2_224	R3
QSFP_RX_P0	MGT_RX_P1_224	V2
QSFP_RX_N0	MGT_RX_N1_224	V1
QSFP_RX_P1	MGT_RX_P3_224	P2
QSFP_RX_N1	MGT_RX_N3_224	P1
QSFP_RX_P2	MGT_RX_P0_224	Y2
QSFP_RX_N2	MGT_RX_N0_224	Y1
QSFP_RX_P3	MGT_RX_P2_224	T2

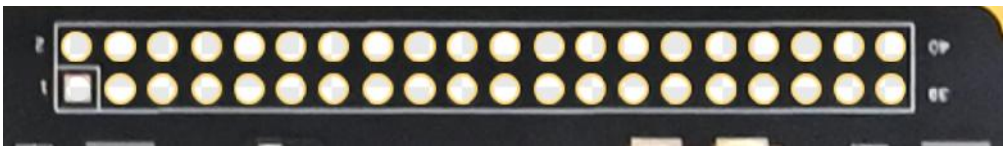
QSFP_RX_N3	MGT_RX_N2_224	T1

2.16 40P Expansion Interface

The CR-P401D / CR-P501D carrier board reserves a 2.54 mm-pitch 40-pin connector for extended signal connectivity, whose signals connect to FPGA BANK45/46 with a 3.3 V voltage level.

Signal-corresponding chip locations are listed in the table below; refer to the schematic section for detailed connection relationships.

JM1 Signal Sequence	Pin Name	Pin Position	JM1 Signal Sequence	Pin Name	Pin Position
5	IO_L1P_25_45	J11	6	IO_L3P_25_45	H11
7	IO_L1N_25_45	J10	8	IO_L3N 25 45	G10
9	IO_L7P_HDGC 25	E10	10	IO_L8P_HDGC_25_45	E12
11	IO L7N_HDGC_25	D10	12	IO L8N HDGC 25 45	D11
13	IO_L9P 25_45	C11	14	IO L5P HDGC 25 45	G11
15	IO L9N 25 45	B10	16	IO_L5N_HDGC_25_45	F10
17	IO_L11P_25_45	A12	18	IO_L10P_25_45	B11
19	IO L11N 25 45	A11	20	IO_L10N_25_45	A10
21	IO_L12P 25 45	D12	22	IO_L6P_HDGC_ 25_45	F12
23	IO L12N 25 45	C12	24	IO_L6N_HDGC_ 25_45	F11
25	IO_L2P_25_45	K13	26	IO_L4P 25_45	J12
27	IO L2N 25 45	K12	28	IO_L4N 25_45	H12
29	IO L3P 26_46	B13	30	IO_L2P_26_46	B14
31	IO_L3N_26_46	A13	32	IO_L2N_26_46	A14
37	IO L1P_26_46	B15	38	IO_L4P_26_46	C14
39	IO L1N 26 46	A15	40	IO_L4N_26_46	C13



2.17 LED Indicators

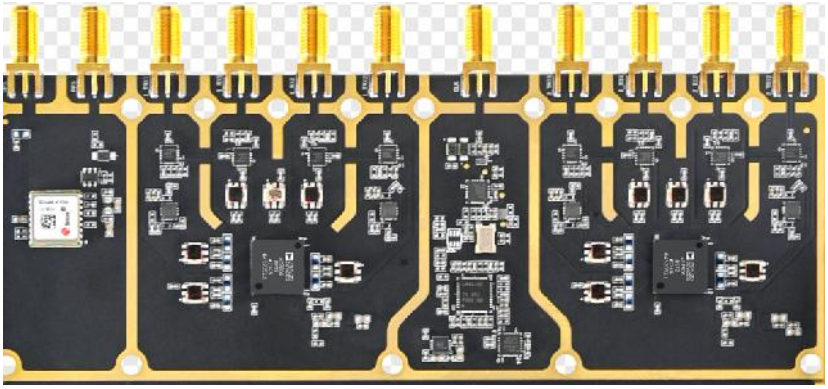
The CR-P401D / CR-P501D carrier board integrates two LEDs configured in active-high

mode: illuminated at high level and extinguished at low level. Refer to the development board schematic for detailed circuit implementation.

LED designator	Pin Name	Pin Position
LED1(D17)	IO_L5N_44	AD14
LED2(D18)	IO_L8P_44	AB15

2.18 AD9361 Introduction

The CR-P401D / CR-P501D carrier board's RF section integrates two ADI AD9361BBCZ RF transceivers. This section elaborates on three key components: RF link, data channels, and clock circuitry.



2.18.1 RF Front-End Circuit

The CR-P401D / CR-P501D carrier board's RF front-end circuit comprises three components: a balun, a power amplifier (PA), and an RF switch. The balun features a 10 MHz–6 GHz bandwidth, covering the AD9361's communication bandwidth.

The power amplifier offers a 10 MHz–8 GHz bandwidth, not only covering the AD9361's communication bandwidth but also delivering high linearity. Power amplifier performance metrics at various frequency points are detailed in the table below.

FREQ	Gain	Isolation	Input Return Loss	Output Return Loss	Stability		IP-3 Output	1dB Comp. Output	Noise Figure
(MHz)	(dB)	(dB)	(dB)	(dB)	K	Measure	(dBm)	(dBm)	(dB)
10	20.46	27.17	9.18	14.25	1.15	0.87	25.43	19.41	8.92
100	22.20	25.13	22.46	21.95	1.05	0.50	30.65	22.45	1.37
200	22.28	25.07	23.42	23.85	1.04	0.48	28.68	22.50	1.06
300	22.29	25.08	23.27	24.74	1.05	0.49	29.17	22.55	1.02
400	22.29	25.15	22.98	25.12	1.05	0.50	27.58	22.54	0.97
500	22.29	25.19	22.58	25.57	1.05	0.50	29.99	22.55	0.96
1000	22.28	25.22	19.66	27.67	1.05	0.52	29.94	22.67	0.94
1200	22.28	25.25	18.42	27.51	1.05	0.52	31.22	22.78	0.96
1400	22.27	25.35	17.29	26.20	1.06	0.54	29.62	22.80	0.91
1600	22.26	25.42	16.20	24.55	1.06	0.55	29.97	22.83	0.94
1800	22.25	25.45	15.30	22.84	1.06	0.55	31.54	22.80	0.96
2000	22.23	25.55	14.44	21.32	1.06	0.57	32.31	22.68	0.97
2200	22.21	25.62	13.69	20.06	1.07	0.58	33.26	22.75	0.93
2400	22.18	25.67	13.06	19.05	1.07	0.58	29.73	22.78	1.07
2600	22.17	25.86	12.58	18.29	1.08	0.60	28.43	22.65	0.98
2800	22.16	25.88	12.19	17.80	1.08	0.61	30.87	22.38	1.05
3000	22.16	25.94	11.94	17.47	1.08	0.62	29.72	22.10	0.99
3200	22.16	26.04	11.74	17.30	1.08	0.63	28.81	21.77	1.06
3400	22.16	26.12	11.63	17.22	1.09	0.64	28.42	21.40	1.04
3600	22.16	26.20	11.60	17.21	1.09	0.64	28.39	21.13	1.06
3800	22.18	26.24	11.60	17.36	1.09	0.65	28.86	21.56	1.05
4000	22.20	26.27	11.70	17.64	1.09	0.65	29.25	21.51	1.16
4200	22.22	26.35	11.87	18.05	1.10	0.66	30.11	21.70	1.14
4400	22.24	26.42	12.10	18.50	1.10	0.67	28.80	21.74	1.19
4600	22.27	26.45	12.36	19.04	1.10	0.67	29.16	21.61	1.14
4800	22.32	26.55	12.67	19.61	1.11	0.68	29.37	21.83	1.19
5000	22.37	26.55	13.02	20.26	1.11	0.68	30.08	21.69	1.21
5200	22.43	26.66	13.44	20.86	1.12	0.69	28.61	21.57	1.22
5400	22.48	26.67	13.87	21.44	1.12	0.68	29.58	21.33	1.27
5600	22.55	26.67	14.42	21.98	1.12	0.68	28.42	21.15	1.23
5800	22.61	26.80	15.06	22.61	1.12	0.69	29.99	21.12	1.22
6000	22.66	26.85	15.80	23.09	1.13	0.69	28.20	21.28	1.22
6200	22.73	26.92	16.75	23.01	1.13	0.69	28.94	21.09	1.10
6400	22.77	26.98	17.74	22.66	1.14	0.69	29.82	21.04	1.20
6600	22.81	27.06	19.02	21.83	1.15	0.69	30.01	21.24	1.14
6800	22.86	27.19	20.71	20.64	1.16	0.70	29.50	21.05	1.15
7000	22.91	27.25	22.82	19.57	1.16	0.70	28.62	20.90	1.17
7200	22.94	27.35	24.91	18.68	1.17	0.70	29.79	20.90	1.14
7400	22.94	27.41	26.72	17.99	1.18	0.70	28.14	20.80	1.16
7600	22.93	27.57	26.69	17.33	1.20	0.71	30.13	20.20	1.15
7800	22.92	27.73	25.02	16.70	1.22	0.72	28.81	20.10	1.19
8000	22.89	27.96	23.01	16.34	1.25	0.74	29.42	19.59	1.23
8200	22.84	28.11	20.99	16.14	1.27	0.75	28.14	19.10	1.23
8400	22.78	28.34	19.42	16.02	1.30	0.77	28.40	18.78	1.23
8600	22.70	28.59	18.18	16.27	1.34	0.79	27.50	18.22	1.25
8800	22.59	28.83	17.09	16.71	1.39	0.82	27.89	18.12	1.33
9000	22.46	29.19	16.24	17.37	1.45	0.84	28.51	18.14	1.45
9200	22.31	29.42	15.50	18.23	1.51	0.87	28.63	17.44	1.59
9400	22.13	29.81	14.75	19.22	1.60	0.89	27.39	17.01	1.65
9600	21.89	30.15	14.06	20.07	1.69	0.92	28.06	16.83	1.83
9800	21.59	30.58	13.41	20.21	1.80	0.94	26.04	16.17	2.00
10000	21.25	31.03	12.70	19.48	1.94	0.96	27.73	16.12	2.14

The RF switch employs an SPDT (Single-Pole Double-Throw) architecture (1 input, 2 outputs) with a frequency range of 9 kHz to 8 GHz. It also integrates an internal ESD (Electrostatic Discharge) protection circuit, delivering robust protection for RF ports.

Refer to the table below for the RF switch's switching logic. For AD9361 TX/RX switching, implement adjustments based on the actual connection details specified in the schematic diagram.

LS	CTRL	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

2.18.2 AD9361 Communication Port

The AD9361 digital ports fall into two categories: data ports and control ports. Moreover, the two AD9361 chips share a single SYNC signal.

Data port pin mappings are listed in the table below; for additional details, refer to the CR-P401D / CR-P501D schematic and corresponding project code.

1-AD9361	Pin Name	Pin Position
1_AD9361_TX_P0	IO_L20P_T3L_N2_AD1P_65	J6
1_AD9361_TX_N0	IO_L20N_T3L_N3_AD1N_65	H6

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1_AD9361_TX_P1	IO_L21P_T3L_N4_AD8P_65	J7
1_AD9361_TX_N1	IO_L21N_T3L_N5_AD8N_65	H7
1_AD9361_TX_P2	IO_L23P_T3U_N8_I2C_SCLK_65	K9
1_AD9361_TX_N2	IO_L23N_T3U_N9_65	J9
1_AD9361_TX_P3	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	H9
1_AD9361_TX_N3	IO_L24N_T3U_N11_PERSTN0_65	H8
1_AD9361_TX_P4	IO_L19P_T3L_N0_DBC_AD9P_65	J5
1_AD9361_TX_N4	IO_L19N_T3L_N1_DBC_AD9N_65	J4
1_AD9361_TX_P5	IO_L22P_T3U_N6_DBC_AD0P_65	K8
1_AD9361_TX_N5	IO_L22N_T3U_N7_DBC_AD0N_65	K7
1_AD9361_FB_CLK_P	IO_L11P_T1U_N8_GC_65	K4
1_AD9361_FB_CLK_N	IO_L11N_T1U_N9_GC_65	K3
1_AD9361_TX_FRAME_P	IO_L9P_T1L_N4_AD12P_65	K2
1_AD9361_TX_FRAME_N	IO_L9N_T1L_N5_AD12N_65	J2
1_AD9361_RX_P0	IO_L2P_T0L_N2_65	U9
1_AD9361_RX_N0	IO_L2N_T0L_N3_65	V9
1_AD9361_RX_P1	IO_L17P_T2U_N8_AD10P_65	N9
1_AD9361_RX_N1	IO_L17N_T2U_N9_AD10N_65	N8
1_AD9361_RX_P2	IO_L15P_T2L_N4_AD11P_65	N7
1_AD9361_RX_N2	IO_L15N_T2L_N5_AD11N_65	N6
1_AD9361_RX_P3	IO_L5P_T0U_N8_AD14P_65	R7
1_AD9361_RX_N3	IO_L5N_T0U_N9_AD14N_65	T7
1_AD9361_RX_P4	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	R8
1_AD9361_RX_N4	IO_L4N_T0U_N7_DBC_AD7N_65	T8
1_AD9361_RX_P5	0_L6P_T0U_N10_AD6P_65	R6
1_AD9361_RX_N5	IO_L6N_T0U_N11_AD6N_65	T6
1_AD9361_DATA_CLK_P	IO_L13P_T2L_N0_GC_QBC_65	L7
1_AD9361_DATA_CLK_N	IO_L13N_T2L_N1_GC_QBC_65	L6
1_AD9361_RX_FRAME_P	IO_L8P_T1L_N2_AD5P_65	J1
1_AD9361_RX_FRAME_N	IO_L8N_T1L_N3_AD5N_65	H1
1_AD9361_CLK_OUT	0_L14P_T2L_N2_GC_65	M6
1_AD9361_SPI_CLK	IO_L3P_T0L_N4_AD15P_65	U8
1_AD9361_SPI_nCS	IO_L1P_T0L_N0_DBC_65	W8
1_AD9361_SPI_DI	IO_T3U_N12_65	K5
1_AD9361_SPI_DO	IO_L1N_T0L_N1_DBC_65	Y8
1_AD9361_nRST	IO_L3N_T0L_N5_AD15N_65	V8
1_AD9361_ENABLE	IO_T2U_N12_65	P9
1_AD9361_EN_AGC	IO_L18P_T2U_N10_AD2P_65	M8
AD9361_SYNC_IN	IO_L18N_T2U_N11_AD2N_65	L8
1_AD9361_TXNRX	IO_L14N_T2L_N3_GC_65	L5
1_AD9361_CTRL_OUT0	IO_L10P_T1U_N6_QBC_AD4P_64	AG6
1_AD9361_CTRL_OUT1	IO_T1U_N12_64	AH6
1_AD9361_CTRL_OUT2	IO_L19P_T3L_N0_DBC_AD9P_64	AG4
1_AD9361_CTRL_OUT3	IO_L20N_T3L_N3_AD1N_64	AH3
1_AD9361_CTRL_OUT4	IO_L19N_T3L_N1_DBC_AD9N_64	AH4
1_AD9361_CTRL_OUT5	IO_L10N_T1U_N7_QBC_AD4N_64	AG5
1_AD9361_CTRL_OUT6	IO_L9N_T1L_N5_AD12N_64	AH7
1_AD9361_CTRL_OUT7	IO_L18P_T2U_N10_AD2P_64	AB1

1_AD9361_CTRL_IN0	IO_L23N_T3U_N9_64	AH1
1_AD9361_CTRL_IN1	IO_L24N_T3U_N11_64	AG1
1_AD9361_CTRL_IN2	IO_L23P_T3U_N8_64	AH2
1_AD9361_CTRL_IN3	IO_L20P_T3L_N2_AD1P_64	AG3

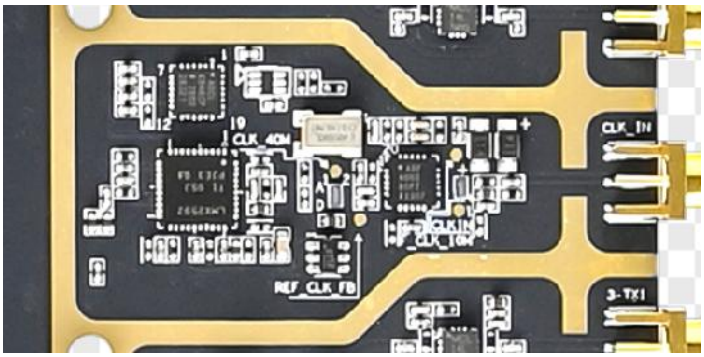
2-AD9361	Pin Name	Pin Position
2_AD9361_TX_P0	IO_L23P_T3U_N8_66	A9
2_AD9361_TX_N0	IO_L23N_T3U_N9_66	A8
2_AD9361_TX_P1	IO_L16P_T2U_N6_QBC_AD3P_66	G8
2_AD9361_TX_N1	IO_L16N_T2U_N7_QBC_AD3N_66	F7
2_AD9361_TX_P2	IO_L18P_T2U_N10_AD2P_66	E9
2_AD9361_TX_N2	IO_L18N_T2U_N11_AD2N_66	D9
2_AD9361_TX_P3	IO_L24P_T3U_N10_66	C9
2_AD9361_TX_N3	IO_L24N_T3U_N11_66	B9
2_AD9361_TX_P4	IO_L22P_T3U_N6_DBC_AD0P_66	C8
2_AD9361_TX_N4	IO_L22N_T3U_N7_DBC_AD0N_66	B8
2_AD9361_TX_P5	IO_L20P_T3L_N2_AD1P_66	C6
2_AD9361_TX_N5	IO_L20N_T3L_N3_AD1N_66	B6
2_AD9361_FB_CLK_P	IO_L13P_T2L_N0_GC_QBC_66	D7
2_AD9361_FB_CLK_N	IO_L13N_T2L_N1_GC_QBC_66	D6
2_AD9361_TX_FRAME_P	IO_L21P_T3L_N4_AD8P_66	A7
2_AD9361_TX_FRAME_N	IO_L21N_T3L_N5_AD8N_66	A6
2_AD9361_RX_P0	IO_L8P_T1L_N2_AD5P_66	A2
2_AD9361_RX_N0	IO_L8N_T1L_N3_AD5N_66	A1
2_AD9361_RX_P1	IO_L10P_T1U_N6_QBC_AD4P_66	B4
2_AD9361_RX_N1	IO_L10N_T1U_N7_QBC_AD4N_66	A4
2_AD9361_RX_P2	IO_L9P_T1L_N4_AD12P_66	B3
2_AD9361_RX_N2	IO_L9N_T1L_N5_AD12N_66	A3
2_AD9361_RX_P3	IO_L7P_T1L_N0_QBC_AD13P_66	C1
2_AD9361_RX_N3	IO_L7N_T1L_N1_QBC_AD13N_66	B1
2_AD9361_RX_P4	IO_L2P_T0L_N2_66	E1
2_AD9361_RX_N4	IO_L2N_T0L_N3_66	D1
2_AD9361_RX_P5	IO_L5P_T0U_N8_AD14P_66	E4
2_AD9361_RX_N5	IO_L5N_T0U_N9_AD14N_66	E3
2_AD9361_DATA_CLK_P	IO_L11P_T1U_N8_GC_66	D4
2_AD9361_DATA_CLK_N	IO_L11N_T1U_N9_GC_66	C4
2_AD9361_RX_FRAME_P	IO_L19P_T3L_N0_DBC_AD9P_66	B5
2_AD9361_RX_FRAME_N	IO_L19N_T3L_N1_DBC_AD9N_66	A5
2_AD9361_CLK_OUT	IO_L14P_T2L_N2_GC_66	E5
2_AD9361_SPI_CLK	IO_L17P_T2U_N8_AD10P_66	F8
2_AD9361_SPI_nCS	IO_L1P_T0L_N0_DBC_66	G1
2_AD9361_SPI_DI	IO_L15N_T2L_N5_AD11N_66	F6
2_AD9361_SPI_DO	IO_L1N_T0L_N1_DBC_66	F1
2_AD9361_nRST	IO_L3P_T0L_N4_AD15P_66	F2
2_AD9361_ENABLE	IO_L15P_T2L_N4_AD11P_66	G6
2_AD9361_EN_AGC	IO_T3U_N12_66	C7
AD9361_SYNC_IN	IO_L18N_T2U_N11_AD2N_65	L8
2_AD9361_TXNRX	IO_T2U_N12_66	E7

2_AD9361_CTRL_OUT0	IO_L5N_T0U_N9_AD14N_64	AC7
2_AD9361_CTRL_OUT1	IO_L3N_T0L_N5_AD15N_64	AC8
2_AD9361_CTRL_OUT2	IO_L1P_T0L_N0_DBC_64	AC9
2_AD9361_CTRL_OUT3	IO_L14P_T2L_N2_GC_64	AC4
2_AD9361_CTRL_OUT4	IO_L6P_T0U_N10_AD6P_64	AB6
2_AD9361_CTRL_OUT5	IO_L16P_T2U_N6_QBC_AD3P_64	AD2
2_AD9361_CTRL_OUT6	IO_L5P_T0U_N8_AD14P_64	AB7
2_AD9361_CTRL_OUT7	IO_L14N_T2L_N3_GC_64	AC3
2_AD9361_CTRL_IN0	IO_L13N_T2L_N1_GC_QBC_64	AD4
2_AD9361_CTRL_IN1	IO_L1N_T0L_N1_DBC_64	AD9
2_AD9361_CTRL_IN2	IO_L6N_T0U_N11_AD6N_64	AC6
2_AD9361_CTRL_IN3	IO_L4P_T0U_N6_DBC_AD7P_64	AD7

2.18.3 AD9361 Clock Circuit

The AD9361 input clock uses a 40 MHz 0.1 ppm high-precision VCXO clock. A dedicated clock chip generates the required multi-channel clocks. Meanwhile, the CR-P401D / CR-P501D carrier board provides reserved clock I/O interfaces: users may inject an external clock for higher precision, with the board capable of outputting required clocks on demand.

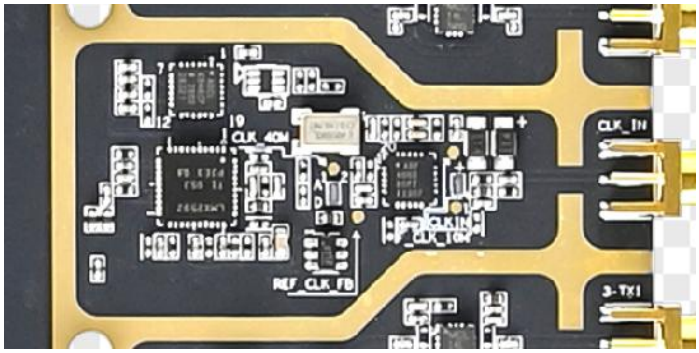
For detailed clock usage, refer to the schematic and corresponding code project for programming implementation.



2.18.4 AD9361 ExternalLocal0 scillator Input

The CR-P401D / CR-P501D carrier board integrates a local oscillator (LO) circuit. The LO chip can be configured to generate LO signals for the AD9361.

For the detailed circuit, refer to the schematic provided by supplier.



2.19 PPS

The CR-P401D / CR-P501D carrier board integrates a PPS (Pulse Per Second) signal channel, which serves as an input signal.

The PPS signal is connected to the following FPGA pin:

PPS signal	Pin Name	Pin Position
PPS_IN	IO_3N_44	AH13

2.20 GPS Module

The CR-P401D / CR-P501D carrier board integrates a GPS module that supports both GPS and BeiDou positioning. The module is configurable and its data readable via the UART interface; moreover, it provides a PPS signal.

GPS module pin mappings are listed in the table below. For detailed specifications, refer to the provided schematic.

GPS Module	Pin Name	Pin Position
GPS_UART_TXD	IO_2P_44	AG14
GPS_UART_RXD	IO_4N_44	AF13
GPS_nRESET	IO_3P_44	AG13
GPS_PPS	IO_2N_44	AH14