Series SDR

CR-P201m/CR-P203m

User Manual

Version Records:

Data	Version	Description
2023.05.25	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

Content

Version Records: 2
Part 1: Product Overview 4
Part 1.1: Product Overview 4
Part 1.2: Product Function Block Diagram 5
Part 1.3: Form Factors 5
Part 2: Hardware Overview 7
Part 2.1: P201M vs P203M 7
Part 2.2: About Power Supply 7
Part 2.3: System Clock 8
Part 2.4: Global Reset 8
Part 2.5: Boot Mode Selection 8
Part 2.6: DDR3 Introduction 9
Part 2.7: QSPI FLASH Introduction 9
Part 2.8: E2PROM Introduction 9
Part 2.9: PL side Gigabit Ethernet 9
Part 2.10: SD Card Slot Interface 10
Part 2.11: USB to JTAG and UART 10
Part 2.12: AD9361 Introduction 10
Part 2.12.1: RF Front-end Circuits 11
Part 2.12.2: AD9361 Control and Data Ports 12
Part 2.12.3: AD9361 Clock Circuit 13
Part 2.13: PPS and Clock Inputs 14
Part 2.14: IO Expansion Ports 14
Part 2.15: User LED 14

Part 1: Product Overview

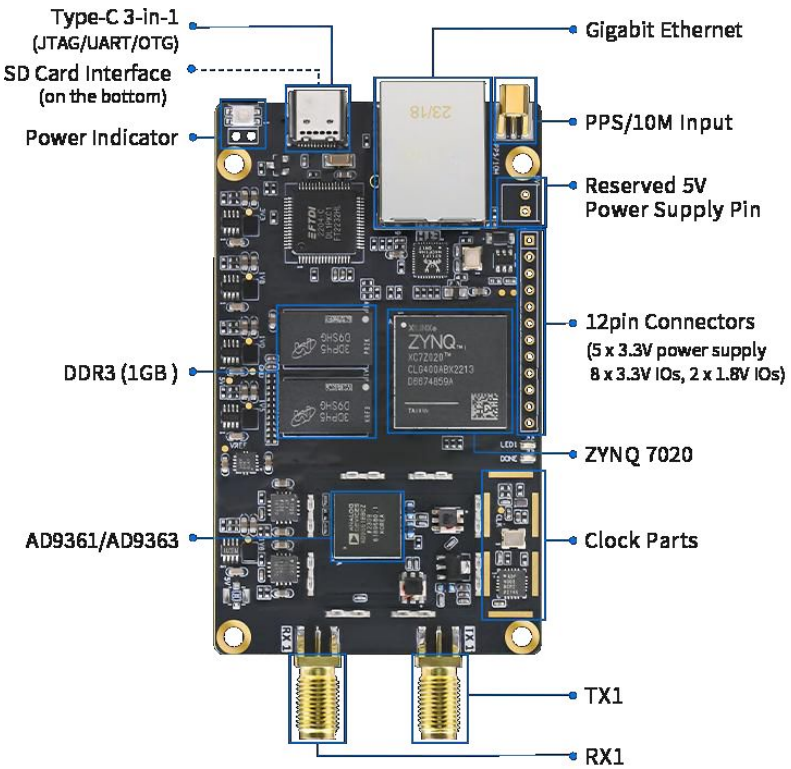
Part 1.1: Product Overview

This article introduces the P201M/P203M, these two hardware is fully compatible, direct software replacement can be used. The P201M/P203M used XILINX's XC7Z020-2CLG400I as the main controller, equipped with ADI's AD9361/AD9363 RF chip constitutes the main structure of the product. P201M is ZYNQ7020 with AD9361, P203M is ZYNQ7020 with AD9363, the main difference between the two is that the bandwidth of the RF chip is different, users can choose the corresponding products according to the actual requirements.

The P201M/P203M integrated a variety of RF and other hardware interfaces, rich resources, easy to use, the following Product Function Block Diagram is an overview of the internal resource structure.

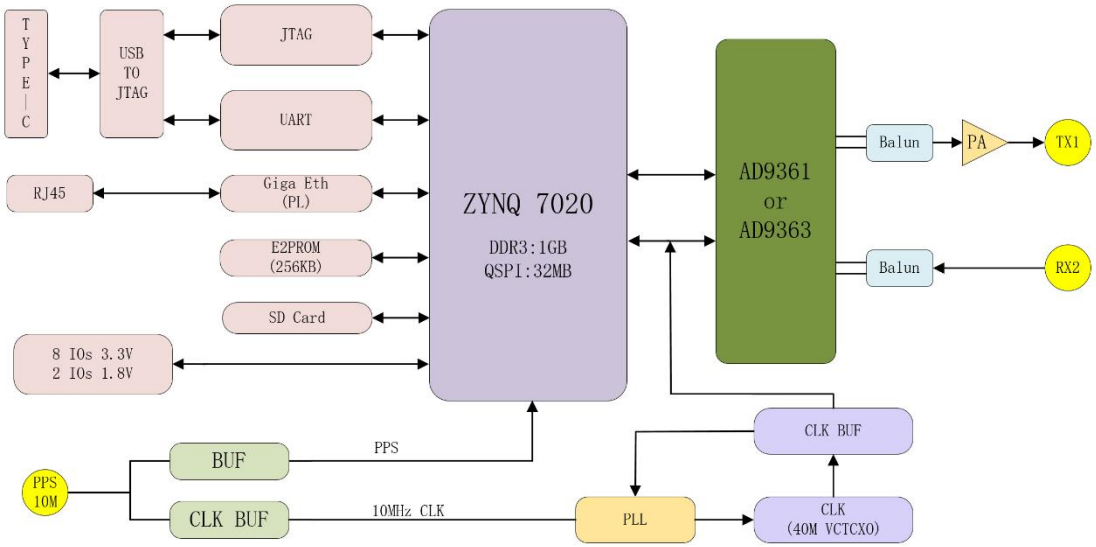
The PCBA Board Form Factors is 85mm * 50mm (3.35 inch * 1.97 inch), and the customized shell form factor is 95mm * 55mm (3.74 inch * 2.17 inch), the whole shell also plays a role in heat dissipation, to ensure the stable operation of the product.

The product is designed in accordance with industrial-grade standards, operating temperature -40℃-85 ℃, using a 0.1ppm high-precision clock, all interfaces are made of static electricity protection.



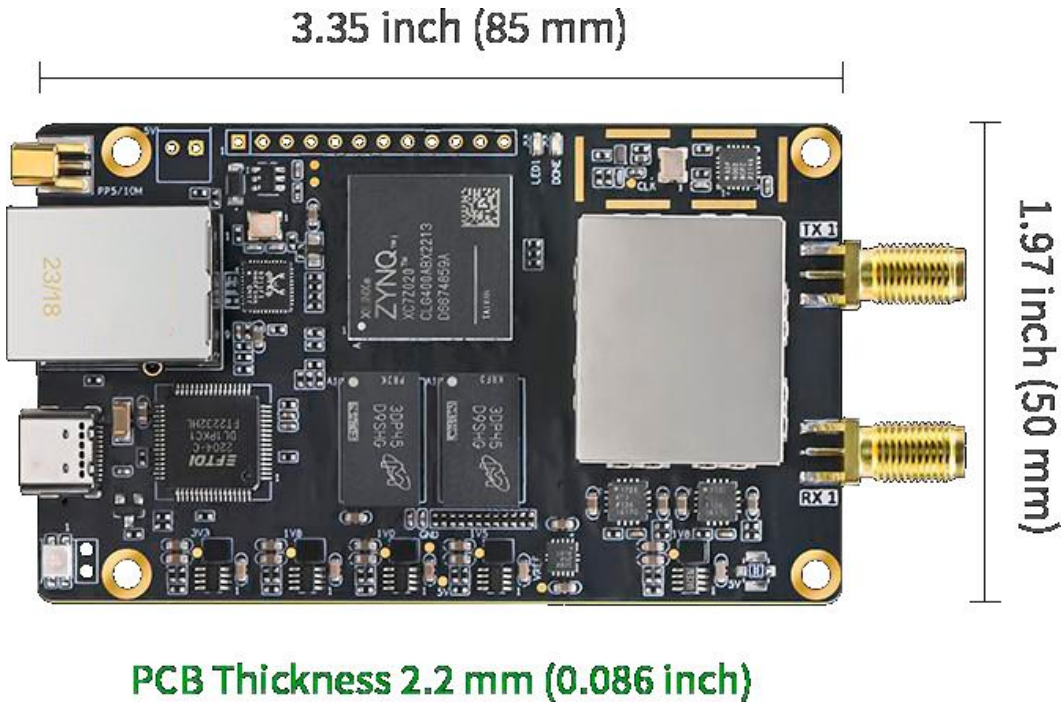
Part 1.2: Product Function Block Diagram

In this section, we will show the configuration details of the product in detail through the product block diagram and product specifications, as shown below.



Part 1.3: Form Factors

PCBA Board form factors is 85mm * 50mm (3.35 inch * 1.97 inch), and the customized shell form factor is 95mm * 55mm (3.74 inch * 2.17 inch).



3.74 inch (95 mm)
2.17 inch (55 mm)
CRUETECH
RX1
TX1
10/100/1000
PPS/10M
nRST
SD/QSPI JTAG
0.91 inch (23mm)

Part 2: Hardware Overview

Part 2.1: P201M vs P203M

The following table lists the parameter indicators of P201M and P203M. The difference between the two products is the selection of different RF chips, so the difference between P201Mini and P203Mini is the different frequency ranges of RF ports and different signal bandwidths. Users can compare the following table to choose the corresponding product.

SDR Main Parameters

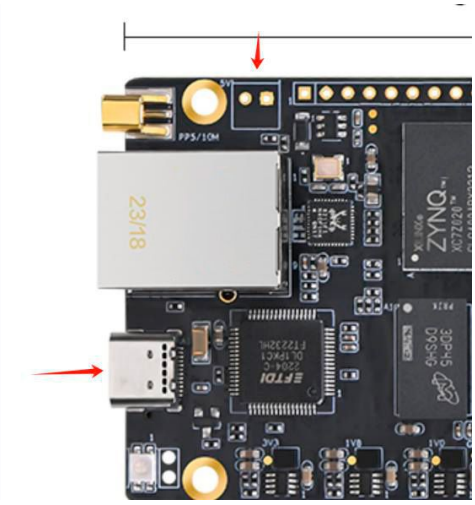
SDR Module	P201M	P203M
RF Chip	AD9361	AD9363
Frequency range	70M-6Ghz	325M-3.8Ghz
Signal Bandwidths	200K-56Mhz	200K-20Mhz
Power Amplifier	10-15dbm	
FPGA Chip	XC7Z020-2CLG400I	
Processor Core	Dual Cortex-A9, 766Mhz	
Logic Cells	85K	
DDR3	1GB	
QSPI FLASH	256Mb	
E2PROM	256Kb	
Gigabit Ethernet	1	
USB OTG	1	
UART	1	
JTAG	1	
SD Card	1	
Expansion Port IOs	8 x 3.3V IOs, 2 x 1.8V IOs	
Form Factors	Board: 3.35 inch x 1.97 inch x 0.09 inch with Shell: 3.74 inch x 2.17 inch x 0.91 inch	
Power Supply	TypeC/XH2.54 Power Supply Options	
Working Temperature	-40°C~+85°C	

Part 2.2: About Power Supply

The product provides two kinds of power supply mode: XH2.54 interface, TypeC interface, two kinds of power supply mode for customers to choose to use in different use mode.

XH2.54: If the product is integrated into the device, it can be powered through the XH2.54 interface, the power supply voltage range is 5V/1A, but it should be noted that the 5V must be handled with a good surge, you can add a capacitor in the input port, or in the external addition of a level of DCDC voltage regulator.

TypeC: Here the TypeC interface provides multiple functions, both on the board power supply, directly connected to the computer USB interface, you can provide 5V power for the board. At the same time is also a communication interface, provides a JTAG, UART communication function, convenient for users to download and debug the board.



Part 2.3: System Clock

The P201M/P203M provides a 33.33Mhz clock input for the PS side, the input pin location is PS_CLK_500; provides a 40M clock for the PL side, the input pin location is IO_L14P_SRCC_35, pin number is J18.

Part 2.4: Global Reset

The P201M/P203M provides the nGST reset key near the board edge location for a system reset key, active low. This pin is connected to the PS_POR_500 on the PS side and the IO_12N_MRCC_34 (pin location U19) pin on the PL side, respectively.

Part 2.5: Boot Mode Selection

The P201M/P203M supports three boot modes, namely JTAG, QSPI Flash, and SD card. Startup mode switching can provide the board side of the toggle switch to choose, when the switch toggle to the JTAG side, that is, JTAG startup mode, you can download the debugging single board through the JTAG interface; when the switch toggle to the side of the QSPI/SD, the startup mode switches to QSPI Flash and SD card mode, in this mode, we have done a special design, when not SD card, the default for QSPI In this mode, we have

made a special design, when SD card is not connected, the default is QSPI Flash startup, when SD card is connected, the startup mode is automatically switched to SD mode.

Part 2.6: DDR3 Introduction

The PS side is equipped with two industrial-grade DDR3 chips, a single capacity of 512MB, two total capacity of 1GB, model MT41K256M16TW-107IT:P, DDR3L pin allocation can directly call the system allocation. You can also refer to the Demos provided by our company.

Part 2.7: QSPI FLASH Introduction

The P201M/P203M has a 32MB QSPI FLASH onboard, which can be used to store startup files and user files.

QSPI FLASH PIN	PIN Name	PIN Position
DATA0	MIO2	B8
DATA1	MIO3	D6
DATA2	MIO4	B7
DATA3	MIO5	A6
QSPI_CS	MIO1	A7
QSPI_CLK	MIO6	A5

Part 2.8: E2PROM Introduction

An E2PROM is reserved on the P201M/P203M with a capacity of 256Kb and the pin definitions are listed in the table below.

E2PROM PIN	PIN Name	PIN Position
I2C_SCL	MIO10	E9
I2C_SDA	MIO11	C6

Part 2.9: PL side Gigabit Ethernet

The Gigabit Ethernet chip is placed on the carrier board, and the Ethernet chip is interconnected with the ZYNQ chip through the PL side, connecting the corresponding pins as shown in the following table Chip address PHY_AD[2:0]=010.

RMGII Signal	Pin Name	Pin Position
GPHY_GTX_CLK	IO_L3P_35	E17
GPHY_TXD0	IO_L3N_35	D18
GPHY_TXD1	IO_L4P_35	D19

GPHY_TXD2	IO_L4N_35	D20
GPHY_TXD3	IO_L5P_35	E18
GPHY_TX_EN	IO_L5N_35	E19
GPHY_RX_CLK	IO_L13P_MRCC_35	H16
GPHY_RXD0	IO_L6P_35	F16
GPHY_RXD1	IO_L6N_35	F17
GPHY_RXD2	IO_L7P_35	M19
GPHY_RXD3	IO_L7N_35	M20
GPHY_RX_DV	IO_L8P_35	M17
GPHY_MDC	IO_L2P_35	B19
GPHY_MDIO	IO_L2N_35	A20

Part 2.10: SD Card Slot Interface

The SD card holder is placed on the carrier board, which is connected to the BANK501 on the PS side of ZYNQ, because the level of BANK501 is 1.8V, but the data level of SD is 3.3V, We use the TXS02612RTWR for level shifting. The following is the pin assignment and schematic diagram of SD card interface, details refer to the schematic.

SD Card Slot Interface	Pin Name	Pin Position
SD_CLK	MIO40	D14
SD_CMD	MIO41	C17
SD_DATA0	MIO42	E12
SD_DATA1	MIO43	A9
SD_DATA2	MIO44	F13
SD_DATA3	MIO45	B15

Part 2.11: USB to JTAG and UART

The P201M/P203M is designed with a USB to JTAG/UART interface, the JTAG is connected to the JTAG interface of the host controller, and the UART is connected to the UART1 pin of the host controller. The following is the UART pin assignment, more detailed circuit can refer to the schematic.

UART	Pin Name	Pin Position
UART1_TX	MIO12	D9
UART1_RX	MIO13	E8

Part 2.12: AD9361 Introduction

The RF part of the product uses ADI's AD9361, and in this subsection will introduce in details, from the RF link, data channel, and clock part.

Part 2.12.1: RF Front-end Circuits

The RF front-end circuit involves three parts: balun, amplifier, and RF switch. The bandwidth of the balun is 10M-6Ghz, which covers the communication bandwidth of the AD9361.

The bandwidth of the amplifier is 50M-6Ghz, which also covers the communication bandwidth of AD9361, but the gain flatness of the amplifier in the whole communication bandwidth is slightly different. The following table can see the amplifier's indicators for each frequency point in detail.

FREQ	Gain	Isolation	Input Return Loss	Output Return Loss	Stability		IP-3 Output	1dB Comp. Output	Noise Figure
(MHz)	(dB)	(dB)	(dB)	(dB)	K	Measure	(dBm)	(dBm)	(dB)
50.00	17.73	23.19	14.21	18.51	1.14	0.76	31.53	17.82	2.10
80.00	17.14	22.43	16.76	18.87	1.14	0.73	32.21	17.91	1.97
100.00	16.93	22.26	18.14	19.00	1.15	0.72	32.46	17.83	2.00
200.00	16.55	22.00	21.40	19.27	1.18	0.72	32.09	17.88	1.96
400.00	16.32	21.92	22.06	19.17	1.19	0.72	32.80	17.69	2.18
500.00	16.22	21.95	21.60	19.08	1.20	0.73	32.65	17.75	2.22
600.00	16.12	21.91	20.87	18.92	1.21	0.73	32.75	17.73	2.18
800.00	15.90	21.94	19.22	18.59	1.23	0.75	32.97	17.68	2.22
1000.00	15.63	21.95	17.75	18.27	1.24	0.77	32.35	17.74	2.14
1200.00	15.34	21.94	16.45	17.96	1.26	0.79	33.10	17.70	2.27
1400.00	15.03	21.96	15.29	17.73	1.29	0.81	33.34	17.71	2.28
1500.00	14.88	21.96	14.70	17.47	1.29	0.82	32.76	17.78	2.31
1600.00	14.70	21.96	14.37	17.59	1.31	0.83	33.06	17.69	2.35
1800.00	14.38	21.98	13.49	17.43	1.33	0.85	33.66	17.56	2.36
2000.00	14.04	21.97	12.88	17.64	1.36	0.87	33.23	17.81	2.39
2200.00	13.72	21.93	12.29	17.75	1.38	0.89	33.13	17.99	2.45
2400.00	13.42	21.90	11.83	17.77	1.40	0.91	33.38	17.82	2.44
2500.00	13.27	21.94	11.64	17.87	1.41	0.92	33.32	17.96	2.50
2600.00	13.13	21.94	11.46	17.91	1.43	0.93	33.58	17.80	2.61
2800.00	12.85	21.83	11.14	17.97	1.44	0.95	33.46	17.78	2.65
3000.00	12.57	21.81	10.87	17.73	1.46	0.96	33.43	17.84	2.57
3200.00	12.35	21.77	10.64	17.84	1.47	0.97	32.91	17.81	2.70
3400.00	12.09	21.84	10.61	18.20	1.52	0.98	33.34	17.88	2.73
3500.00	12.00	21.75	10.43	17.93	1.51	0.98	33.57	17.63	2.89
3600.00	11.89	21.62	10.24	17.62	1.50	0.99	33.63	17.80	2.78
3800.00	11.68	21.57	10.12	17.40	1.52	0.99	33.53	17.82	2.91
4000.00	11.51	21.44	9.87	17.10	1.51	1.00	33.78	17.77	3.01
4200.00	11.36	21.39	9.75	16.86	1.52	1.00	33.67	17.67	2.96
4400.00	11.24	21.35	9.57	16.39	1.51	1.01	33.48	17.50	3.04
4500.00	11.08	21.33	9.53	16.36	1.54	1.01	33.53	17.62	3.12
4600.00	11.06	21.42	9.49	16.15	1.55	1.01	33.33	17.68	3.19
4800.00	10.90	21.23	9.20	15.40	1.52	1.02	33.45	17.59	3.25
5000.00	10.75	21.21	9.09	15.04	1.53	1.02	33.46	17.18	3.27
5200.00	10.64	21.03	8.71	14.21	1.49	1.02	33.61	17.24	3.34
5400.00	10.55	20.98	8.50	13.69	1.48	1.02	33.92	16.79	3.45
5500.00	10.50	20.92	8.35	13.36	1.47	1.02	33.27	17.75	3.44
5600.00	10.67	21.34	8.50	13.68	1.51	1.03	33.63	17.27	3.51
5700.00	10.57	21.11	8.18	13.01	1.46	1.03	33.71	17.19	3.51
5800.00	10.48	20.92	7.96	12.52	1.43	1.03	33.58	17.27	3.59
5900.00	10.40	20.86	7.76	12.12	1.41	1.03	33.69	17.15	3.70
6000.00	10.37	20.82	7.64	12.03	1.40	1.03	34.30	16.80	3.72
6500.00	10.12	20.52	6.68	10.59	1.30	1.04	33.96	16.82	4.00
7000.00	9.73	20.58	5.74	9.16	1.23	1.05	33.55	16.34	4.12
7500.00	8.78	20.45	5.07	7.72	1.19	1.04	32.63	15.47	4.72
8000.00	7.49	21.63	4.30	6.09	1.27	1.01	30.33	15.48	5.32

The RF switch adopts SPDT one-in-two-out, with a bandwidth of 9K-8G, and the RF switch has an internal integrated electrostatic protection circuit, which effectively protects the RF port. The switching logic of the corresponding RF switch can be referred to the following table, for the TX/RX switching of AD9361, you can refer to the schematic for the

actual connection relationship to correspond to the adjustment.

LS	CTRL	RFC-RFC1	RFC-RFC1
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

In addition, for the RF front-end we have involved 4-way LED indication, port setting 1 corresponds to LED on and port setting 0 corresponds to LED off. The following table lists the LED pin correspondences.

LED	Pin Name	Pin Position
LED_RF_TX1	IO_13P_MRCC_12	AE28
LED_RF_RX1	IO_13N_MRCC_12	AF28
LED_RF_TX2	IO_18P_12	AE25
LED_RF_RX2	IO_18N_12	AF25

Part 2.12.2: AD9361 Control and Data Ports

The AD9361 digital port is divided into data port and control port, the data port can be defined as LVCMOS, can also be defined as LVDS, LVCMOS communication rate is not high, so the project provided by Puzhi, default LVDS interface to define the data port, the following table lists the pin correspondence, you can also refer to the schematic.

AD9361 Interface	Pin Name	Pin Position
AD9631_TX_P0	IO_4P_10	AJ16
AD9631_TX_N0	IO_4N_10	AK16
AD9631_TX_P1	IO_15P_10	AF18
AD9631_TX_N1	IO_15N_10	AF17
AD9631_TX_P2	IO_12P_MRCC_10	AF14
AD9631_TX_N2	IO_12N_MRCC_10	AG14
AD9631_TX_P3	IO_2P_10	AH18
AD9631_TX_N3	IO_2N_10	AJ18
AD9631_TX_P4	IO_6P_10	AH17
AD9631_TX_N4	IO_6N_10	AH16
AD9631_TX_P5	IO_5P_10	AJ15
AD9631_TX_N5	IO_5N_10	AK15
AD9631_TX_FRAME_P	IO_8P_10	AH14
AD9631_TX_FRAME_N	IO_8N_10	AH13
AD9631_FB_CLK_P	IO_14P_MRCC_10	AF15
AD9631_FB_CLK_N	IO_14N_MRCC_10	AG15
AD9631_RX_P0	IO_22P_10	AB15
AD9631_RX_N0	IO_22N_10	AB14
AD9631_RX_P1	IO_19P_10	AC14
AD9631_RX_N1	IO_19N_10	AC13

AD9631_RX_P2	IO_16P_10	AE16
AD9631_RX_N2	IO_16N_10	AE15
AD9631_RX_P3	IO_17P_10	AE18
AD9631_RX_N3	IO_17N_10	AE17
AD9631_RX_P4	IO_23P_10	AC17
AD9631_RX_N4	IO_23N_10	AC16
AD9631_RX_P5	IO_3P_10	AJ14
AD9631_RX_N5	IO_3N_10	AJ13
AD9631_RX_FRAME_P	IO_18P_10	AD16
AD9631_RX_FRAME_N	IO_18N_10	AD15
AD9631_DATA_CLK_P	IO_13P_MRCC_10	AG17
AD9631_DATA_CLK_N	IO_13N_MRCC_10	AG16
AD9631_CLK_OUT	IO_13P_MRCC_11	AG21
AD9631_SPI_CLK	IO_16P_11	AK17
AD9631_SPI_nCS	IO_16N_11	AK18
AD9631_SPI_DI	IO_20P_11	W21
AD9631_SPI_DO	IO_20N_11	Y21
AD9631_nRST	IO_10N_11	AE21
AD9631_ENABLE	IO_17P_11	AH19
AD9631_EN_AGC	IO_17N_11	AJ19
AD9631_SYNC_IN	IO_23P_11	AA22
AD9631_TXNRX	IO_23N_11	AA23
AD9631_CTRL_OUT0	IO_11P_MRCC_10	AE13
AD9631_CTRL_OUT1	IO_11N_MRCC_10	AF13
AD9631_CTRL_OUT2	IO_9P_10	AD14
AD9631_CTRL_OUT3	IO_9N_10	AD13
AD9631_CTRL_OUT4	IO_21P_10	AB12
AD9631_CTRL_OUT5	IO_21N_10	AC12
AD9631_CTRL_OUT6	IO_24P_10	AB17
AD9631_CTRL_OUT7	IO_24N_10	AB16
AD9631_CTRL_IN0	IO_7P_10	AE12
AD9631_CTRL_IN1	IO_7N_10	AF12
AD9631_CTRL_IN2	IO_10P_10	AG12
AD9631_CTRL_IN3	IO_10N_10	AH12

Part 2.12.3: AD9361 Clock Circuit

The input clock of AD9361 adopts 40M VCTCXO with an accuracy of up to 0.1ppm. In addition, the board has reserved ADF4002BRUZ chip, so if there is a higher requirement for the clock accuracy, it can be adjusted by inputting it to ADF4002BRUZ through RF header. For detailed use of the clock you can refer to the schematic.

Part 2.13: PPS and Clock Inputs

The P201M/P203M designed a PPS input and 10M clock input circuit, this circuit from the same mmcx interface input, RC circuit with the FPGA's IO control to select the PPS and the clock circuit on and off, in addition to the 10M clock signal is also connected to the ADF4002, to do the clock correction.PPS and the clock were connected to the FPGA's The PPS and clock are connected to the following FPGA pins:

Signal Name	Pin Name	Pin Position
PPS-IN	IO_12P_MRCC_35	K17
10M_FPGA	IO_12P_MRCC_34	U18
EN_10M_FPGA	IO_18N_13	Y11
EN_10M_CLKIN	IO_18P_13	W11

Part 2.14: IO Expansion Ports

The 12P 2.54mm pitch row of pins is designed on the carrier board for the connection of the expansion signals, the following table marks the location of the chip where the signals are located, refer to the schematic section for detailed connections.

IO Interface	Pin Name	Pin Position	Level Standards
1	5V		Power
2	GND		GND
3	IO_15P_35	F19	3.3V
4	IO_15N_35	F20	
5	IO_20P_35	G19	
6	IO_20N_35	G20	
7	IO_23P_35	M14	
8	IO_23N_35	M15	
9	IO_17P_35	J20	
10	IO_17N_35	H20	
11	IO_20P_13	Y12	1.8V
12	IO_20N_13	Y13	

Part 2.15: User LED

The P201M/P203M has one LED reserved for user-defined use, LED high level on,LED low level off. The following table lists the pin correspondences of the LEDs, for a more detailed description you can refer to the schematic.

LED Pin	Pin Name	Pin Position
LED1	IO_0_35	G14