Ver 1.0

BQ7K Series FPGA

Datasheet

Part Number: BQ7K325TBG900、BQ7K410TBG900

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	20220121		Initial Release.	

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1. Product Description

1.1 Features

- **Fully compatible with Kintex7 series of Xilinx and higher security**
  - Optimized for best price-performance
  - Speed grade same with Kintex7 series "-1M"
  - Solve the "StarBleed" vulnerability at the hardware level, provide higher security for users
- **Configurable Logic Block（CLB）**
  - Real 6-input look-up tables (LUTs)
  - Memory capability within the LUT
  - Register and shift register functionality
- **Clock Management Tile (CMT)**
  - High-speed buffers and routing for low-skew clock distribution
  - Frequency synthesis and phase shifting
  - Low-jitter clock generation and jitter filtering
- **Block RAM**
  - Dual-port 36 Kb block RAM with port widths of up to 72
  - Programmable FIFO logic
  - Built-in optional error correction circuitry
- **Digital Signal Processing Slice（DSP）**
  - 25 × 18 two's complement multiplier/48-bit accumulator
  - Power saving pre-adder to optimize symmetrical filter applications
  - Optional pipelining, optional ALU, and dedicated buses for cascading
- **Input/Output（IOB）**
  - High-performance SelectIO technology with support for DDR3
  - High range (HR) I/O , from 1.2V to 3.3V
  - High performance (HP) I/O , from 1.2V to 1.8V
  - High-frequency decoupling capacitors for enhanced signal integrity
  - Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation
- **Low-Power Gigabit Transceivers（GTX）**
  - capable of 8.0 Gb/s line rates
  - Low-power mode to optimize chip-to-chip interfaces
- **Integrated Interface Blocks for PCI Express Designs**
  - Compliant to the PCI Express Base Specification 2.1 with Endpoint and Root Port capability
- **Configuration**
  - High-speed SPI and BPI Flash configuration
  - 256-bit AES encryption with HMAC/ SHA-256 authentication
  - Partial reconfiguration
- **XADC(Analog-to-Digital Converter)**
  - 12-bit 1 MSPS analog-to-digital converters (ADCs)
  - Up to 12 user-configurable analog inputs
  - On-chip temperature and power supply
  - voltage sensors
  - Continuous JTAG access to ADC measurements
- **28 nm CMOS Process Technology**
- **1.0V Core Voltage**
- **Reliability**
  - temperature range: –55℃ to +125℃
  - ESD (human body model): 2000V for regular I/O and power, 1500V for GTX Transceivers.

1.2 General Description

The BQ7K Series FPGA is a new generation of high performance SRAM FPGA. In addition to the advanced, high-performance logic fabric, BQ7K FPGAs contain many hard-IP system level blocks, including powerful 36-Kbit block RAM/FIFOs, 25 x 18 DSP slices, SelectIO technology with built-in digitally-controlled impedance, ChipSync source-synchronous interface blocks, system monitor functionality, enhanced clock management tiles with integrated mixed-mode clock manager and phase-locked loop clock generators, and advanced configuration options. Additional platform dependent features include power-optimized high-speed serial transceiver blocks for enhanced serial connectivity and integrated blocks for PCI Express. Most importantly, BQ7K FPGAs provide higher security for users by solving the "StarBleed" vulnerability at the hardware level. These features allow advanced logic designers to build high levels of performance and functionality into their FPGA-based systems. Built on a 28-nm CMOS process technology, BQ7K FPGAs are a programmable alternative to custom ASIC technology. The most advanced system designs require the programmable strength of FPGAs. BQ7K FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities.

The BQ7K series FPGAs currently include two products BQ7K325TBG900 and BQ7K410TBG900. The details are as follows：

Device	CLB		DSP slice	BRAM MAX（Kb）	CMT	PCIe	GTX	XADC	User IO	Package
	slice	Distributed RAM (Kb)								
BQ7K325TBG900	50950	4000	840	10620	10	1	16	1	500	PBGA900
BQ7K410TBG900	63550	5663	1540	28620	10	1	16	1	500	PBGA900

2. DC Characteristics

2.1 Absolute Maximum Ratings

a) Internal supply voltage（V_{CCINT}）：-0.5V～1.1V

b) Auxiliary supply voltage（V_{CCAUX}）：-0.5V～2.0V

c) Auxiliary supply voltage（V_{CCAUX_IO}）：-0.5V～2.06V

d) Supply voltage for the block RAM memories（V_{CCBRAM}）：-0.5V～1.1V

e) Output drivers supply voltage（V_{CCO}）：-0.5V～3.6V（3.3V HR I/O banks）
-0.5V～2.0V（1.8V HP I/O banks）

f) Key memory battery backup supply（V_{CCBATT}）：-0.5V～2.0V

g) Input reference voltage（V_{REF}）：-0.5 V～2.0 V

h) I/O input voltage（V_{IN}）：

-0.40V～VCCO +0.55V（3.3V HR I/O banks）

-0.55V～VCCO +0.55V（1.8V HP I/O banks）

-0.40V～2.625V（when V_{CCO} = 3.3V for VREF and differential I/O standards except TMDS_33）

i) Analog supply voltage for the GTX transmitter and receiver circuits（$V_{MGTAVCC}$）：-0.5V～1.1V

j) Analog supply voltage for the GTX transmitter and receiver termination circuits（$V_{MGTAVTT}$）：-0.5V～1.32V

k) Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers（$V_{MGTVCCAUX}$）：-0.5V～1.935V

l) GTX transceiver reference clock absolute input voltage（$V_{MGTREFCLK}$）：-0.5V～1.32V

m) Analog supply voltage for the resistor calibration circuit of the GTX transceiver column（$V_{MGTAVTTRCAL}$）：-0.5V～1.32V

n) Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage（V_{IN}）：-0.5V～1.26V

o) DC input current for receiver input pins DC coupled：

$I_{DCIN-FLOAT}$ =14mA（RX termination = floating）

$I_{DCIN-MGTAVTT}$ =12mA（RX termination =$V_{MGTAVTT}$）

$I_{DCIN-GND}$ =6.5mA（RX termination = GND）

p) DC output current for transmitter pins DC coupled：

$I_{DCOUT-FLOAT}$ =14mA（RX termination = floating

$I_{DCOUT-MGTAVTT}$ =12mA（RX termination =$V_{MGTAVTT}$）

q) XADC supply relative to GNDADC（V_{CCADC}）：-0.5V～2.0V

r) XADC reference input relative to GNDADC（V_{REFP}）：-0.5V～2.0V

s) Storage temperature（T_{STG}）：-65℃～150℃

t) Maximum soldering temperature（T_{SOL}）：220℃

u) Maximum junction temperature（T_J）：+125°C

v) Junction-to-case thermal resistance（θ_{JC}）：1℃/W

2.2 Recommended Operating Conditions

a) Internal supply voltage（V_{CCINT}）：0.97V～1.03V

b) Auxiliary supply voltage（V_{CCAUX}）：1.71V～1.89V

c) Auxiliary supply voltage（V_{CCAUX_IO}）：

1.71V～1.89V（Auxiliary supply voltage when set to 1.8V）

1.94V～2.06V（Auxiliary supply voltage when set to 2.0V）

d) Block RAM supply voltage（V_{CCBRAM}）：0.97V～1.03V

e) Supply voltage（V_{CCO}）：

1.14V～3.465V（3.3V HR I/O banks）

1.14V～1.89V（1.8V HP I/O banks）

f) I/O input voltage（V_{IN}）：

-0.20V～VCCO +0.2V

-0.20V～2.625V（when V_{CCO} = 3.3V for VREF and differential I/O standards except TMDS_33）

g) Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode（I_{IN}）：10mA

h) Battery voltage（V_{CCBATT}）：1.0V～1.89V

i) Analog supply voltage for the GTX transceiver QPLL frequency range（$V_{MGTAVCC}$）：1.05V～1.08V

j) Analog supply voltage for the GTX transmitter and receiver termination circuits（$V_{MGTAVTT}$）：1.17V～1.23V

k) Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers（$V_{MGTVCCAUX}$）：1.75V～1.85V

l) Analog supply voltage for the resistor calibration circuit of the GTX transceiver column（$V_{MGTAVTTRCAL}$）：1.17V～1.23V

m) XADC supply relative to GNDADC（V_{CCADC}）：1.71V～1.89V

n) Externally supplied reference voltage（V_{REFP}）：1.20V～1.30V

o) Junction temperature（T_J）：-55°C～ +125°C

3. Pinout Information and Package

3.1 BQ7K325TBG900-PBGA900

As shown in Figure 3-1, the BQ7K325TBG900 device is available in the PBGA900 packages.

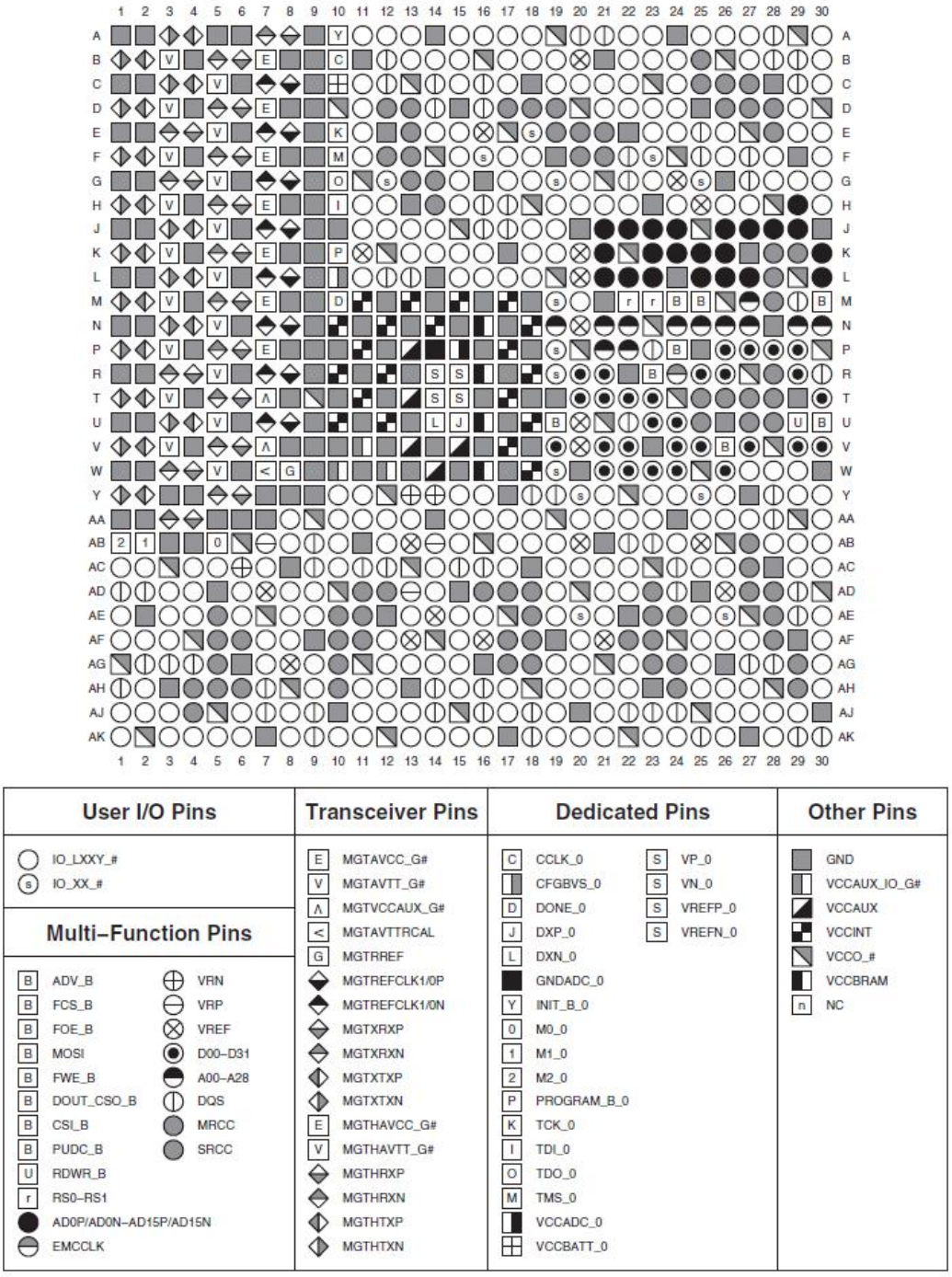
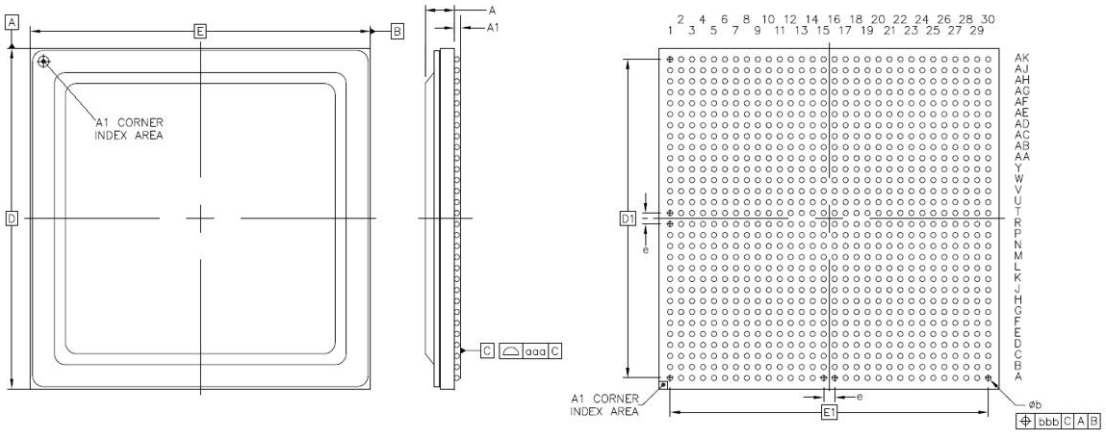


Figure 3-1 BQ7K325TBG900-PBGA900 Pinout Diagram

Figure 3-2 shows the package specifications for BQ7K325TBG900-PBGA900.



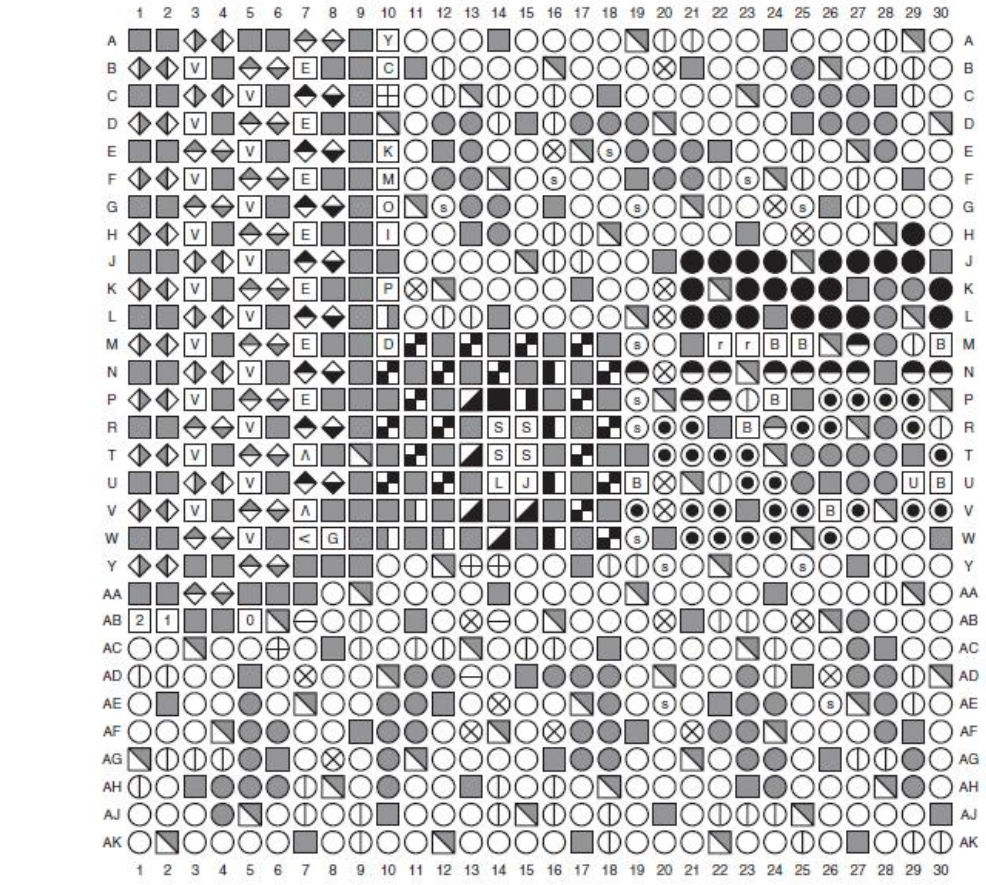
Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	2.9
A1	0.40	——	0.6
D/E	30.50	——	31.5
D1/E1	0.50	——	1.50
e	——	1.00	——
Ø *b*	0.5	——	0.7
aaa	——	——	0.20
bbb	——	——	0.30

Figure 3-2 Flip-Chip Package Specifications for BQ7K325TBG900-PBGA900

BQ7K325TBG900-PBGA900 pinout list is shown in Appendix II Table 1.

3.2 BQ7K410TBG900-PBGA900

As shown in Figure 3-3, the BQ7K410TBG900 device is available in the PBGA900 packages.



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

Figure 3-3 BQ7K410TBG900-PBGA900 Pinout Diagram

Figure 3-4 shows the package specifications for BQ7K410TBG900-PBGA900.

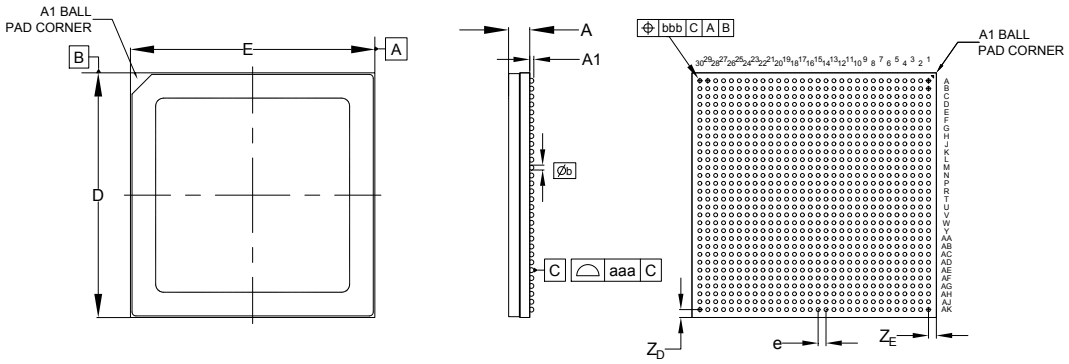


Figure 3-4 shows the package specifications for BQ7K410TBG900-PBGA900.

Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.53	——	2.83
A1	0.40	——	0.60
D/E	30.50	——	31.50
D1/E1	0.50	——	1.50
e	——	1.00	——
Ø *b*	0.50	——	0.70
aaa	——	——	0.20
bbb	——	——	0.30

Figure 3-4 Flip-Chip Package Specifications for BQ7K410TBG900-PBGA900

BQ7K410TBG900-PBGA900 pinout list is shown in Appendix II Table 2.

4. Architecture Features

This section briefly describes BQ7K series features.

4.1 Input/Output Blocks (SelectIO)

IOBs of BQ7K series FPGAs are programmable and include two types of SelectIO module according to the requirements of different application scenarios: high-performance (HP) and high-range (HR) I/O banks. The HP I/O banks are designed to meet the performance requirements of high-speed memory and other chip-to-chip interfaces with voltages up to 1.8V. The HR I/O banks are designed to support a wider range of I/O standards with voltages up to 3.3V.

Supported Features in the HR and HP I/O Banks：

Feature	HP I/O Banks	HR I/O Banks
3.3V I/O standards	N/A	Supported
2.5V I/O standards	N/A	Supported
1.8V I/O standards	Supported	Supported
1.5V I/O standards	Supported	Supported
1.35V I/O standards	Supported	Supported
1.2V I/O standards	Supported	Supported
LVDS signaling	Supported	Supported
24 mA drive option for LVCMOS18 and LVTTL outputs	N/A	Supported
VCCAUX_IO supply rail	Supported	N/A
Digitally-controlled impedance (DCI) and DCI cascading	Supported	N/A
Internal VREF	Supported	Supported
Internal differential termination (DIFF_TERM)	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	N/A
IDELAYCTRL	Supported	Supported
ISERDES	Supported	Supported
OSERDES	Supported	Supported
ZHOLD_DELAY	N/A	Supported

BQ7K series FPGAs contain following basic I/O logic resources:

- Combinatorial input/output
- 3-state output control
- Registered input/output
- Registered 3-state output control
- Double-Data-Rate (DDR) input/output
- DDR output 3-state control
- IDELAY provides users control of an adjustable, fine-resolution delay taps

- ODELAY provides users control of an adjustable, fine-resolution delay taps
- SAME_EDGE output DDR mode
- SAME_EDGE and SAME_EDGE_PIPELINED input DDR mode

The Select IO input, output, and 3-state drivers are contained in the input/output buffer (IOB). The HP banks have separate IDELAY and ODELAY blocks. The HR banks have the same logic elements as the HP banks except for the ODELAY block.

More details about Select IO can be found in Xilinx's official manual UG471: Select IO Resources.

4.2 Configurable Logic Block(CLB)

A configurable logic block(CLB) of a BQ7K series FPGA is composed of two slices. Each slice contains and is equivalent to:

- Four function generators
- Eight storage elements
- Arithmetic logic gate
- Large multiplexer
- Fast Carry Forward Chain

The function generator can be configured as 6-input LUT or as 5-input with dual-output LUT. The SLICEM in some CLBs can be configured as a 32-bit shift register (or two 16-bit registers) or 64-bit distributed RAM. In addition, the four storage elements can be configured as edge-triggered D-type flip-flops or level-sensitive latches. Each CLB has an internal fast carry chain function and can be connected to a switch matrix that accesses common wiring resources.

A CLB contains two slices, the two slices are located in two independent columns. They have independent carry chains and are not connected to each other. The lower Slice of the CLB is Slice0, and the upper Slice is Slice1 as shown in Figure 4-1.

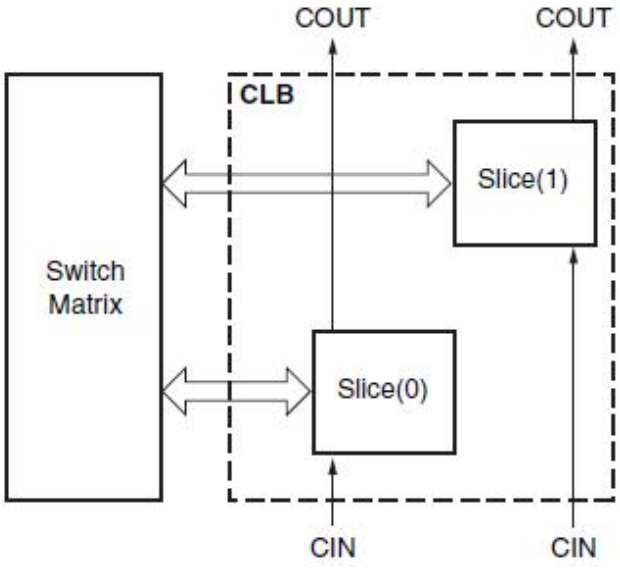


Figure 4-1 Slice in CLB

More details about CLB refer to Xilinx user guide UG474: 7 Series FPGAs Configurable Logic Block User Guide。

4.3 Global Clocking

The BQ7K series FPGAs clocking resources manage complex and simple clocking requirements with dedicated global and regional I/O and clocking resources. The clock management tiles (CMT) provide clock frequency synthesis, deskew, and jitter filtering functionality.

The CMT includes a mixed-mode clock manager (MMCM) and a phase-locked loop (PLL). The CMT diagram (Figure 4-2) shows a high-level view of the connection between the various clock input sources and the MMCM/PLL. Each BQ7K series FPGA contains up to 10 CMTs, providing up to 20 total clock generator elements.

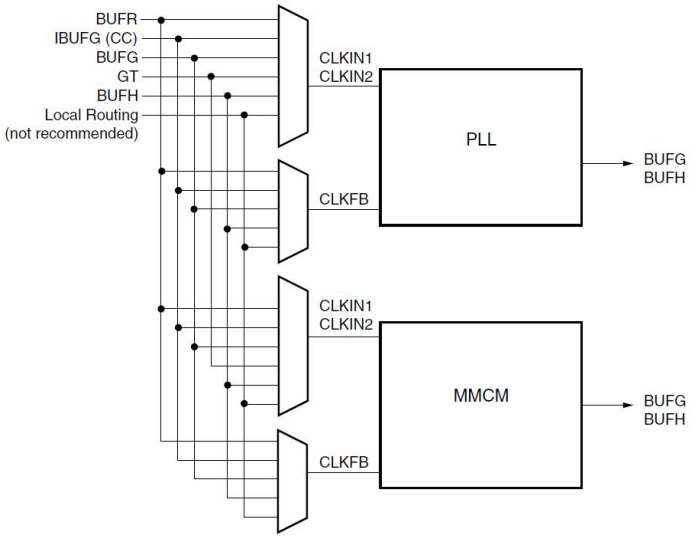


Figure 4-2 Block Diagram of the 7 Series FPGAs CMT

Figure 4-3 shows PLL primitives, detailed PLL block diagram, MMCM primitives and detailed MMCM block diagram. The PLL contains a subset of the MMCM functions. The MMCM supports following additional features:

- Direct HPC to BUFR or BUFIO using CLKOUT[0:3]
- Inverted clock outputs (CLKOUT[0:3]B)
- CLKOUT6
- CLKOUT4_CASCADE
- Fractional divide for CLKOUT0_DIVIDE_F
- Fractional multiply for CLKFBOUT_MULT_F
- Fine phase shifting
- Dynamic phase shifting

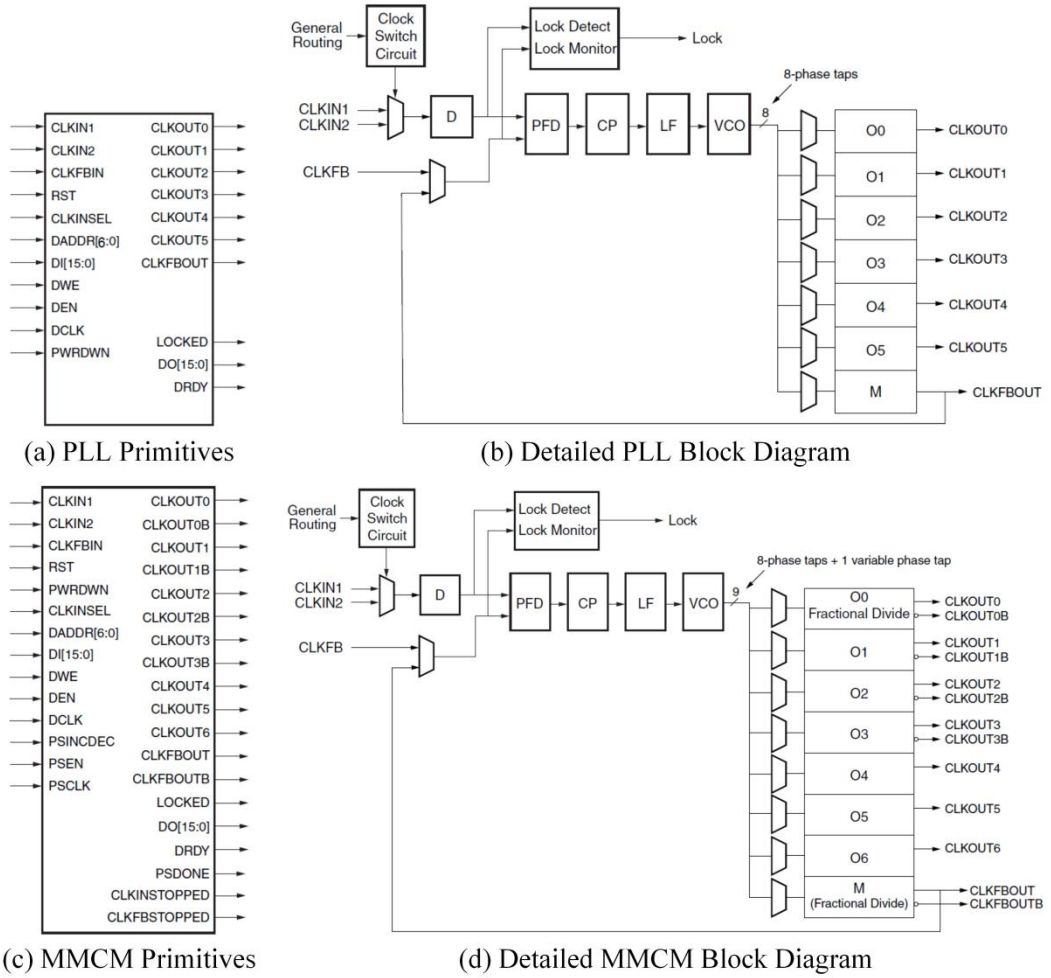


Figure 4-3 PLL Primitives, Detailed PLL Block Diagram, MMCM Primitives and Detailed MMCM Block Diagram

More details about clocking resources can be found in Xilinx's official manual UG472: 7 Series FPGAs Clocking Resources.

4.4 Block RAM

The block RAM stores up to 36 Kbits of data and can be configured as either two independent 18 Kb RAMs, or one 36 Kb RAM. Each 36 Kb block RAM can be configured as a 64K x 1 (when cascaded with an adjacent 36 Kb block RAM), 32K x 1, 16K x 2, 8K x 4, 4K x 9, 2K x 18, 1K x 36, or 512 x 72 in simple dual-port mode. Each 18 Kb block RAM can be configured as a 16K x 1, 8K x 2, 4K x 4, 2K x 9, 1K x 18 or 512 x 36 in simple dual-port mode. Power gating is enabled on each 18Kb block which is not instantiated in the design to save power.

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate)

operation increments the internal addresses and provides four handshaking flags: full, empty, almost full, and almost empty. The almost full and almost empty flags are freely programmable.

More details about BRAM refer to Xilinx User Guide UG473：7 Series FPGAs Memory Resources.

4.5 DSP Slice

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. BQ7K series FPGAs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 × 18 bit two's complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

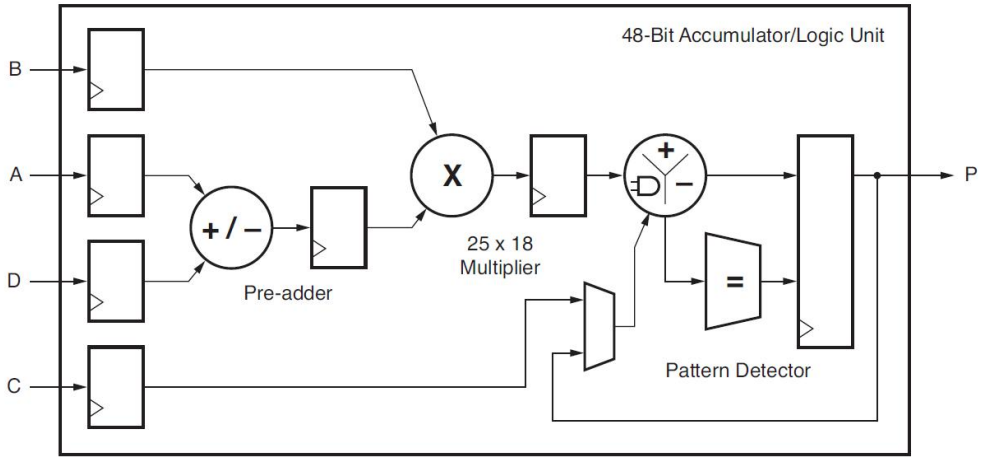


Figure 4-4 Basic Function Diagram of DSP Slice

More details about DSP refer to Xilinx User Guide UG479: 7 Series DSP48E1 Slice.

4.6 Integrated Block for PCI Express Designs

BQ7K series FPGA include Integrated Block for PCI Express. Highlights of the integrated blocks for PCI Express include：

- Compliant to the PCI Express Base Specification 2.1 with Endpoint and Root Port capability
- Supports Gen1 (2.5 Gb/s), Gen2 (5 Gb/s)
- Advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC

(ECRC) Advanced Error

Integrated Block for PCI Express can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 2.1. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom FPGA-to-FPGA communication via the PCI Express protocol. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. The integrated block consists of the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol. Figure 4-5 illustrates the block diagram.

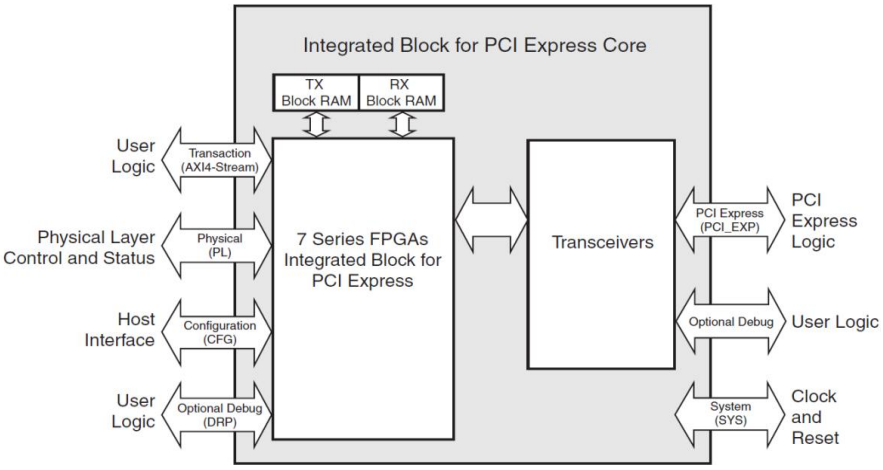


Figure 4-5 Integrated Block for PCI Express

More design details refer to Xilinx PG054：7 Series FPGAs Integrated Block for PCI Express v3.3.

4.7 Boundary Scan

Boundary-Scan instructions and associated data registers support a standard methodology for accessing and configuring BQ7K devices, complying with IEEE standards 1149.1 and 1532.

4.8 RocketIO GTX Transceivers

The GTX transceivers is a low-power and high-efficient four-channel transceivers, supporting line rates from 500 Mb/s to 8.0 Gb/s. The GTX transceiver supports a variety of high-speed serial communication protocols, including:

- PCI Express Revision 1.1/2.0
- Interlaken
- 10 Gb Attachment Unit Interface (XAUI), Reduced Pin Extended Attachment Unit Interface (RXAUI)
- Common Packet Radio Interface (CPRI)/Open Base Station Architecture Initiative (OBSAI)
- OC-48
- OTU-1,
- Serial RapidIO（SRIO）
- Serial Advanced Technology Attachment (SATA)/Serial Attached SCSI (SAS)
- Serial Digital Interface (SDI)

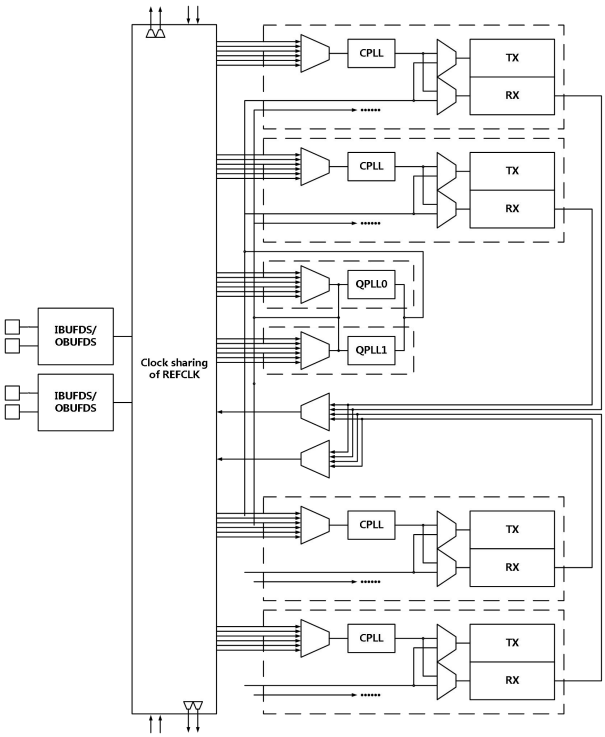


Figure 4-6 Overall Structure of GTX

The overall structure of the GTX lower-power four-channel high-speed serial transceiver is illustrated in Figure 4-6, including four channels and LC VCO phase-locked loop (QPLL). Each high-speed serial transceiver channel contains a transmit (TX) data channel and a receive (RX) data channel, together for realizing data transmit and reception. The channel is embedded with a channel phase-locked loop (CPLL) to realize the internal clock of a single channel management. The QPLL provides high-frequency and low-jitter reference clocks for four channels.

The overall structure of GTH transceiver consists of two parts: the shared part and the data path. The shared part includes the QPLL, band-gap reference source, and terminal impedance calibration module. The data path part includes the transmit data path and the receiver data path. The transmit data path performs channel coding on the input parallel data. After PISO and pre-emphasis processing, it is output as a high-speed differential serial signal. In the receiving data path, the high-speed differential serial signal is converted into parallel data after signal equalization processing, clock and data recovery. After channel decoding, clock correction, channel alignment and other operations, it is transmitted to the FPGA internal logic in parallel data.

More detail about rocketIO GTX transceivers can be found in Xilinx's official manual UG476: 7Series FPGAs GTX/GTH Transceivers.

4.9 XADC

The XADC is available in all BQ7K series FPGA devices. The XADC includes a dual 12-bit (for temperature range -40℃-100℃, 10-bit when temperature range is -55℃-125℃), 1 Mega sample per second(MSPS) ADC and on-chip sensors. By combining XADC with programmable logic, it is

possible to craft customized analog interfaces for a wide range of applications. Most commonly used XADC functions are: 1) Sets up a predefined operating mode and a number of channels, the XADC automatically selects the channel for conversion and stores the results in the status registers based on the setting; 2) The XADC provides a digital averaging function that allows a user to average up to 256 individual measurements to produce a reading. Averaging the sensor measurements helps generate a noise-free measurement; 3) The XADC can be set to automatically generate alarm outputs when the defined operating ranges for the FPGA supply voltages and temperature are exceeded.

Figure 4-7 shows a block diagram of the XADC. The XADC is built around a dual 12-bit(for temperature range -40 ℃ -100 ℃ , 10-bit when temperature range is -55 ℃ -125 ℃), 1MSPS Analog-to-Digital Converter (ADC). When combined with a number of on-chip sensors, the XADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures. Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 users-electable analog inputs, known as auxiliary analog inputs (VAUXP[15:0], VAUXN[15:0]). Apart from a single dedicated analog input pair (VP/VN), the external analog inputs use dual-purpose I/O.

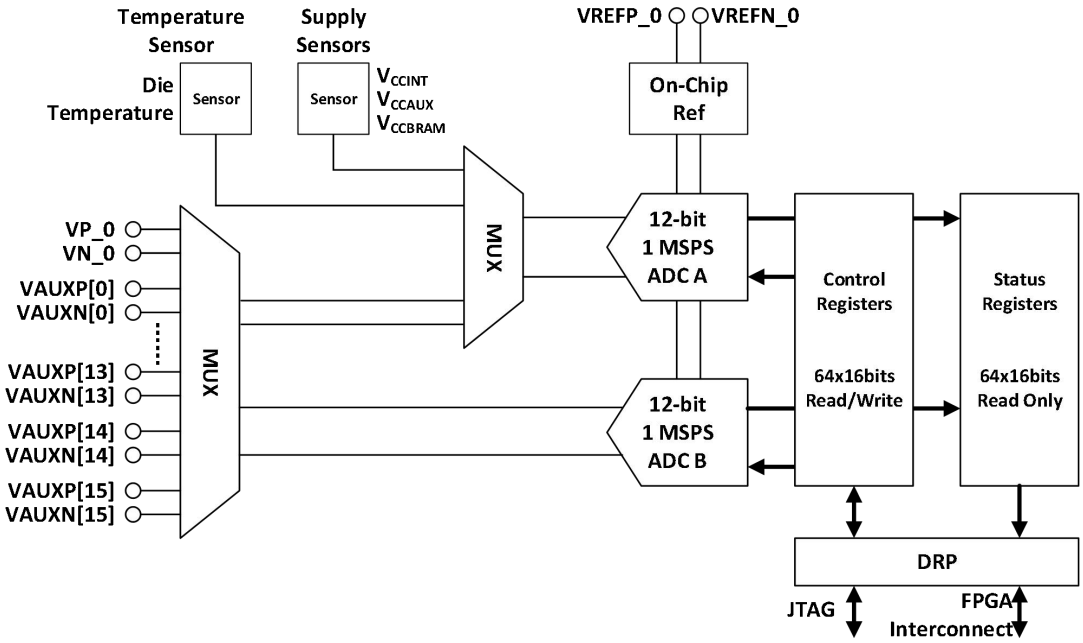


Figure 4-7 XADC Block Diagram

The XADC accommodates both unipolar and bipolar signals. The ADC conversion data is stored in dedicated registers called status registers. These registers are accessible via the FPGA interconnect using a 16-bit synchronous read and write port called the Dynamic Reconfiguration Port (DRP). ADC conversion data is also accessible via the JTAG TAP. In the latter case, users are not required to instantiate the XADC. If the XADC is not instantiated in a design, the device operates in a predefined mode (called default mode) that monitors on-chip temperature and supply voltages.

Control registers are used to configure the XADC operation. All XADC functionality is controlled through these registers. These control registers are initialized using the XADC attributes when the XADC is instantiated in a design. The configuration registers can be modified through the DRP after the FPGA has been configured.

The read-only status registers contain the results of an analog-to-digital conversion of the on-chip sensors and external analog channels. The status registers also store the maximum and minimum measurements recorded for the on-chip sensors from the device power-up or the last user reset of the XADC. At the end of an ADC conversion when the measurement is written to the status registers EOC (End of Conversion) or EOS (End of Sequence) signals transition to active High.

When the die temperature exceeds a factory set limit of 125°C or a user-defined threshold in Control Register, the Over-Temperature alarm logic output (OT) becomes active. The OT signal resets when the FPGA temperature has fallen below 70°C or a user-programmable limit in Control Register. When the automatic power-down feature is enabled, the OT signal can be used to trigger a device power down. When OT goes High, the FPGA enters power down mode which initiates a configuration shutdown sequence, disabling the device and asserts GHIGH to prevent any contention. When OT is de-asserted, GHIGH is de-asserted and the start-up sequence is initiated releasing all global resources.

For more details on XADC see UG480: Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide.

4.10 Configuration

BQ7K devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE-1532 and -1149)
- SPI mode (Serial Peripheral Interface standard Flash)
- BPI-up modes (Byte-wide Peripheral interface standard x8 or x16 NOR Flash)

In addition, BQ7K devices also support the following configuration options:

- Partial reconfiguration
- Built-in SEU detection and correction
- Built-in MultiBoot and safe-update capability
- 256-bit AES encryption with HMAC/SHA-256 authentication
- Parallel configuration bus width auto-detection

The configuration banks voltage select pin (CFGBVS) determines the I/O voltage operating range and voltage tolerance for the dedicated configuration bank0. If the VCCO_0 supply for bank 0 is

supplied with 2.5V or 3.3V, then the CFGBVS pin must be tied High. Tie CFGBVS to Low, only if the VCCO_0 for bank0 is less than or equal to 1.8V.

BQ7K have five configuration interfaces. Each configuration interface corresponds to one or more configuration modes and bus width, shown in Table 4-1.

Table 4-1 BQ7K Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1,2,4	Output
Master BPI	010	8,16	Output
Master SelectMAP	100	8,16	Output
JTAG	101	1	Not Applicable
Slave SelectMAP	110	8,16,32	Input
Slave Serial	111	1	Input

4.10.1 Serial Configuration Interface

In serial configuration modes, the FPGA is configured by loading one configuration bit per CCLK cycle:

- In Master Serial mode, CCLK is an output.
- In Slave Serial mode, CCLK is an input.

Figure 4-8 shows the basic BQ7K serial configuration interface. There are four methods of configuring an FPGA in serial mode:

- Master serial configuration
- Slave serial configuration
- Serial daisy-chain configuration
- Ganged serial configuration

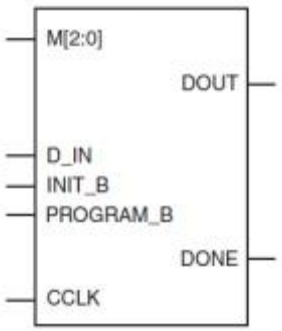


Figure 4-8 BQ7K FPGA Serial Configuration Interface

Table 4-2 BQ7K FPGA Serial Configuration Interface Pins

Pin Name	Direction	Type	Description
M[2:0]	Input	Dedicated	M[2:0] determine the configuration mode M[2:0] = 000：Master Serial Configuration； M[2:0] = 111：Slave Serial Configuration。
CCLK	Input or Output	Dedicated	CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode.
DIN	Input	Multi-function	DIN is the serial data input pin. By default, data from DIN is captured on the rising edge of CCLK.
DONE	Bidirectional	Dedicated	A High signal on the DONE pin indicates completion of the configuration sequence.
INIT_B	Bidirectional (open-drain)	Dedicated	Active-Low FPGA initialization pin or configuration error signal. Upon completing the FPGA initialization process, INIT_B is released to high-Z at which time an external resistor is expected to pull INIT_B High.
PROGRAM_B	Input	Dedicated	Active-Low reset to configuration logic
DOUT	Output	Multi-function	DOUT is the data output for a serial configuration daisy-chain.
PUDC_B	Input	Multi-function	Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. PUDC_B must be tied either directly, or via a ≤1 kΩ to VCCO_14 or GND. ***Caution!*** Do not allow this pin to float before and during configuration.

Slave Serial Configuration

Slave serial configuration is typically used for devices in a serial daisy chain or when configuring a single device from an external microprocessor or CPLD (See Figure 4-9). Design considerations are similar to Master serial configuration except for the direction of CCLK. CCLK must be driven from an external clock source.

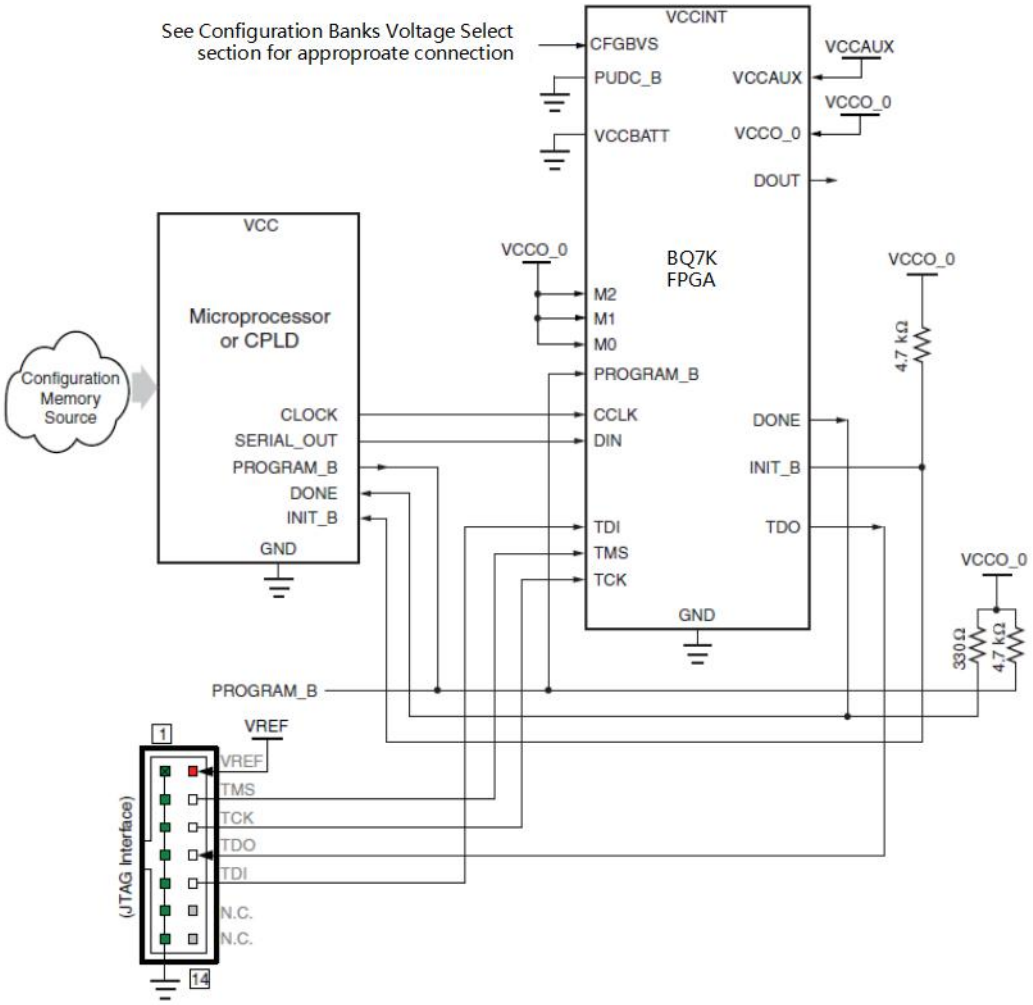


Figure4-9 Slave Serial Mode Configuration Example

Master Serial Configuration

The Master Serial configuration mode is the same as the Slave Serial configuration mode, except that the FPGA generates the CCLK. That is, the CCLK is an output in Master serial mode.

Serial Daisy Chains

Multiple BQ7K devices can be configured from a single configuration source by arranging the devices in a serial daisy chain. In a serial daisy chain, devices receive their configuration data through their D_IN pin, passing configuration data along to downstream devices through their DOUT pin. The device closest to the configuration data source is considered the most upstream device, while the device furthest from the configuration data source is considered the most downstream device.

In a serial daisy chain, the configuration clock is typically provided by the most upstream device in Master serial mode. All other devices are set for Slave serial mode. Figure 4-10 illustrates this configuration.

Another alternative is to use SPI mode for the first device. The daisy chain data is still sent out through DOUT in SPI mode.

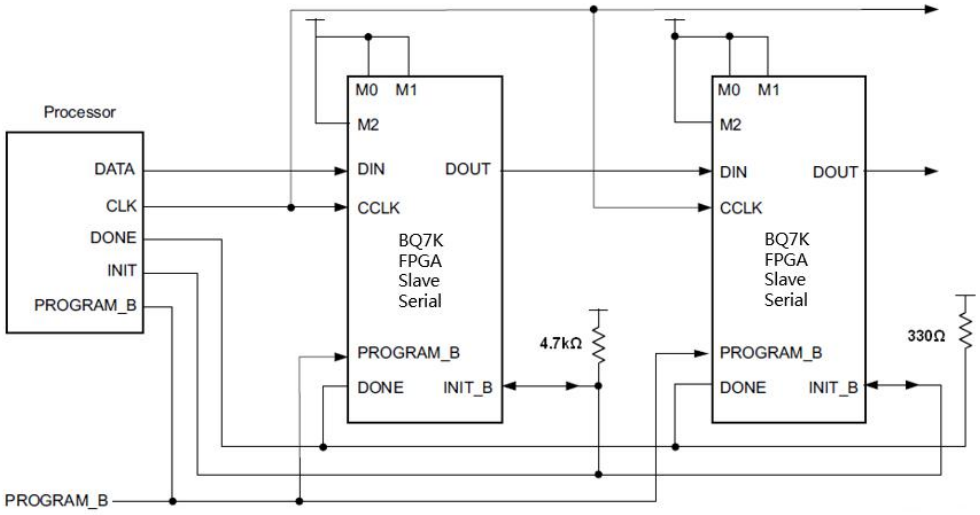


Figure4-10 Master/Slave Serial Mode Daisy Chain Configuration

The first device in a serial daisy chain is the last to be configured. CRC only checks the data for the current device, not for any others in the chain.

It is important that all DONE pins in a Slave serial daisy chain be connected. Only the first device in the serial daisy chain should have the DONE active pull-up driver enabled. Enabling the DONE driver on downstream devices causes contention on the DONE signal.

Mixed Serial Daisy Chains

BQ7K devices can be daisy-chained with BMTI BQ2V, BQR2V, BQ5V, BQR5V and the Xilinx Virtex, Spartan families. There are three important design considerations when designing a mixed serial daisy chain:

- Many older FPGA devices cannot accept as fast a CCLK frequency as a BQ7K device can generate. Select a configuration CCLK speed supported by all devices in the chain.
- BQ7K devices should always be at the beginning of the serial daisy chain, with older family devices located at the end of the chain.
- All BMTI device families have similar BitGen options. The guidelines provided for BQ7K BitGen options should be applied to all BMTI devices in a serial daisy chain.
- The number of configuration bits that a device can pass through its DOUT pin is limited. This limit varies for different families (Table 4-2). The sum of the bit stream lengths for all downstream devices must not exceed the number in Table 4-3 for each family.

Table 4-3 Maximum Number of Configuration Bits, Various Device Families

Architecture	Maximum DOUT Bits
BQ2V、BQR2V、BQ5V、BQR5V	4,294,967,264

Ganged Serial Configuration

More than one device can be configured simultaneously from the same bitstream using a ganged serial configuration setup (Figure 4-11). In this arrangement, the serial configuration pins are tied together such that each device sees the same signal transitions. One device is typically set for Master serial mode (to drive CCLK) while the others are set for Slave serial mode. For ganged serial

configuration, all devices must be identical. Configuration can be driven from a configuration PROM or from an external configuration controller.

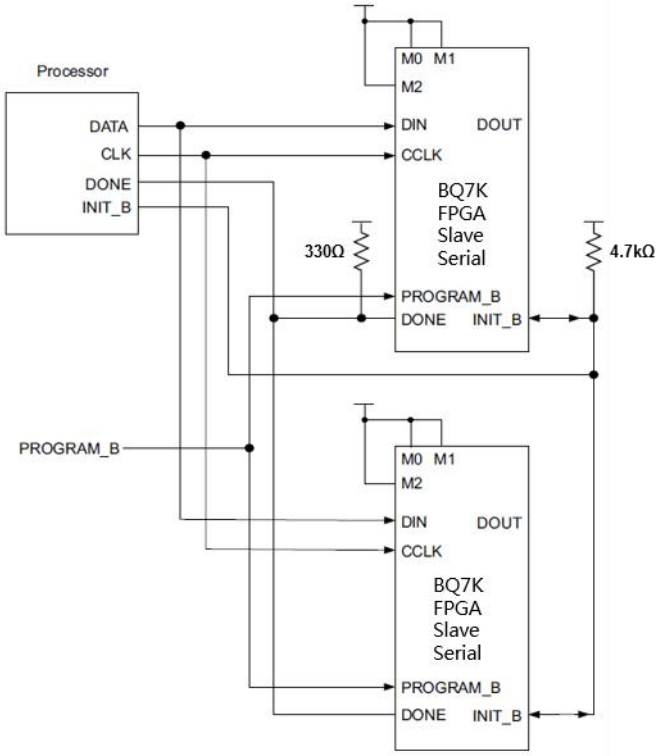


Figure 4-11 Ganged Serial Configuration

4.10.2 SelectMAP Configuration Interface

The SelectMAP configuration interface (Figure 4-12) provides an 8-bit, 16-bit, or 32-bit bidirectional data bus interface to the BQ7K configuration logic which can be used for both configuration and readback. The bus width of SelectMAP is automatically detected. CCLK is an output in Master SelectMAP mode; in Slave SelectMAP mode, CCLK is an input.

There are four methods of configuring an FPGA in SelectMAP mode:

- Single device Master SelectMAP
- Single device Slave SelectMAP
- Multiple device SelectMAP bus
- Multiple device ganged SelectMAP

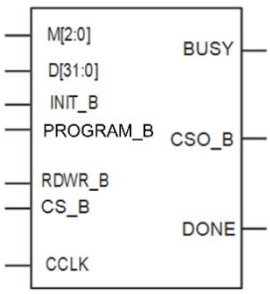


Figure 4-12 BQ7K Device SelectMAP Configuration Interface

Table 4-4 describes the SelectMAP configuration interface.

Table 4-4 BQ7K Device SelectMAP Configuration Interface Pins

Pin Name	Type	Dedicated or Dual-Purpose	Description
M[2:0]	Input	Dedicated	Mode pins - determine configuration mode
CCLK	Input and Output	Dedicated	Configuration clock source for all configuration modes except JTAG
D[31:0]	Three-State Bidirectional	Dual-Purpose	Configuration and readback data bus, clocked on the rising edge of CCLK.
DONE	Bidirectional, Open-Drain or active	Dedicated	Active-High signal indicating configuration is complete: 0= FPGA not configured 1= FPGA configured
INIT_B	Input or Output, Open-Drain	Dedicated	Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration. After the Mode pins are sampled, INIT_B is an open-drain, active-Low output indicating whether a CRC error occurred during configuration: 0= CRC error 1= No CRC error When the SEU detection function is enabled, INIT_B is optionally driven Low when a read back CRC error is detected.
PROGRAM_B	Input	Dedicated	Active-Low asynchronous full-chip reset.
CSI_B	Input	Dedicated	Active-Low chip select to enable the SelectMAP data bus (see "SelectMAP Data Loading") :0= SelectMAP data bus enabled 1= SelectMAP data bus disabled
RDWR_B	Input	Dedicated	Determines the direction of the D[x:0] data bus (see "SelectMAP Data Loading"): 0= inputs 1= outputs RDWR_B input can only be changed while CS_B is de-asserted, otherwise an ABORT occurs (see "SelectMAP ABORT").
CSO_B	Output	Dual-Purpose	Parallel daisy chain active-Low chip select output. Not used in single FPGA applications.
			RS0 and RS1 are high-Z during configuration. However, the FPGA can drive the RS0 and RS1 pins under two possible conditions. When the ConfigFallback option is enabled, the

RS[1:0]	Output	Dual-Purpose	FPGA drives RS0 and RS1 Low during the fallback configuration process that follows a detected configuration error. When a user-invoked MultiBoot configuration is initiated, the FPGA can drive the RS0 and RS1 pins to a user-defined state during the MultiBoot configuration process. If fallback is disabled (default) and if MultiBoot is not used, or if SPI mode is used, then RS0 and RS1 are high-Z and can be left unconnected.
PUDC_B	Input	Multi-function	Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. PUDC_B must be tied either directly, or via a ≤1 kΩ to VCCO_14 or GND. ***Caution!*** Do not allow this pin to float before and during configuration.

Single Device SelectMAP Configuration

For custom applications where a microprocessor or CPLD is used to configure a single BQ7K FPGA device, either Master SelectMAP mode (use CCLK from the FPGA) or Slave SelectMAP mode can be used (Figure 4-13). Slave SelectMAP mode is preferred.

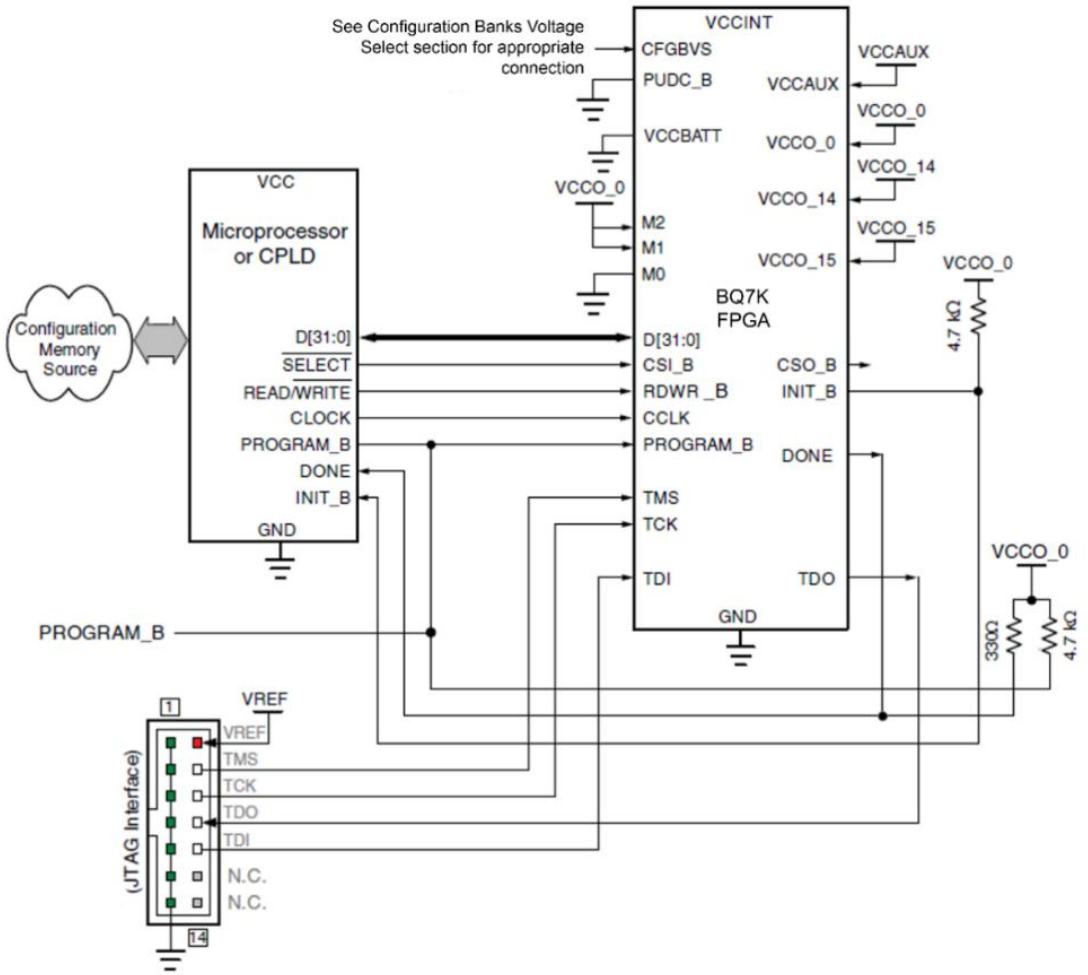


Figure 4-13 Single Slave Device SelectMAP Configuration from Microprocessor or CPLD Example

Multiple Device SelectMAP Configuration

Multiple BQ7K devices in Slave SelectMAP mode can be connected on a common SelectMAP bus (Figure 4-14). In a SelectMAP bus, the DATA, CCLK, RDWR_B, BUSY, PROGRAM_B, DONE, and INIT_B pins share a common connection between all of the devices. To allow each device to be accessed individually, the CSI_B (Chip Select) inputs must not be tied together. External control of the CSI_B signal is required and is usually provided by a microprocessor or CPLD.

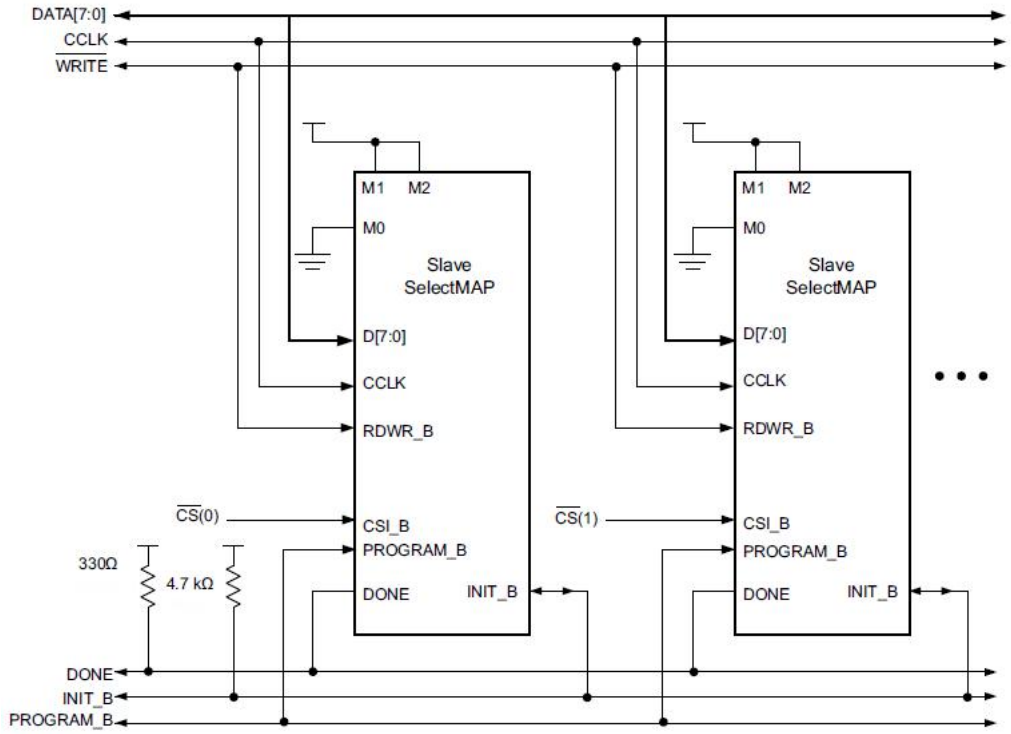


Figure 4-14 Multiple Slave Device Configuration on an 8-Bit SelectMAP Bus

Parallel Daisy Chain

BQ7K FPGA configuration supports parallel daisy-chain. Figure 4-15 shows an example schematic of the leading device in BPI mode. The leading device can also be in Master or Slave SelectMAP modes. The D, CCLK, RDWR_B, PROGRAM_B, DONE, and INIT_B pins share a common connection between all of the devices. The CSI_B pins are daisy chained.

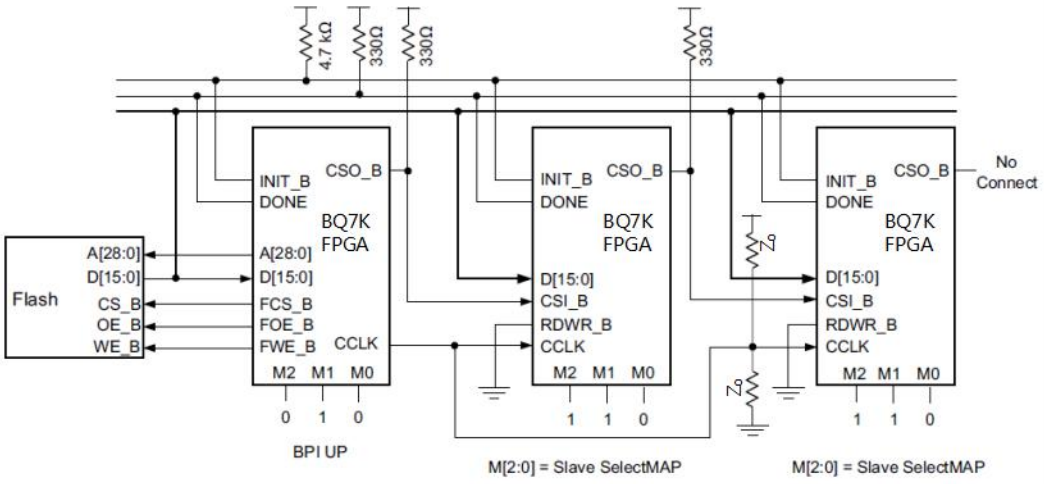


Figure 4-15 Parallel Daisy Chain

Within Figure 4-15, Z_0 is the characteristic impedance of CCLK transmission line.

Ganged SelectMAP

It is also possible to configure multiple devices simultaneously with the same configuration bitstream by using a ganged SelectMAP configuration. In a ganged SelectMAP arrangement, the CSI_B pins of two or more devices are connected together (or tied to ground), causing all devices to recognize data presented on the D pins. All devices can be set for Slave SelectMAP mode if an external oscillator is available, or one device can be designated as the Master device, as illustrated in Figure 4-16.

An external pull-up resistor is required on the common DONE signal. Designers must carefully focus on signal integrity due to the increased fanout. Signal integrity simulation is recommended.

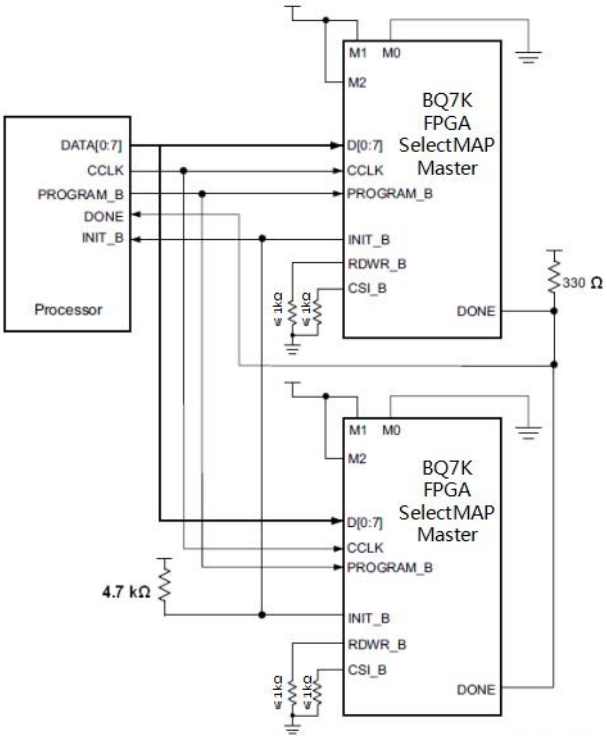


Figure 4-16 Ganged x8 SelectMAP Configuration

SelectMAP Data Loading

The SelectMAP interface allows for either continuous or non-continuous data loading. Data loading is controlled by the CSI_B, RDWR_B, CCLK, and BUSY signals.

CSI_B

The Chip Select input (CSI_B) enables the SelectMAP bus. When CSI_B is High, the 7 series device ignores the SelectMAP interface, neither registering any inputs nor driving any outputs. The D[31:0] pins are placed in a High-Z state, and RDWR_B is ignored.

- If CSI_B = 0, the device's SelectMAP interface is enabled.
- If CSI_B = 1, the device's SelectMAP interface is disabled.

If only one device is being configured through the SelectMAP and readback is not required, the CSI_B signal can be tied to ground.

RDWR_B

RDWR_B is an input to the BQ7K device that controls whether the data pins are inputs or outputs:

- If RDWR_B = 0, the data pins are inputs (writing to the FPGA).
- If RDWR_B = 1, the data pins are outputs (reading from the FPGA).

For configuration, RDWR_B must be set for write control (RDWR_B = 0). For readback, RDWR_B must be set for read control (RDWR_B = 1) while CSI_B is asserted.

Changing the value of RDWR_B from High to Low while CSI_B is Low also triggers an ABORT, and the configuration I/O changes from output to input asynchronously with no ABORT status readback. If readback is not needed, RDWR_B can be tied to ground or used for debugging with SelectMAP ABORT.

CCLK

All activity on the SelectMAP data bus is synchronous to CCLK. When RDWR_B is set for write control (RDWR_B = 0, Configuration), the FPGA samples the SelectMAP data pins on rising CCLK edges. When RDWR_B is set for read control (RDWR_B = 1, Readback), the FPGA updates the SelectMAP data pins on rising CCLK edges.

In Slave SelectMAP mode, configuration can be paused by stopping CCLK

SelectMAP ABORT

In monolithic devices an ABORT is an interruption in the SelectMAP configuration or readback sequence occurring when the state of RDWR_B changes while CSI_B is asserted as sampled by CCLK. During a configuration ABORT, internal status is driven onto the D[04:07] pins over the next four CCLK cycles. The other D pins are always High. After the ABORT sequence finishes, the user can resynchronize the configuration logic and resume configuration.

ABORT Status Word

During the configuration ABORT sequence, the device drives a status word onto the D[00:07] pins. The status bits do not bit-swap. The other data pins are always High. The key for the status word is given in Table 4-5.

Table 4-5 ABORT Status Word

Bit Number	Status Bit Name	Meaning
D07	CFGERR_B	Configuration error (active Low) 0 = A configuration error has occurred. 1 = No configuration error.
D06	DALIGN	Sync word received (active High) 0 = No sync word received. 1 = Sync word received by interface logic.
D05	RIP	Readback in progress (active High) 0 = No readback in progress. 1 = A readback is in progress.
D04	IN_ABORT_B	ABORT in progress (active Low) 0 = Abort is in progress. 1 = No abort in progress.
D03-D02	RSVD	Reserved
D01-D00	11	Fixed to ones.

There are two ways to resume configuration or readback after an ABORT:

- The device can be resynchronized after the ABORT completes.
- The device can be reset by pulsing PROGRAM_B Low at any time.

4.10.3 SPI Configuration Interface

In SPI serial Flash mode, M[2:0]=001. The BQ7K FPGA configures itself from an attached industry-standard SPI serial Flash PROM. Although SPI is a standard four-wire interface, various available SPI Flash memories use different read commands and protocol. Besides M[2:0], FS[2:0] pins are sampled by the INIT_B rising edge to determine the type of read commands used by SPI Flash. For BQ7K FPGA configurations, the default address always starts from 0. Figure 4-17 shows the SPI related configuration pins, and the standard connection between BQ7K devices and SPI Flash.

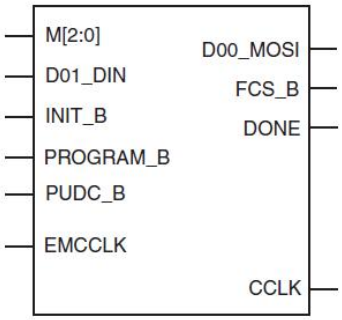


Figure 4-17 BQ7K Device SPI Configuration Interface

Table 4-6 describes the SPI configuration interface pins.

Table 4-6 BQ7K Device SPI Configuration Interface Pins

Pin Name	Type	Dedicated or Dual- Purpose	Description
M[2:0]	Input	Dedicated	Mode pins – 001for SPI
D01_DIN	Bidirectional	Dual- Purpose	DIN is the serial data input pin. By default, data from DIN is captured on the rising edge of CCLK.
CCLK	Output	Dedicated	Configuration clock output (to SPI).
D00_MOSI	Bidirectional	Dual- Purpose	FPGA (master) SPI mode output for sending commands to the SPI (slave) flash device.
DONE	Bidirectional	Dedicated	A High signal on the DONE pin indicates completion of the configuration sequence.
INIT_B	Input or Output, Open-Drain	Dedicated	Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration. After the Mode pins are sampled, INIT_B is an open-drain active Low output indicating whether a CRC error occurred during configuration: 0= CRC error

			1= No CRC error When the SEU detection function is enabled, INIT_B is optionally driven Low when read back CRC error is detected.
PROGRAM_B	Input	Dedicated	Active-Low asynchronous full-chip reset
FCS_B	Output	Dual- Purpose	Active-Low chip select output, clocked by the CCLK falling edge.
EMCCLK	Input	Dual- Purpose	Optional external clock input for running the configuration logic in a master mode (versus the internal configuration oscillator).
PUDC_B	Input	Multi-function	Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. PUDC_B must be tied either directly, or via a ≤1 kΩ to VCCO_14 or GND. ***Caution!*** Do not allow this pin to float before and during configuration.

Figure 4-18 shows the connections for a SPI configuration with a x1 or x2 data width. These connections are the same because the x2 mode uses the D00_MOSI pin as a dual-purpose Data In/Out pin. Daisy-chained configuration mode is only available in SPI.

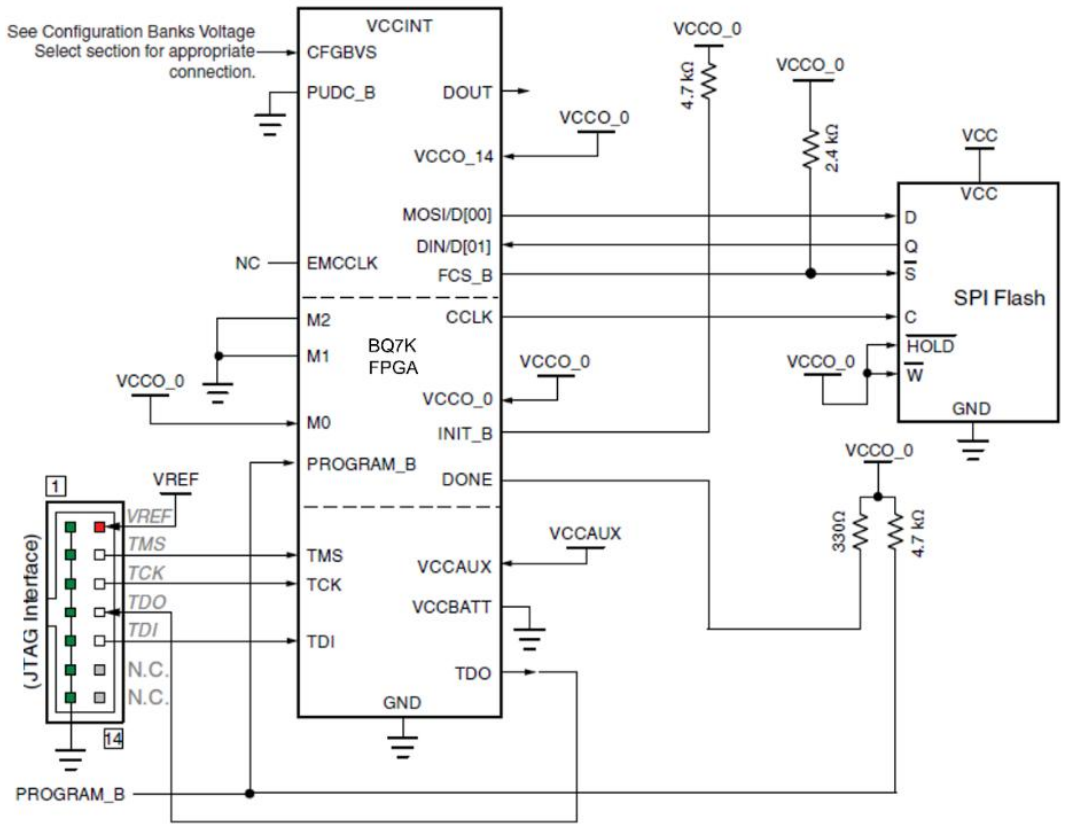


Figure 4-18 SPI x1/x2 Configuration Interface

BQ7K FPGA supports a x4 quad SPI master configuration width as shown in Figure 4-19.

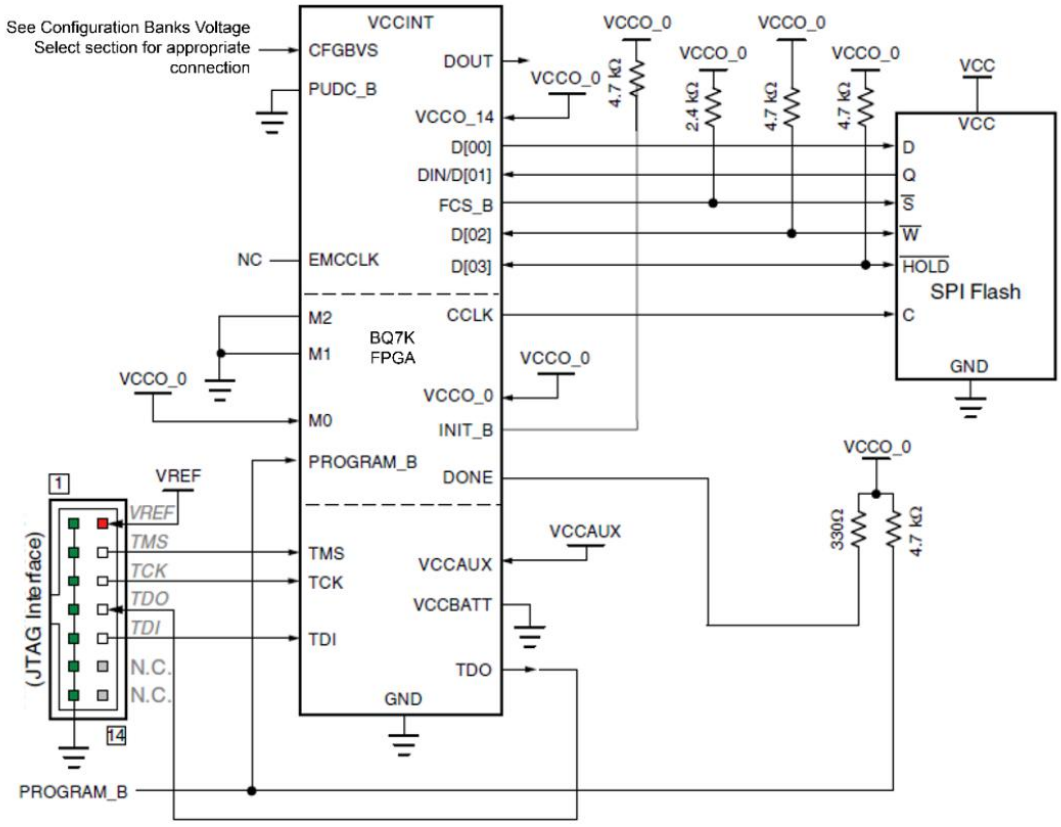


Figure 4-19 SPI x4 Configuration Interface

When configuration starts, the FPGA clocks data is imported on the rising edge. This continues until the FPGA reads the command in the early part of the bitstream which instructs it to change to the falling edge. This occurs before the command to change to external clocking or the command to change the master clock frequency. The falling edge clocking option is enabled by setting the option spi_fall_edge.

SPI Serial Daisy Chain

In a serial daisy chain application, the leading device can be in SPI mode and all downstream devices in Slave Serial mode. In this case, all configuration bitstreams can be stored inside one SPI device. The bitstream format for master and slave serial daisy chains is exactly the same.

4.10.4 Byte Peripheral Interface Parallel Flash Mode

In BPI (M[2:0]=100) mode, the BQ7K FPGA configures itself from an industry-standard parallel NOR Flash PROM, as illustrated in Figure 4-20. BPI configuration mode has two BPI flash read modes available: asynchronous and synchronous. Bus widths of x8 and x16 are supported.

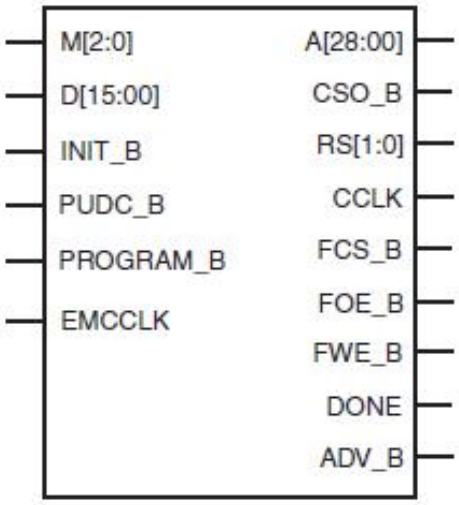


Figure 4-20 BQ7K BPI Configuration Interface

Asynchronous Read Mode Support

In the Master BPI configuration mode, the BQ7K FPGAs use the BPI flash asynchronous read mode by default to read bitstream data. After power-up, the Mode pins, M[2:0], are sampled when the FPGA's INIT_B output goes High. The Mode pins must be defined at the valid logic levels (Master BPI Configuration mode M[2:0] = 010) at this time. The PUDC_B pin must remain at a constant logic level throughout the FPGA configuration. After the Master BPI configuration mode is determined, the FPGA drives the flash control signals (FWE_B High, FOE_B Low, and FCS_B Low). Although the CCLK output is not connected to the BPI flash device for BPI flash asynchronous read mode, the FPGA outputs an address after the rising edge of CCLK, and the data is still sampled on the next rising edge of CCLK. The timing parameters related to BPI use the CCLK pin as a reference. In the Master BPI mode, the address starts at 0 and increments by 1 until the DONE pin is asserted. If the address reaches the maximum value (29'h1FFFFFFF) and configuration is not done (DONE is not asserted), an error flag is raised in the status register, and fallback reconfiguration starts.

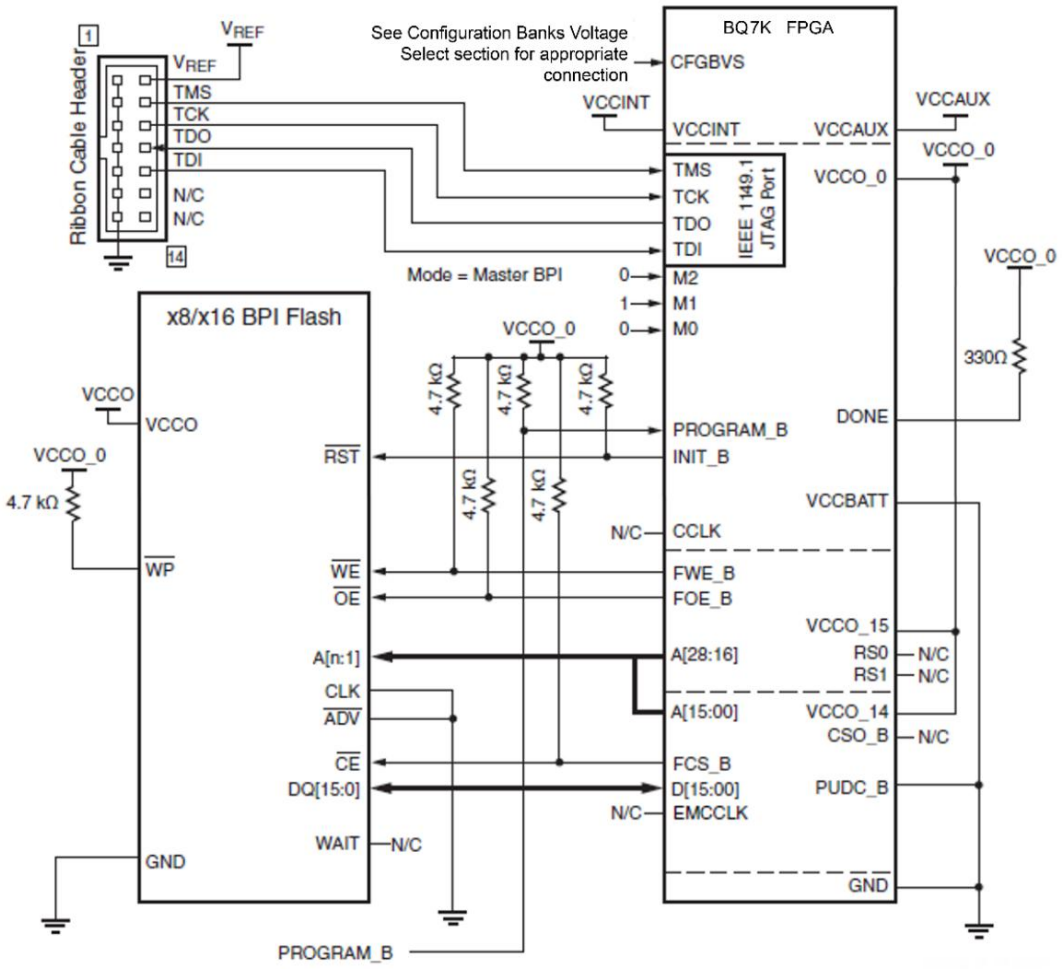


Figure 4-21 BQ7K BPI Asynchronous Configuration

Synchronous Read Mode Support

The BQ7K FPGA Master BPI configuration mode with synchronous read is the fastest direct flash configuration option without the need for customized external control logic. The FPGA starts in asynchronous read mode, using the default CCLK frequency, and the bitstream header determines if the read mode continues asynchronously or if it switches to the faster synchronous read mode. Bitstream commands initiate the switch from asynchronous read to synchronous read if the BPI_ sync_ mode option is set. There are two available settings for the option: Type1 or Type2. Type1 is used to set the G18F flash family synchronous and latency bits and Type2 is used to set the P30/P33. The switch to synchronous mode is done by the FPGA controller, which performs an asynchronous write to the BPI flash configuration register to set the device into synchronous mode and initiate a bitstream reread. To support the synchronous read mode, the FPGA CCLK output is connected to the BPI flash device, and the ADV_B FPGA signal must be connected to the flash ADV signal.

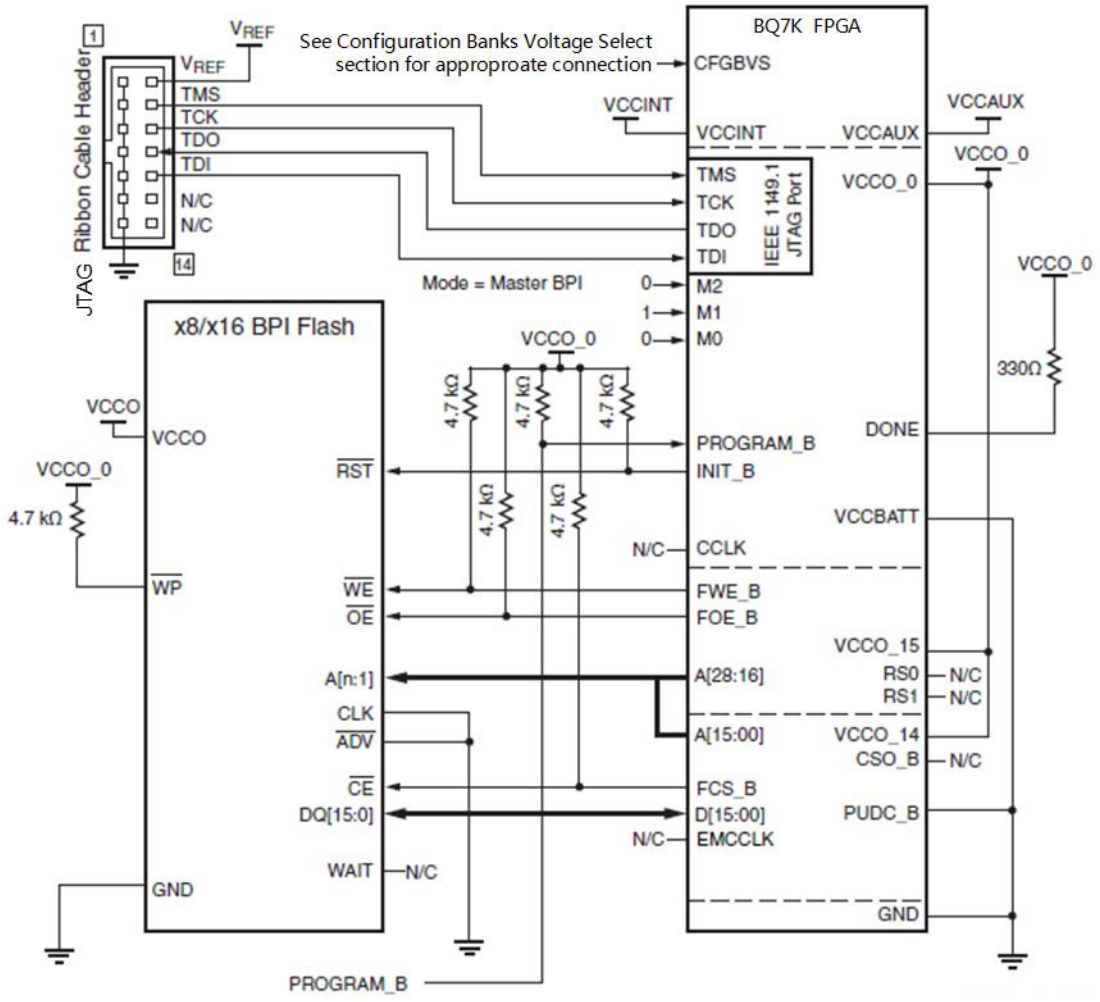


Figure4-21 BQ7K BPI Synchronous Configuration

Page Mode Support

Many NOR Flash devices support asynchronous page reads. The first access to a page usually takes the longest time (~100 ns), subsequent accesses to the same page take less time (~25 ns). The following parameters are bitstream programmable in BQ7K devices to take advantage of page reads and maximize the CCLK frequency:

- Page sizes of 1 (default), 4, or 8.
- If the actual Flash page size is larger than 8, the value of 8 should be used to maximize the efficiency.
- First access CCLK cycles of 1 (default), 2, 3, or 4. CCLK cycles must be 1 if the page size is 1.
- CCLK frequency

For more details on configuration, see UG470: 7 Series FPGAs Configuration User Guide .

5. Electrical Characteristics

Table 5-1 DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	MAX	Units
IREF	VREF leakage current per pin		15	μA
IL	Input or output leakage current per pin (sample-tested)		15	μA
IRPU	Pad pull-up (when selected) @ VIN = 0V, VCCO = 3.3V	90	330	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 2.5V	68	250	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 1.8V	34	220	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 1.5V	23	150	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 1.2V	12	120	μA
IRPD	Pad pull-down (when selected) @ VIN = 3.3V	68	330	μA
	Pad pull-down (when selected) @ VIN = 1.8V	45	180	μA

Table 5-2 SelectIO DC Input and Output Levels

I/O Standard	VIL		VIH		VOL	VOH	lOL	lOH
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	8(1)	-8(2)
HSTL_I_12	- 0.300	VREF-0.080	VREF + 0.080	VCCO + 0.300	25% VCCO	75% VCCO	6.3(3)	-6.3(4)
HSTL_I_18	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	8(1)	-8(2)
HSTL_II	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	16(1)	-16(2)
HSTL_II_18	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	16(1)	-16(2)
HSUL_12	- 0.300	VREF-0.130	VREF+ 0.130	VCCO + 0.300	20% VCCO	80% VCCO	0.1(1)	-0.1(2)
LVCMOS12	- 0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.400	VCCO-0.400	12(5)	-12(16)
LVCMOS15,	- 0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.450	VCCO-0.450	16(1)	-16(2)
LVCMOS18	- 0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.400	VCCO-0.400	24(5)	-24(6)

SSTL12	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	VCCO/2 - 0.150	VCCO/2 + 0.150	14.25 (3)	-14.25 (4)
SSTL135	- 0.300	VREF-0.090	VREF + 0.090	VCCO + 0.300	VCCO/2 - 0.150	VCCO/2 + 0.150	13.0(1)	-13.0(2)
SSTL15	- 0.300	VREF-0.100	VREF + 0.100	VCCO+ 0.300	VCCO/2 - 0.175	VCCO/2+ 0.175	13.0(1)	-13.0(2)
SSTL18_I	-0.300	VREF-0.125	VREF + 0.125	VCCO +0.300	VCCO/2 - 0.470	VCCO/2 + 0.470	8(1)	-8(2)
SSTL18_II	-0.300	VREF-0.125	VREF+ 0.125	VCCO +0.300	VCCO/2 - 0.600	VCCO/2 + 0.600	13.4(1)	-13.4(2)

(1)Test VOL in HP-I/O and HR-I/O, Supported drive current(positive).

(2)Test VOH in HP-I/O and HR-I/O, Supported drive current(negative).

(3)Test VOL only in HP-I/O , Supported drive current(positive).

(4)Test VOH only in HP-I/O, Supported drive current(negative).

(5)Test VOL only in HR-I/O, Supported drive current(positive).

(6)Test VOH only in HR-I/O, Supported drive current(negative).

Table 5-3 Differential IO DC Input and Output Levels

Symbol	DC Parameter	Conditions	Min	Max	Units
VOH	Output High voltage	LVDS are only supported in in HP I/O banks		1.675	V
VOL	Output Low voltage		0.825		V
VODIFF	Differential output voltage		247	600	mV
VOCM	Output common-mode voltage		1.000	1.425	V
VIDIFF	Differential input voltage		100	600	mV
VICM	Input common-mode voltage		0.300	1.425	V
VOH	Output High voltage	LVDS_25 are only supported in in HR I/O banks		1.675	V
VOL	Output Low voltage		0.700		V
VODIFF	Differential output voltage		247	600	mV
VOCM	Output common-mode voltage		1.000	1.425	V
VIDIFF	Differential input voltage		100	600	mV
VICM	Input common-mode voltage		0.300	1.500	V

Table 5-4 MMCM Switching Characteristics

Symbol	Description	Min	M MAX	Units
MMCM_FINMIN	MMCM Minimum input clock frequency	10		MHz
MMCM_FINMAX	MMCM Maximum input clock frequency		800	MHz

MMCM_FOUTMIN	MMCM minimum output frequency	4.69		MHz
MMCM_FOUTMAX	MMCM maximum output frequency		800	MHz
MMCM_FVCOTMIN	MMCM minimum VCO frequency	600		MHz
MMCM_FVCOTMAX	MMCM maximum VCO frequency		1200	MHz
MMCM_FPFDMIN	Minimum frequency at the phase frequency detector	10		MHz
MMCM_FPFDMAX	Maximum frequency at the phase frequency detector		450	MHz

Table 5-5 PLL Switching Characteristics

Symbol	Description	Min	MAX	Units
PLL_FINMIN	PLL Minimum input clock frequency	19		MHz
PLL_FINMAX	PLL Maximum input clock frequency		800	MHz
PLL_FOUTMIN	PLL minimum output frequency	6.25		MHz
PLL_FOUTMAX	PLL maximum output frequency		800	MHz
PLL_FVCOTMIN	PLL minimum VCO frequency	800		MHz
PLL_FVCOTMAX	PLL maximum VCO frequency		1600	MHz
PLL_FPFDMIN	Minimum frequency at the phase frequency detector	19		MHz
PLL_FPFDMAX	Maximum frequency at the phase frequency detector		450	MHz

Table 5-6 GTX Transceiver DC Specifications

Symbol	Description	Conditions	Min	MAX	Units
DVPPIN	Differential mode input voltage (DC coupled)	>10.3125 Gb/s	150	1250	mV
		6.6 Gb/s - 10.3125 Gb/s	150	1250	mV
		< 6.6 Gb/s	150	2000	mV
VCMIN	Common mode input voltage	2/3 VMGTAVTT			mV
DVPPOUT	Differential mode output voltage	Transmitter output swing is set to 4'b1010	1000		mV
VCMOUTDC	Common mode output voltage:	DC coupled		VMGTAVTT-DVPPOUT/4	mV
VIDIFF	Differential clock input voltage		100	600	mV

Table 5-7 GTX Transceiver AC Specifications

Symbol	Description	Conditions	Min	MAX	Units
FGTHMAX	Maximum GTX transceiver data rate			8.0	Gbps
FGTHMIN	Minimum GTX transceiver data rate		0.5		Gbps
FGCLK	Reference clock frequency range		60	670	MHz

6. Typical Applications

The application fields of BQ7K series FPGA include: communication transmission field, mainly used for high-speed interface circuit design of communication equipment, to complete high-speed data transceiver and exchange; high performance digital signal and image processing field, to achieve a variety of more complex mathematical algorithms, using FPGA internal resources to make it into the actual processing circuit; SOPC and other control processing fields, mainly use FPGA platform to build embedded system, and then carry out embedded system software development.

A typical kind of hardware system application of BQ7K series FPGA is shown in Figure 6-1. The system includes a BQ7K series FPGA, a PROM configuration memory, DDR3 data storage, PCIE circuit, SFP optical fiber communication interface, RS232/ RS485 interface, GTX and universal I/O extended interface, etc.

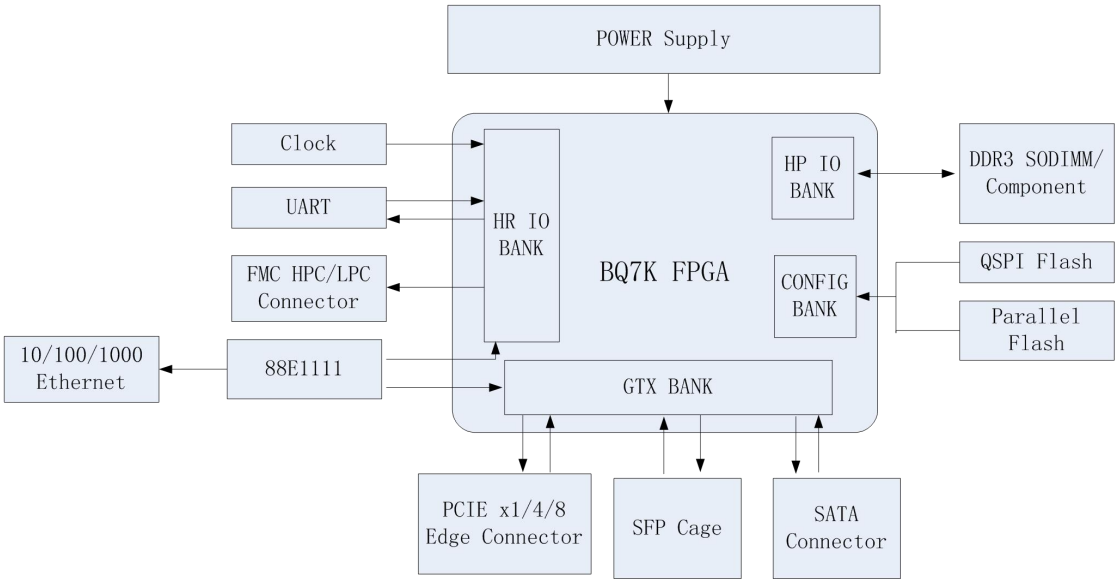


Figure 6-1 Typical Hardware Application

7. Notes for Application

7.1 Product Introduction of Application

BQ7K325TBG900, BQ7K410TBG900 and XILINX XQ7K325T, XQ7K410T are consistent in circuit structure, various electrical parameters, design process and development tools. BQ7K325TBG900, BQ7K410TBG900 have no special requirements. Xilinx Vivado development environment is recommended as development tools.

7.2 Attention Matters

a. The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO}. To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence;

b. The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

c. It's suggested that the actual frequency of the device should not exceed 80% of the maximum constraint frequency which can be passed, so as to keep sufficient design margin;

d. Maximum data transmission rate of PCI Express is not higher than 8.0Gbps;

e. Recommended analog supply voltage for the GTX transceiver QPLL frequency range （VMGTAVCC）：1.05V～1.08V

7.3 Product Protection

The packaging of the product is made of non-corrosive material, which can conduct electricity or be coated or impregnated with antistatic material, and has sufficient antistatic ability.

Under the condition of avoiding the direct influence of rain and snow, the packing boxes which contain the product can be transported by any means of transportation. But don't put them with acid, alkaline or other corrosive objects.

The storage environment of the packaged products shall meet the requirements in Section 8.1 of Q/W 657A－2007(temperature: 15℃~25℃, humidity: 25%~65%), without acid, alkaline or other corrosive gases, with good ventilation and corresponding anti-static measures.

7.3.1 Product Packaging

The device packaging shall at least meet the following requirements:

a. Made of non-corrosive material;

b. Strong enough to withstand the shock during handling;

c. Coated or impregnated with antistatic materials and has sufficient antistatic capacity;

d. Can firmly support the installed device in a certain position;

e. Can keep the lead of the device from deformation;

f. No sharp edges or corners;

g. Can safely and easily remove, check and replace the device;

h. Generally, do not use polyvinyl chloride, neoprene rubber, vinyl resin or polysulfide materials. It's advisable to use materials with low exhaust index and low dust particle shedding.

7.3.2 Transport and Storage

During transportation and storage, the device shall at least meet the following requirements:

a. Transportation: Under the condition of avoiding the direct influence of rain and snow, the packing boxes which contain the products can be transported by any means of transportation. But don't put them with acid, alkaline or other corrosive objects.

b. Storage: Packaged products shall be stored in a well-ventilated warehouse with ambient temperature of 16℃~28℃, relative humidity not greater than 30%~70%, and without acid, alkaline or other corrosive gases.

Appendix I Soldering Suggestion

Reflow soldering curve is shown as Figure 1.

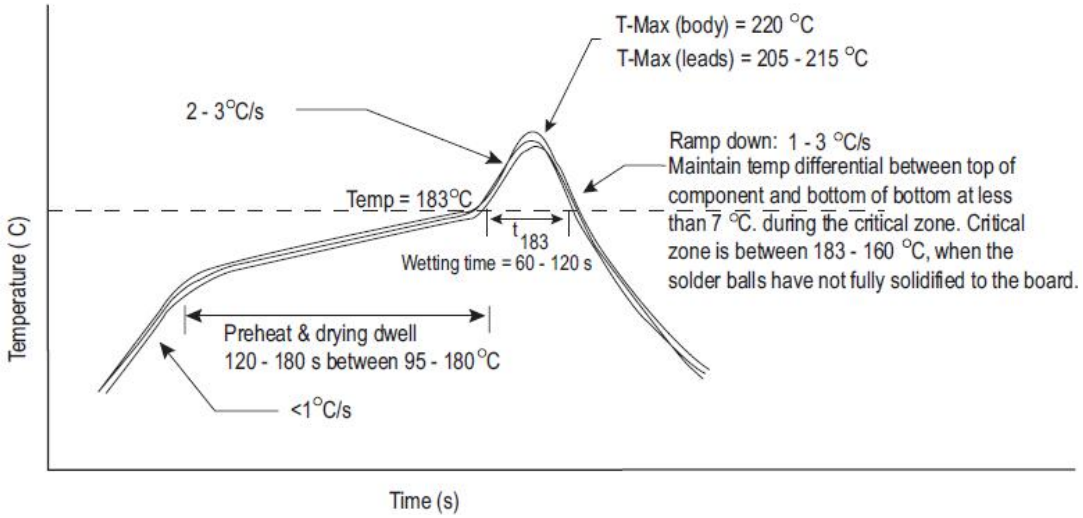


Figure 1 Reflow Soldering Curve

Appendix II Pinout Information

Table 1 BQ7K325TBG900-PBGA900 Pinout

Bank	**Pin name**	**Pin**	**I/O Type**
0	DXN_0	U14	CONFIG
0	VCCADC_0	P15	CONFIG
0	GNDADC_0	P14	CONFIG
0	DXP_0	U15	CONFIG
0	VREFN_0	R14	CONFIG
0	VREFP_0	T15	CONFIG
0	VP_0	R15	CONFIG
0	VN_0	T14	CONFIG
0	VCCBATT_0	C10	CONFIG
0	CCLK_0	B10	CONFIG
0	TCK_0	E10	CONFIG
0	TMS_0	F10	CONFIG
0	TDO_0	G10	CONFIG
0	TDI_0	H10	CONFIG
0	INIT_B_0	A10	CONFIG
0	PROGRAM_B_0	K10	CONFIG
0	CFGBVS_0	L10	CONFIG
0	DONE_0	M10	CONFIG
0	M2_0	AB1	CONFIG
0	M0_0	AB5	CONFIG
0	M1_0	AB2	CONFIG

Bank	Pin name	Pin	I/O Type
12	IO_0_12	Y20	HR
12	IO_L1P_T0_12	Y23	HR
12	IO_L1N_T0_12	Y24	HR
12	IO_L2P_T0_12	Y21	HR
12	IO_L2N_T0_12	AA21	HR
12	IO_L3P_T0_DQS_12	AB22	HR
12	IO_L3N_T0_DQS_12	AB23	HR
12	IO_L4P_T0_12	AA22	HR
12	IO_L4N_T0_12	AA23	HR
12	IO_L5P_T0_12	AC20	HR
12	IO_L5N_T0_12	AC21	HR
12	IO_L6P_T0_12	AA20	HR
12	IO_L6N_T0_VREF_12	AB20	HR
12	IO_L7P_T1_12	AB24	HR
12	IO_L7N_T1_12	AC25	HR
12	IO_L8P_T1_12	AC22	HR
12	IO_L8N_T1_12	AD22	HR
12	IO_L9P_T1_DQS_12	AC24	HR
12	IO_L9N_T1_DQS_12	AD24	HR
12	IO_L10P_T1_12	AD21	HR
12	IO_L10N_T1_12	AE21	HR
12	IO_L11P_T1_SRCC_12	AE23	HR
12	IO_L11N_T1_SRCC_12	AF23	HR
12	IO_L12P_T1_MRCC_12	AD23	HR
12	IO_L12N_T1_MRCC_12	AE24	HR
12	IO_L13P_T2_MRCC_12	AF22	HR
12	IO_L13N_T2_MRCC_12	AG23	HR
12	IO_L14P_T2_SRCC_12	AG24	HR
12	IO_L14N_T2_SRCC_12	AH24	HR
12	IO_L15P_T2_DQS_12	AJ24	HR
12	IO_L15N_T2_DQS_12	AK25	HR
12	IO_L16P_T2_12	AE25	HR
12	IO_L16N_T2_12	AF25	HR
12	IO_L17P_T2_12	AK23	HR
12	IO_L17N_T2_12	AK24	HR
12	IO_L18P_T2_12	AG25	HR
12	IO_L18N_T2_12	AH25	HR
12	IO_L19P_T3_12	AF20	HR
12	IO_L19N_T3_VREF_12	AF21	HR
12	IO_L20P_T3_12	AG22	HR

Bank	Pin name	Pin	I/O Type
12	IO_L20N_T3_12	AH22	HR
12	IO_L21P_T3_DQS_12	AJ22	HR
12	IO_L21N_T3_DQS_12	AJ23	HR
12	IO_L22P_T3_12	AG20	HR
12	IO_L22N_T3_12	AH20	HR
12	IO_L23P_T3_12	AH21	HR
12	IO_L23N_T3_12	AJ21	HR
12	IO_L24P_T3_12	AK20	HR
12	IO_L24N_T3_12	AK21	HR
12	IO_25_12	AE20	HR
13	IO_0_13	Y25	HR
13	IO_L1P_T0_13	Y26	HR
13	IO_L1N_T0_13	AA26	HR
13	IO_L2P_T0_13	W27	HR
13	IO_L2N_T0_13	W28	HR
13	IO_L3P_T0_DQS_13	Y28	HR
13	IO_L3N_T0_DQS_13	AA28	HR
13	IO_L4P_T0_13	W29	HR
13	IO_L4N_T0_13	Y29	HR
13	IO_L5P_T0_13	AA27	HR
13	IO_L5N_T0_13	AB28	HR
13	IO_L6P_T0_13	AA25	HR
13	IO_L6N_T0_VREF_13	AB25	HR
13	IO_L7P_T1_13	AC29	HR
13	IO_L7N_T1_13	AC30	HR
13	IO_L8P_T1_13	Y30	HR
13	IO_L8N_T1_13	AA30	HR
13	IO_L9P_T1_DQS_13	AD29	HR
13	IO_L9N_T1_DQS_13	AE29	HR
13	IO_L10P_T1_13	AB29	HR
13	IO_L10N_T1_13	AB30	HR
13	IO_L11P_T1_SRCC_13	AD27	HR
13	IO_L11N_T1_SRCC_13	AD28	HR
13	IO_L12P_T1_MRCC_13	AB27	HR
13	IO_L12N_T1_MRCC_13	AC27	HR
13	IO_L13P_T2_MRCC_13	AG29	HR
13	IO_L13N_T2_MRCC_13	AH29	HR
13	IO_L14P_T2_SRCC_13	AE28	HR
13	IO_L14N_T2_SRCC_13	AF28	HR
13	IO_L15P_T2_DQS_13	AK29	HR

Bank	Pin name	Pin	I/O Type
13	IO_L15N_T2_DQS_13	AK30	HR
13	IO_L16P_T2_13	AE30	HR
13	IO_L16N_T2_13	AF30	HR
13	IO_L17P_T2_13	AJ28	HR
13	IO_L17N_T2_13	AJ29	HR
13	IO_L18P_T2_13	AG30	HR
13	IO_L18N_T2_13	AH30	HR
13	IO_L19P_T3_13	AC26	HR
13	IO_L19N_T3_VREF_13	AD26	HR
13	IO_L20P_T3_13	AJ27	HR
13	IO_L20N_T3_13	AK28	HR
13	IO_L21P_T3_DQS_13	AG27	HR
13	IO_L21N_T3_DQS_13	AG28	HR
13	IO_L22P_T3_13	AH26	HR
13	IO_L22N_T3_13	AH27	HR
13	IO_L23P_T3_13	AF26	HR
13	IO_L23N_T3_13	AF27	HR
13	IO_L24P_T3_13	AJ26	HR
13	IO_L24N_T3_13	AK26	HR
13	IO_25_13	AE26	HR
14	IO_0_14	R19	HR
14	IO_L1P_T0_D00_MOSI_14	P24	HR
14	IO_L1N_T0_D01_DIN_14	R25	HR
14	IO_L2P_T0_D02_14	R20	HR
14	IO_L2N_T0_D03_14	R21	HR
14	IO_L3P_T0_DQS_PUDC_B_14	R23	HR
14	IO_L3N_T0_DQS_EMCCLK_14	R24	HR
14	IO_L4P_T0_D04_14	T20	HR
14	IO_L4N_T0_D05_14	T21	HR
14	IO_L5P_T0_D06_14	T22	HR
14	IO_L5N_T0_D07_14	T23	HR
14	IO_L6P_T0_FCS_B_14	U19	HR
14	IO_L6N_T0_D08_VREF_14	U20	HR
14	IO_L7P_T1_D09_14	P29	HR
14	IO_L7N_T1_D10_14	R29	HR
14	IO_L8P_T1_D11_14	P27	HR
14	IO_L8N_T1_D12_14	P28	HR
14	IO_L9P_T1_DQS_14	R30	HR
14	IO_L9N_T1_DQS_D13_14	T30	HR
14	IO_L10P_T1_D14_14	P26	HR

Bank	Pin name	Pin	I/O Type
14	IO_L10N_T1_D15_14	R26	HR
14	IO_L11P_T1_SRCC_14	R28	HR
14	IO_L11N_T1_SRCC_14	T28	HR
14	IO_L12P_T1_MRCC_14	T26	HR
14	IO_L12N_T1_MRCC_14	T27	HR
14	IO_L13P_T2_MRCC_14	U27	HR
14	IO_L13N_T2_MRCC_14	U28	HR
14	IO_L14P_T2_SRCC_14	T25	HR
14	IO_L14N_T2_SRCC_14	U25	HR
14	IO_L15P_T2_DQS_RDWR_B_14	U29	HR
14	IO_L15N_T2_DQS_DOUT_CSO_B_14	U30	HR
14	IO_L16P_T2_CSI_B_14	V26	HR
14	IO_L16N_T2_A15_D31_14	V27	HR
14	IO_L17P_T2_A14_D30_14	V29	HR
14	IO_L17N_T2_A13_D29_14	V30	HR
14	IO_L18P_T2_A12_D28_14	V25	HR
14	IO_L18N_T2_A11_D27_14	W26	HR
14	IO_L19P_T3_A10_D26_14	V19	HR
14	IO_L19N_T3_A09_D25_VREF_14	V20	HR
14	IO_L20P_T3_A08_D24_14	W23	HR
14	IO_L20N_T3_A07_D23_14	W24	HR
14	IO_L21P_T3_DQS_14	U22	HR
14	IO_L21N_T3_DQS_A06_D22_14	U23	HR
14	IO_L22P_T3_A05_D21_14	V21	HR
14	IO_L22N_T3_A04_D20_14	V22	HR
14	IO_L23P_T3_A03_D19_14	U24	HR
14	IO_L23N_T3_A02_D18_14	V24	HR
14	IO_L24P_T3_A01_D17_14	W21	HR
14	IO_L24N_T3_A00_D16_14	W22	HR
14	IO_25_14	W19	HR
15	IO_0_15	M19	HR
15	IO_L1P_T0_AD0P_15	J23	HR
15	IO_L1N_T0_AD0N_15	J24	HR
15	IO_L2P_T0_AD8P_15	L22	HR
15	IO_L2N_T0_AD8N_15	L23	HR
15	IO_L3P_T0_DQS_AD1P_15	K23	HR
15	IO_L3N_T0_DQS_AD1N_15	K24	HR
15	IO_L4P_T0_AD9P_15	L21	HR
15	IO_L4N_T0_AD9N_15	K21	HR
15	IO_L5P_T0_AD2P_15	J21	HR

Bank	Pin name	Pin	I/O Type
15	IO_L5N_T0_AD2N_15	J22	HR
15	IO_L6P_T0_15	M20	HR
15	IO_L6N_T0_VREF_15	L20	HR
15	IO_L7P_T1_AD10P_15	J29	HR
15	IO_L7N_T1_AD10N_15	H29	HR
15	IO_L8P_T1_AD3P_15	J27	HR
15	IO_L8N_T1_AD3N_15	J28	HR
15	IO_L9P_T1_DQS_AD11P_15	L30	HR
15	IO_L9N_T1_DQS_AD11N_15	K30	HR
15	IO_L10P_T1_AD4P_15	K26	HR
15	IO_L10N_T1_AD4N_15	J26	HR
15	IO_L11P_T1_SRCC_AD12P_15	L26	HR
15	IO_L11N_T1_SRCC_AD12N_15	L27	HR
15	IO_L12P_T1_MRCC_AD5P_15	L25	HR
15	IO_L12N_T1_MRCC_AD5N_15	K25	HR
15	IO_L13P_T2_MRCC_15	K28	HR
15	IO_L13N_T2_MRCC_15	K29	HR
15	IO_L14P_T2_SRCC_15	M28	HR
15	IO_L14N_T2_SRCC_15	L28	HR
15	IO_L15P_T2_DQS_15	M29	HR
15	IO_L15N_T2_DQS_ADV_B_15	M30	HR
15	IO_L16P_T2_A28_15	N27	HR
15	IO_L16N_T2_A27_15	M27	HR
15	IO_L17P_T2_A26_15	N29	HR
15	IO_L17N_T2_A25_15	N30	HR
15	IO_L18P_T2_A24_15	N25	HR
15	IO_L18N_T2_A23_15	N26	HR
15	IO_L19P_T3_A22_15	N19	HR
15	IO_L19N_T3_A21_VREF_15	N20	HR
15	IO_L20P_T3_A20_15	N21	HR
15	IO_L20N_T3_A19_15	N22	HR
15	IO_L21P_T3_DQS_15	P23	HR
15	IO_L21N_T3_DQS_A18_15	N24	HR
15	IO_L22P_T3_A17_15	P21	HR
15	IO_L22N_T3_A16_15	P22	HR
15	IO_L23P_T3_FOE_B_15	M24	HR
15	IO_L23N_T3_FWE_B_15	M25	HR
15	IO_L24P_T3_RS1_15	M22	HR
15	IO_L24N_T3_RS0_15	M23	HR
15	IO_25_15	P19	HR

Bank	Pin name	Pin	I/O Type
16	IO_0_16	F23	HR
16	IO_L1P_T0_16	B23	HR
16	IO_L1N_T0_16	A23	HR
16	IO_L2P_T0_16	E23	HR
16	IO_L2N_T0_16	D23	HR
16	IO_L3P_T0_DQS_16	F25	HR
16	IO_L3N_T0_DQS_16	E25	HR
16	IO_L4P_T0_16	E24	HR
16	IO_L4N_T0_16	D24	HR
16	IO_L5P_T0_16	F26	HR
16	IO_L5N_T0_16	E26	HR
16	IO_L6P_T0_16	G23	HR
16	IO_L6N_T0_VREF_16	G24	HR
16	IO_L7P_T1_16	B27	HR
16	IO_L7N_T1_16	A27	HR
16	IO_L8P_T1_16	C24	HR
16	IO_L8N_T1_16	B24	HR
16	IO_L9P_T1_DQS_16	B28	HR
16	IO_L9N_T1_DQS_16	A28	HR
16	IO_L10P_T1_16	A25	HR
16	IO_L10N_T1_16	A26	HR
16	IO_L11P_T1_SRCC_16	D26	HR
16	IO_L11N_T1_SRCC_16	C26	HR
16	IO_L12P_T1_MRCC_16	C25	HR
16	IO_L12N_T1_MRCC_16	B25	HR
16	IO_L13P_T2_MRCC_16	D27	HR
16	IO_L13N_T2_MRCC_16	C27	HR
16	IO_L14P_T2_SRCC_16	E28	HR
16	IO_L14N_T2_SRCC_16	D28	HR
16	IO_L15P_T2_DQS_16	C29	HR
16	IO_L15N_T2_DQS_16	B29	HR
16	IO_L16P_T2_16	D29	HR
16	IO_L16N_T2_16	C30	HR
16	IO_L17P_T2_16	B30	HR
16	IO_L17N_T2_16	A30	HR
16	IO_L18P_T2_16	E29	HR
16	IO_L18N_T2_16	E30	HR
16	IO_L19P_T3_16	H24	HR
16	IO_L19N_T3_VREF_16	H25	HR
16	IO_L20P_T3_16	G28	HR

Bank	Pin name	Pin	I/O Type
16	IO_L20N_T3_16	F28	HR
16	IO_L21P_T3_DQS_16	G27	HR
16	IO_L21N_T3_DQS_16	F27	HR
16	IO_L22P_T3_16	G29	HR
16	IO_L22N_T3_16	F30	HR
16	IO_L23P_T3_16	H26	HR
16	IO_L23N_T3_16	H27	HR
16	IO_L24P_T3_16	H30	HR
16	IO_L24N_T3_16	G30	HR
16	IO_25_16	G25	HR
17	IO_0_17	G19	HR
17	IO_L1P_T0_17	K18	HR
17	IO_L1N_T0_17	J18	HR
17	IO_L2P_T0_17	H20	HR
17	IO_L2N_T0_17	G20	HR
17	IO_L3P_T0_DQS_17	J17	HR
17	IO_L3N_T0_DQS_17	H17	HR
17	IO_L4P_T0_17	J19	HR
17	IO_L4N_T0_17	H19	HR
17	IO_L5P_T0_17	L17	HR
17	IO_L5N_T0_17	L18	HR
17	IO_L6P_T0_17	K19	HR
17	IO_L6N_T0_VREF_17	K20	HR
17	IO_L7P_T1_17	H21	HR
17	IO_L7N_T1_17	H22	HR
17	IO_L8P_T1_17	D21	HR
17	IO_L8N_T1_17	C21	HR
17	IO_L9P_T1_DQS_17	G22	HR
17	IO_L9N_T1_DQS_17	F22	HR
17	IO_L10P_T1_17	D22	HR
17	IO_L10N_T1_17	C22	HR
17	IO_L11P_T1_SRCC_17	F21	HR
17	IO_L11N_T1_SRCC_17	E21	HR
17	IO_L12P_T1_MRCC_17	F20	HR
17	IO_L12N_T1_MRCC_17	E20	HR
17	IO_L13P_T2_MRCC_17	D17	HR
17	IO_L13N_T2_MRCC_17	D18	HR
17	IO_L14P_T2_SRCC_17	E19	HR
17	IO_L14N_T2_SRCC_17	D19	HR
17	IO_L15P_T2_DQS_17	D16	HR

Bank	Pin name	Pin	I/O Type
17	IO_L15N_T2_DQS_17	C16	HR
17	IO_L16P_T2_17	G18	HR
17	IO_L16N_T2_17	F18	HR
17	IO_L17P_T2_17	C17	HR
17	IO_L17N_T2_17	B17	HR
17	IO_L18P_T2_17	G17	HR
17	IO_L18N_T2_17	F17	HR
17	IO_L19P_T3_17	C20	HR
17	IO_L19N_T3_VREF_17	B20	HR
17	IO_L20P_T3_17	A16	HR
17	IO_L20N_T3_17	A17	HR
17	IO_L21P_T3_DQS_17	A20	HR
17	IO_L21N_T3_DQS_17	A21	HR
17	IO_L22P_T3_17	B18	HR
17	IO_L22N_T3_17	A18	HR
17	IO_L23P_T3_17	B22	HR
17	IO_L23N_T3_17	A22	HR
17	IO_L24P_T3_17	C19	HR
17	IO_L24N_T3_17	B19	HR
17	IO_25_17	E18	HR
18	IO_0_18	G12	HR
18	IO_L1P_T0_18	L16	HR
18	IO_L1N_T0_18	K16	HR
18	IO_L2P_T0_18	L15	HR
18	IO_L2N_T0_18	K15	HR
18	IO_L3P_T0_DQS_18	L12	HR
18	IO_L3N_T0_DQS_18	L13	HR
18	IO_L4P_T0_18	K13	HR
18	IO_L4N_T0_18	J13	HR
18	IO_L5P_T0_18	K14	HR
18	IO_L5N_T0_18	J14	HR
18	IO_L6P_T0_18	L11	HR
18	IO_L6N_T0_VREF_18	K11	HR
18	IO_L7P_T1_18	H15	HR
18	IO_L7N_T1_18	G15	HR
18	IO_L8P_T1_18	J11	HR
18	IO_L8N_T1_18	J12	HR
18	IO_L9P_T1_DQS_18	J16	HR
18	IO_L9N_T1_DQS_18	H16	HR
18	IO_L10P_T1_18	H11	HR

Bank	Pin name	Pin	I/O Type
18	IO_L10N_T1_18	H12	HR
18	IO_L11P_T1_SRCC_18	H14	HR
18	IO_L11N_T1_SRCC_18	G14	HR
18	IO_L12P_T1_MRCC_18	G13	HR
18	IO_L12N_T1_MRCC_18	F13	HR
18	IO_L13P_T2_MRCC_18	D12	HR
18	IO_L13N_T2_MRCC_18	D13	HR
18	IO_L14P_T2_SRCC_18	F12	HR
18	IO_L14N_T2_SRCC_18	E13	HR
18	IO_L15P_T2_DQS_18	C12	HR
18	IO_L15N_T2_DQS_18	B12	HR
18	IO_L16P_T2_18	F11	HR
18	IO_L16N_T2_18	E11	HR
18	IO_L17P_T2_18	A11	HR
18	IO_L17N_T2_18	A12	HR
18	IO_L18P_T2_18	D11	HR
18	IO_L18N_T2_18	C11	HR
18	IO_L19P_T3_18	F15	HR
18	IO_L19N_T3_VREF_18	E16	HR
18	IO_L20P_T3_18	E14	HR
18	IO_L20N_T3_18	E15	HR
18	IO_L21P_T3_DQS_18	D14	HR
18	IO_L21N_T3_DQS_18	C14	HR
18	IO_L22P_T3_18	B13	HR
18	IO_L22N_T3_18	A13	HR
18	IO_L23P_T3_18	C15	HR
18	IO_L23N_T3_18	B15	HR
18	IO_L24P_T3_18	B14	HR
18	IO_L24N_T3_18	A15	HR
18	IO_25_18	F16	HR
32	IO_0_VRN_32	Y14	HP
32	IO_L1P_T0_32	AK16	HP
32	IO_L1N_T0_32	AK15	HP
32	IO_L2P_T0_32	AG15	HP
32	IO_L2N_T0_32	AH15	HP
32	IO_L3P_T0_DQS_32	AH16	HP
32	IO_L3N_T0_DQS_32	AJ16	HP
32	IO_L4P_T0_32	AF15	HP
32	IO_L4N_T0_32	AG14	HP
32	IO_L5P_T0_32	AH17	HP

Bank	Pin name	Pin	I/O Type
32	IO_L5N_T0_32	AJ17	HP
32	IO_L6P_T0_32	AE16	HP
32	IO_L6N_T0_VREF_32	AF16	HP
32	IO_L7P_T1_32	AJ19	HP
32	IO_L7N_T1_32	AK19	HP
32	IO_L8P_T1_32	AG19	HP
32	IO_L8N_T1_32	AH19	HP
32	IO_L9P_T1_DQS_32	AJ18	HP
32	IO_L9N_T1_DQS_32	AK18	HP
32	IO_L10P_T1_32	AD19	HP
32	IO_L10N_T1_32	AE19	HP
32	IO_L11P_T1_SRCC_32	AF18	HP
32	IO_L11N_T1_SRCC_32	AG18	HP
32	IO_L12P_T1_MRCC_32	AF17	HP
32	IO_L12N_T1_MRCC_32	AG17	HP
32	IO_L13P_T2_MRCC_32	AD18	HP
32	IO_L13N_T2_MRCC_32	AE18	HP
32	IO_L14P_T2_SRCC_32	AD17	HP
32	IO_L14N_T2_SRCC_32	AD16	HP
32	IO_L15P_T2_DQS_32	Y19	HP
32	IO_L15N_T2_DQS_32	Y18	HP
32	IO_L16P_T2_32	AA18	HP
32	IO_L16N_T2_32	AB18	HP
32	IO_L17P_T2_32	AB19	HP
32	IO_L17N_T2_32	AC19	HP
32	IO_L18P_T2_32	AB17	HP
32	IO_L18N_T2_32	AC17	HP
32	IO_L19P_T3_32	AE15	HP
32	IO_L19N_T3_VREF_32	AE14	HP
32	IO_L20P_T3_32	AA15	HP
32	IO_L20N_T3_32	AB15	HP
32	IO_L21P_T3_DQS_32	AC16	HP
32	IO_L21N_T3_DQS_32	AC15	HP
32	IO_L22P_T3_32	AC14	HP
32	IO_L22N_T3_32	AD14	HP
32	IO_L23P_T3_32	AA17	HP
32	IO_L23N_T3_32	AA16	HP
32	IO_L24P_T3_32	Y16	HP
32	IO_L24N_T3_32	Y15	HP
32	IO_25_VRP_32	AB14	HP

Bank	Pin name	Pin	I/O Type
33	IO_0_VRN_33	Y13	HP
33	IO_L1P_T0_33	AA12	HP
33	IO_L1N_T0_33	AB12	HP
33	IO_L2P_T0_33	AA8	HP
33	IO_L2N_T0_33	AB8	HP
33	IO_L3P_T0_DQS_33	AB9	HP
33	IO_L3N_T0_DQS_33	AC9	HP
33	IO_L4P_T0_33	Y11	HP
33	IO_L4N_T0_33	Y10	HP
33	IO_L5P_T0_33	AA11	HP
33	IO_L5N_T0_33	AA10	HP
33	IO_L6P_T0_33	AA13	HP
33	IO_L6N_T0_VREF_33	AB13	HP
33	IO_L7P_T1_33	AB10	HP
33	IO_L7N_T1_33	AC10	HP
33	IO_L8P_T1_33	AD8	HP
33	IO_L8N_T1_33	AE8	HP
33	IO_L9P_T1_DQS_33	AC12	HP
33	IO_L9N_T1_DQS_33	AC11	HP
33	IO_L10P_T1_33	AD9	HP
33	IO_L10N_T1_33	AE9	HP
33	IO_L11P_T1_SRCC_33	AE11	HP
33	IO_L11N_T1_SRCC_33	AF11	HP
33	IO_L12P_T1_MRCC_33	AD12	HP
33	IO_L12N_T1_MRCC_33	AD11	HP
33	IO_L13P_T2_MRCC_33	AG10	HP
33	IO_L13N_T2_MRCC_33	AH10	HP
33	IO_L14P_T2_SRCC_33	AE10	HP
33	IO_L14N_T2_SRCC_33	AF10	HP
33	IO_L15P_T2_DQS_33	AJ9	HP
33	IO_L15N_T2_DQS_33	AK9	HP
33	IO_L16P_T2_33	AG9	HP
33	IO_L16N_T2_33	AH9	HP
33	IO_L17P_T2_33	AK11	HP
33	IO_L17N_T2_33	AK10	HP
33	IO_L18P_T2_33	AH11	HP
33	IO_L18N_T2_33	AJ11	HP
33	IO_L19P_T3_33	AE13	HP
33	IO_L19N_T3_VREF_33	AF13	HP
33	IO_L20P_T3_33	AK14	HP

Bank	Pin name	Pin	I/O Type
33	IO_L20N_T3_33	AK13	HP
33	IO_L21P_T3_DQS_33	AH14	HP
33	IO_L21N_T3_DQS_33	AJ14	HP
33	IO_L22P_T3_33	AJ13	HP
33	IO_L22N_T3_33	AJ12	HP
33	IO_L23P_T3_33	AF12	HP
33	IO_L23N_T3_33	AG12	HP
33	IO_L24P_T3_33	AG13	HP
33	IO_L24N_T3_33	AH12	HP
33	IO_25_VRP_33	AD13	HP
34	IO_0_VRN_34	AC6	HP
34	IO_L1P_T0_34	AD4	HP
34	IO_L1N_T0_34	AD3	HP
34	IO_L2P_T0_34	AC2	HP
34	IO_L2N_T0_34	AC1	HP
34	IO_L3P_T0_DQS_34	AD2	HP
34	IO_L3N_T0_DQS_34	AD1	HP
34	IO_L4P_T0_34	AC5	HP
34	IO_L4N_T0_34	AC4	HP
34	IO_L5P_T0_34	AD6	HP
34	IO_L5N_T0_34	AE6	HP
34	IO_L6P_T0_34	AC7	HP
34	IO_L6N_T0_VREF_34	AD7	HP
34	IO_L7P_T1_34	AF3	HP
34	IO_L7N_T1_34	AF2	HP
34	IO_L8P_T1_34	AE1	HP
34	IO_L8N_T1_34	AF1	HP
34	IO_L9P_T1_DQS_34	AG4	HP
34	IO_L9N_T1_DQS_34	AG3	HP
34	IO_L10P_T1_34	AE4	HP
34	IO_L10N_T1_34	AE3	HP
34	IO_L11P_T1_SRCC_34	AE5	HP
34	IO_L11N_T1_SRCC_34	AF5	HP
34	IO_L12P_T1_MRCC_34	AF6	HP
34	IO_L12N_T1_MRCC_34	AG5	HP
34	IO_L13P_T2_MRCC_34	AH4	HP
34	IO_L13N_T2_MRCC_34	AJ4	HP
34	IO_L14P_T2_SRCC_34	AH6	HP
34	IO_L14N_T2_SRCC_34	AH5	HP
34	IO_L15P_T2_DQS_34	AG2	HP

Bank	Pin name	Pin	I/O Type
34	IO_L15N_T2_DQS_34	AH1	HP
34	IO_L16P_T2_34	AH2	HP
34	IO_L16N_T2_34	AJ2	HP
34	IO_L17P_T2_34	AJ1	HP
34	IO_L17N_T2_34	AK1	HP
34	IO_L18P_T2_34	AJ3	HP
34	IO_L18N_T2_34	AK3	HP
34	IO_L19P_T3_34	AF8	HP
34	IO_L19N_T3_VREF_34	AG8	HP
34	IO_L20P_T3_34	AF7	HP
34	IO_L20N_T3_34	AG7	HP
34	IO_L21P_T3_DQS_34	AH7	HP
34	IO_L21N_T3_DQS_34	AJ7	HP
34	IO_L22P_T3_34	AJ6	HP
34	IO_L22N_T3_34	AK6	HP
34	IO_L23P_T3_34	AJ8	HP
34	IO_L23N_T3_34	AK8	HP
34	IO_L24P_T3_34	AK5	HP
34	IO_L24N_T3_34	AK4	HP
34	IO_25_VRP_34	AB7	HP
115	MGTXTXP3_115	T2	GTX
115	MGTXRXP3_115	V6	GTX
115	MGTXTXN3_115	T1	GTX
115	MGTXRXN3_115	V5	GTX
115	MGTXTXP2_115	U4	GTX
115	MGTXRXP2_115	W4	GTX
115	MGTXTXN2_115	U3	GTX
115	MGTREFCLK0P_115	R8	GTX
115	MGTXRXN2_115	W3	GTX
115	MGTAVTTRCAL_115	W7	GTX
115	MGTREFCLK0N_115	R7	GTX
115	MGTRREF_115	W8	GTX
115	MGTREFCLK1N_115	U7	GTX
115	MGTREFCLK1P_115	U8	GTX
115	MGTXTXP1_115	V2	GTX
115	MGTXRXP1_115	Y6	GTX
115	MGTXTXN1_115	V1	GTX
115	MGTXRXN1_115	Y5	GTX
115	MGTXTXP0_115	Y2	GTX
115	MGTXRXP0_115	AA4	GTX

Bank	Pin name	Pin	I/O Type
115	MGTXTXN0_115	Y1	GTX
115	MGTXRXN0_115	AA3	GTX
116	MGTXTXP3_116	L4	GTX
116	MGTXRXP3_116	M6	GTX
116	MGTXTXN3_116	L3	GTX
116	MGTXRXN3_116	M5	GTX
116	MGTXTXP2_116	M2	GTX
116	MGTXRXP2_116	P6	GTX
116	MGTXTXN2_116	M1	GTX
116	MGTREFCLK0P_116	L8	GTX
116	MGTXRXN2_116	P5	GTX
116	MGTREFCLK0N_116	L7	GTX
116	MGTREFCLK1N_116	N7	GTX
116	MGTREFCLK1P_116	N8	GTX
116	MGTXTXP1_116	N4	GTX
116	MGTXRXP1_116	R4	GTX
116	MGTXTXN1_116	N3	GTX
116	MGTXRXN1_116	R3	GTX
116	MGTXTXP0_116	P2	GTX
116	MGTXRXP0_116	T6	GTX
116	MGTXTXN0_116	P1	GTX
116	MGTXRXN0_116	T5	GTX
117	MGTXTXP3_117	F2	GTX
117	MGTXRXP3_117	F6	GTX
117	MGTXTXN3_117	F1	GTX
117	MGTXRXN3_117	F5	GTX
117	MGTXTXP2_117	H2	GTX
117	MGTXRXP2_117	G4	GTX
117	MGTXTXN2_117	H1	GTX
117	MGTREFCLK0P_117	G8	GTX
117	MGTXRXN2_117	G3	GTX
117	MGTREFCLK0N_117	G7	GTX
117	MGTREFCLK1N_117	J7	GTX
117	MGTREFCLK1P_117	J8	GTX
117	MGTXTXP1_117	J4	GTX
117	MGTXRXP1_117	H6	GTX
117	MGTXTXN1_117	J3	GTX
117	MGTXRXN1_117	H5	GTX
117	MGTXTXP0_117	K2	GTX
117	MGTXRXP0_117	K6	GTX

Bank	Pin name	Pin	I/O Type
117	MGTXTXN0_117	K1	GTX
117	MGTXRXN0_117	K5	GTX
118	MGTXTXP3_118	A4	GTX
118	MGTXRXP3_118	A8	GTX
118	MGTXTXN3_118	A3	GTX
118	MGTXRXN3_118	A7	GTX
118	MGTXTXP2_118	B2	GTX
118	MGTXRXP2_118	B6	GTX
118	MGTXTXN2_118	B1	GTX
118	MGTREFCLK0P_118	C8	GTX
118	MGTXRXN2_118	B5	GTX
118	MGTREFCLK0N_118	C7	GTX
118	MGTREFCLK1N_118	E7	GTX
118	MGTREFCLK1P_118	E8	GTX
118	MGTXTXP1_118	C4	GTX
118	MGTXRXP1_118	D6	GTX
118	MGTXTXN1_118	C3	GTX
118	MGTXRXN1_118	D5	GTX
118	MGTXTXP0_118	D2	GTX
118	MGTXRXP0_118	E4	GTX
118	MGTXTXN0_118	D1	GTX
118	MGTXRXN0_118	E3	GTX
NA	MGTAVCC	B7	NA
NA	MGTAVCC	D7	NA
NA	MGTAVCC	F7	NA
NA	MGTAVCC	H7	NA
NA	MGTAVCC	K7	NA
NA	MGTAVCC	M7	NA
NA	MGTAVCC	P7	NA
NA	MGTVCCAUX	T7	NA
NA	MGTVCCAUX	V7	NA
NA	MGTAVTT	B3	NA
NA	MGTAVTT	C5	NA
NA	MGTAVTT	D3	NA
NA	MGTAVTT	E5	NA
NA	MGTAVTT	F3	NA
NA	MGTAVTT	G5	NA
NA	MGTAVTT	H3	NA
NA	MGTAVTT	J5	NA
NA	MGTAVTT	K3	NA

Bank	Pin name	Pin	I/O Type
NA	MGTAVTT	L5	NA
NA	MGTAVTT	M3	NA
NA	MGTAVTT	N5	NA
NA	MGTAVTT	P3	NA
NA	MGTAVTT	R5	NA
NA	MGTAVTT	T3	NA
NA	MGTAVTT	U5	NA
NA	MGTAVTT	V3	NA
NA	MGTAVTT	W5	NA
NA	VCCBRAM	N16	NA
NA	VCCBRAM	R16	NA
NA	VCCBRAM	U16	NA
NA	VCCBRAM	W16	NA
NA	GND	A1	NA
NA	GND	A14	NA
NA	GND	A2	NA
NA	GND	A24	NA
NA	GND	A5	NA
NA	GND	A6	NA
NA	GND	A9	NA
NA	GND	AA1	NA
NA	GND	AA14	NA
NA	GND	AA2	NA
NA	GND	AA24	NA
NA	GND	AA5	NA
NA	GND	AA6	NA
NA	GND	AA7	NA
NA	GND	AB11	NA
NA	GND	AB21	NA
NA	GND	AB3	NA
NA	GND	AB4	NA
NA	GND	AC18	NA
NA	GND	AC28	NA
NA	GND	AC8	NA
NA	GND	AD15	NA
NA	GND	AD25	NA
NA	GND	AD5	NA
NA	GND	AE12	NA
NA	GND	AE2	NA
NA	GND	AE22	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AF19	NA
NA	GND	AF29	NA
NA	GND	AF9	NA
NA	GND	AG16	NA
NA	GND	AG26	NA
NA	GND	AG6	NA
NA	GND	AH13	NA
NA	GND	AH23	NA
NA	GND	AH3	NA
NA	GND	AJ10	NA
NA	GND	AJ20	NA
NA	GND	AJ30	NA
NA	GND	AK17	NA
NA	GND	AK27	NA
NA	GND	AK7	NA
NA	GND	B11	NA
NA	GND	B21	NA
NA	GND	B4	NA
NA	GND	B8	NA
NA	GND	B9	NA
NA	GND	C1	NA
NA	GND	C18	NA
NA	GND	C2	NA
NA	GND	C28	NA
NA	GND	C6	NA
NA	GND	C9	NA
NA	GND	D15	NA
NA	GND	D25	NA
NA	GND	D4	NA
NA	GND	D8	NA
NA	GND	D9	NA
NA	GND	E1	NA
NA	GND	E12	NA
NA	GND	E2	NA
NA	GND	E22	NA
NA	GND	E6	NA
NA	GND	E9	NA
NA	GND	F19	NA
NA	GND	F29	NA
NA	GND	F4	NA

Bank	Pin name	Pin	I/O Type
NA	GND	F8	NA
NA	GND	F9	NA
NA	GND	G1	NA
NA	GND	G16	NA
NA	GND	G2	NA
NA	GND	G26	NA
NA	GND	G6	NA
NA	GND	G9	NA
NA	GND	H13	NA
NA	GND	H23	NA
NA	GND	H4	NA
NA	GND	H8	NA
NA	GND	H9	NA
NA	GND	J1	NA
NA	GND	J10	NA
NA	GND	J2	NA
NA	GND	J20	NA
NA	GND	J30	NA
NA	GND	J6	NA
NA	GND	J9	NA
NA	GND	K17	NA
NA	GND	K27	NA
NA	GND	K4	NA
NA	GND	K8	NA
NA	GND	K9	NA
NA	GND	L1	NA
NA	GND	L14	NA
NA	GND	L2	NA
NA	GND	L24	NA
NA	GND	L6	NA
NA	GND	L9	NA
NA	GND	M12	NA
NA	GND	M14	NA
NA	GND	M16	NA
NA	GND	M18	NA
NA	GND	M21	NA
NA	GND	M4	NA
NA	GND	M8	NA
NA	GND	M9	NA
NA	GND	N1	NA

Bank	Pin name	Pin	I/O Type
NA	GND	N11	NA
NA	GND	N13	NA
NA	GND	N15	NA
NA	GND	N17	NA
NA	GND	N2	NA
NA	GND	N28	NA
NA	GND	N6	NA
NA	GND	N9	NA
NA	GND	P10	NA
NA	GND	P12	NA
NA	GND	P16	NA
NA	GND	P18	NA
NA	GND	P25	NA
NA	GND	P4	NA
NA	GND	P8	NA
NA	GND	P9	NA
NA	GND	R1	NA
NA	GND	R11	NA
NA	GND	R13	NA
NA	GND	R17	NA
NA	GND	R2	NA
NA	GND	R22	NA
NA	GND	R6	NA
NA	GND	R9	NA
NA	GND	T10	NA
NA	GND	T12	NA
NA	GND	T16	NA
NA	GND	T18	NA
NA	GND	T19	NA
NA	GND	T29	NA
NA	GND	T4	NA
NA	GND	T8	NA
NA	GND	U1	NA
NA	GND	U11	NA
NA	GND	U13	NA
NA	GND	U17	NA
NA	GND	U2	NA
NA	GND	U26	NA
NA	GND	U6	NA
NA	GND	U9	NA

Bank	Pin name	Pin	I/O Type
NA	GND	V10	NA
NA	GND	V12	NA
NA	GND	V14	NA
NA	GND	V16	NA
NA	GND	V18	NA
NA	GND	V23	NA
NA	GND	V4	NA
NA	GND	V8	NA
NA	GND	V9	NA
NA	GND	W1	NA
NA	GND	W11	NA
NA	GND	W13	NA
NA	GND	W15	NA
NA	GND	W17	NA
NA	GND	W2	NA
NA	GND	W20	NA
NA	GND	W30	NA
NA	GND	W6	NA
NA	GND	W9	NA
NA	GND	Y17	NA
NA	GND	Y27	NA
NA	GND	Y3	NA
NA	GND	Y4	NA
NA	GND	Y7	NA
NA	GND	Y8	NA
NA	GND	Y9	NA
NA	VCCINT	M11	NA
NA	VCCINT	M13	NA
NA	VCCINT	M15	NA
NA	VCCINT	M17	NA
NA	VCCINT	N10	NA
NA	VCCINT	N12	NA
NA	VCCINT	N14	NA
NA	VCCINT	N18	NA
NA	VCCINT	P11	NA
NA	VCCINT	P17	NA
NA	VCCINT	R10	NA
NA	VCCINT	R12	NA
NA	VCCINT	R18	NA
NA	VCCINT	T11	NA

Bank	Pin name	Pin	I/O Type
NA	VCCINT	T17	NA
NA	VCCINT	U10	NA
NA	VCCINT	U12	NA
NA	VCCINT	U18	NA
NA	VCCINT	V17	NA
NA	VCCINT	W18	NA
NA	VCCAUX	P13	NA
NA	VCCAUX	T13	NA
NA	VCCAUX	V13	NA
NA	VCCAUX	V15	NA
NA	VCCAUX	W14	NA
NA	VCCAUX_IO_G0	W12	NA
NA	VCCAUX_IO_G0	V11	NA
NA	VCCAUX_IO_G0	W10	NA
32	VCCO_32	AA19	NA
32	VCCO_32	AB16	NA
32	VCCO_32	AE17	NA
32	VCCO_32	AF14	NA
32	VCCO_32	AH18	NA
32	VCCO_32	AJ15	NA
33	VCCO_33	AA9	NA
33	VCCO_33	AC13	NA
33	VCCO_33	AD10	NA
33	VCCO_33	AG11	NA
33	VCCO_33	AK12	NA
33	VCCO_33	Y12	NA
34	VCCO_34	AC3	NA
34	VCCO_34	AE7	NA
34	VCCO_34	AF4	NA
34	VCCO_34	AG1	NA
34	VCCO_34	AH8	NA
34	VCCO_34	AJ5	NA
34	VCCO_34	AK2	NA
12	VCCO_12	AC23	NA
12	VCCO_12	AD20	NA
12	VCCO_12	AF24	NA
12	VCCO_12	AG21	NA
12	VCCO_12	AK22	NA
12	VCCO_12	Y22	NA
13	VCCO_13	AA29	NA

Bank	Pin name	Pin	I/O Type
13	VCCO_13	AB26	NA
13	VCCO_13	AD30	NA
13	VCCO_13	AE27	NA
13	VCCO_13	AH28	NA
13	VCCO_13	AJ25	NA
14	VCCO_14	P30	NA
14	VCCO_14	R27	NA
14	VCCO_14	T24	NA
14	VCCO_14	U21	NA
14	VCCO_14	V28	NA
14	VCCO_14	W25	NA
15	VCCO_15	J25	NA
15	VCCO_15	K22	NA
15	VCCO_15	L29	NA
15	VCCO_15	M26	NA
15	VCCO_15	N23	NA
15	VCCO_15	P20	NA
16	VCCO_16	A29	NA
16	VCCO_16	B26	NA
16	VCCO_16	C23	NA
16	VCCO_16	D30	NA
16	VCCO_16	E27	NA
16	VCCO_16	F24	NA
16	VCCO_16	H28	NA
17	VCCO_17	A19	NA
17	VCCO_17	B16	NA
17	VCCO_17	D20	NA
17	VCCO_17	E17	NA
17	VCCO_17	G21	NA
17	VCCO_17	H18	NA
17	VCCO_17	L19	NA
18	VCCO_18	C13	NA
18	VCCO_18	D10	NA
18	VCCO_18	F14	NA
18	VCCO_18	G11	NA
18	VCCO_18	J15	NA
18	VCCO_18	K12	NA
0	VCCO_0	AB6	NA
0	VCCO_0	T9	NA

Table 2 BQ7K410TBG900-PBGA900 Pinout

Bank	Pin name	Pin	I/O Type
0	DXN_0	U14	CONFIG
0	VCCADC_0	P15	CONFIG
0	GNDADC_0	P14	CONFIG
0	DXP_0	U15	CONFIG
0	VREFN_0	R14	CONFIG
0	VREFP_0	T15	CONFIG
0	VP_0	R15	CONFIG
0	VN_0	T14	CONFIG
0	VCCBATT_0	C10	CONFIG
0	CCLK_0	B10	CONFIG
0	TCK_0	E10	CONFIG
0	TMS_0	F10	CONFIG
0	TDO_0	G10	CONFIG
0	TDI_0	H10	CONFIG
0	INIT_B_0	A10	CONFIG
0	PROGRAM_B_0	K10	CONFIG
0	CFGBVS_0	L10	CONFIG
0	DONE_0	M10	CONFIG
0	M2_0	AB1	CONFIG
0	M0_0	AB5	CONFIG
0	M1_0	AB2	CONFIG
12	IO_0_12	Y20	HR
12	IO_L1P_T0_12	Y23	HR
12	IO_L1N_T0_12	Y24	HR
12	IO_L2P_T0_12	Y21	HR
12	IO_L2N_T0_12	AA21	HR
12	IO_L3P_T0_DQS_12	AB22	HR
12	IO_L3N_T0_DQS_12	AB23	HR
12	IO_L4P_T0_12	AA22	HR
12	IO_L4N_T0_12	AA23	HR
12	IO_L5P_T0_12	AC20	HR
12	IO_L5N_T0_12	AC21	HR
12	IO_L6P_T0_12	AA20	HR
12	IO_L6N_T0_VREF_12	AB20	HR
12	IO_L7P_T1_12	AB24	HR
12	IO_L7N_T1_12	AC25	HR
12	IO_L8P_T1_12	AC22	HR
12	IO_L8N_T1_12	AD22	HR
12	IO_L9P_T1_DQS_12	AC24	HR

Bank	Pin name	Pin	I/O Type
12	IO_L9N_T1_DQS_12	AD24	HR
12	IO_L10P_T1_12	AD21	HR
12	IO_L10N_T1_12	AE21	HR
12	IO_L11P_T1_SRCC_12	AE23	HR
12	IO_L11N_T1_SRCC_12	AF23	HR
12	IO_L12P_T1_MRCC_12	AD23	HR
12	IO_L12N_T1_MRCC_12	AE24	HR
12	IO_L13P_T2_MRCC_12	AF22	HR
12	IO_L13N_T2_MRCC_12	AG23	HR
12	IO_L14P_T2_SRCC_12	AG24	HR
12	IO_L14N_T2_SRCC_12	AH24	HR
12	IO_L15P_T2_DQS_12	AJ24	HR
12	IO_L15N_T2_DQS_12	AK25	HR
12	IO_L16P_T2_12	AE25	HR
12	IO_L16N_T2_12	AF25	HR
12	IO_L17P_T2_12	AK23	HR
12	IO_L17N_T2_12	AK24	HR
12	IO_L18P_T2_12	AG25	HR
12	IO_L18N_T2_12	AH25	HR
12	IO_L19P_T3_12	AF20	HR
12	IO_L19N_T3_VREF_12	AF21	HR
12	IO_L20P_T3_12	AG22	HR
12	IO_L20N_T3_12	AH22	HR
12	IO_L21P_T3_DQS_12	AJ22	HR
12	IO_L21N_T3_DQS_12	AJ23	HR
12	IO_L22P_T3_12	AG20	HR
12	IO_L22N_T3_12	AH20	HR
12	IO_L23P_T3_12	AH21	HR
12	IO_L23N_T3_12	AJ21	HR
12	IO_L24P_T3_12	AK20	HR
12	IO_L24N_T3_12	AK21	HR
12	IO_25_12	AE20	HR
13	IO_0_13	Y25	HR
13	IO_L1P_T0_13	Y26	HR
13	IO_L1N_T0_13	AA26	HR
13	IO_L2P_T0_13	W27	HR
13	IO_L2N_T0_13	W28	HR
13	IO_L3P_T0_DQS_13	Y28	HR
13	IO_L3N_T0_DQS_13	AA28	HR
13	IO_L4P_T0_13	W29	HR

Bank	Pin name	Pin	I/O Type
13	IO_L4N_T0_13	Y29	HR
13	IO_L5P_T0_13	AA27	HR
13	IO_L5N_T0_13	AB28	HR
13	IO_L6P_T0_13	AA25	HR
13	IO_L6N_T0_VREF_13	AB25	HR
13	IO_L7P_T1_13	AC29	HR
13	IO_L7N_T1_13	AC30	HR
13	IO_L8P_T1_13	Y30	HR
13	IO_L8N_T1_13	AA30	HR
13	IO_L9P_T1_DQS_13	AD29	HR
13	IO_L9N_T1_DQS_13	AE29	HR
13	IO_L10P_T1_13	AB29	HR
13	IO_L10N_T1_13	AB30	HR
13	IO_L11P_T1_SRCC_13	AD27	HR
13	IO_L11N_T1_SRCC_13	AD28	HR
13	IO_L12P_T1_MRCC_13	AB27	HR
13	IO_L12N_T1_MRCC_13	AC27	HR
13	IO_L13P_T2_MRCC_13	AG29	HR
13	IO_L13N_T2_MRCC_13	AH29	HR
13	IO_L14P_T2_SRCC_13	AE28	HR
13	IO_L14N_T2_SRCC_13	AF28	HR
13	IO_L15P_T2_DQS_13	AK29	HR
13	IO_L15N_T2_DQS_13	AK30	HR
13	IO_L16P_T2_13	AE30	HR
13	IO_L16N_T2_13	AF30	HR
13	IO_L17P_T2_13	AJ28	HR
13	IO_L17N_T2_13	AJ29	HR
13	IO_L18P_T2_13	AG30	HR
13	IO_L18N_T2_13	AH30	HR
13	IO_L19P_T3_13	AC26	HR
13	IO_L19N_T3_VREF_13	AD26	HR
13	IO_L20P_T3_13	AJ27	HR
13	IO_L20N_T3_13	AK28	HR
13	IO_L21P_T3_DQS_13	AG27	HR
13	IO_L21N_T3_DQS_13	AG28	HR
13	IO_L22P_T3_13	AH26	HR
13	IO_L22N_T3_13	AH27	HR
13	IO_L23P_T3_13	AF26	HR
13	IO_L23N_T3_13	AF27	HR
13	IO_L24P_T3_13	AJ26	HR

Bank	Pin name	Pin	I/O Type
13	IO_L24N_T3_13	AK26	HR
13	IO_25_13	AE26	HR
14	IO_0_14	R19	HR
14	IO_L1P_T0_D00_MOSI_14	P24	HR
14	IO_L1N_T0_D01_DIN_14	R25	HR
14	IO_L2P_T0_D02_14	R20	HR
14	IO_L2N_T0_D03_14	R21	HR
14	IO_L3P_T0_DQS_PUDC_B_14	R23	HR
14	IO_L3N_T0_DQS_EMCCLK_14	R24	HR
14	IO_L4P_T0_D04_14	T20	HR
14	IO_L4N_T0_D05_14	T21	HR
14	IO_L5P_T0_D06_14	T22	HR
14	IO_L5N_T0_D07_14	T23	HR
14	IO_L6P_T0_FCS_B_14	U19	HR
14	IO_L6N_T0_D08_VREF_14	U20	HR
14	IO_L7P_T1_D09_14	P29	HR
14	IO_L7N_T1_D10_14	R29	HR
14	IO_L8P_T1_D11_14	P27	HR
14	IO_L8N_T1_D12_14	P28	HR
14	IO_L9P_T1_DQS_14	R30	HR
14	IO_L9N_T1_DQS_D13_14	T30	HR
14	IO_L10P_T1_D14_14	P26	HR
14	IO_L10N_T1_D15_14	R26	HR
14	IO_L11P_T1_SRCC_14	R28	HR
14	IO_L11N_T1_SRCC_14	T28	HR
14	IO_L12P_T1_MRCC_14	T26	HR
14	IO_L12N_T1_MRCC_14	T27	HR
14	IO_L13P_T2_MRCC_14	U27	HR
14	IO_L13N_T2_MRCC_14	U28	HR
14	IO_L14P_T2_SRCC_14	T25	HR
14	IO_L14N_T2_SRCC_14	U25	HR
14	IO_L15P_T2_DQS_RDWR_B_14	U29	HR
14	IO_L15N_T2_DQS_DOUT_CSO_B_14	U30	HR
14	IO_L16P_T2_CSI_B_14	V26	HR
14	IO_L16N_T2_A15_D31_14	V27	HR
14	IO_L17P_T2_A14_D30_14	V29	HR
14	IO_L17N_T2_A13_D29_14	V30	HR
14	IO_L18P_T2_A12_D28_14	V25	HR
14	IO_L18N_T2_A11_D27_14	W26	HR
14	IO_L19P_T3_A10_D26_14	V19	HR

Bank	Pin name	Pin	I/O Type
14	IO_L19N_T3_A09_D25_VREF_14	V20	HR
14	IO_L20P_T3_A08_D24_14	W23	HR
14	IO_L20N_T3_A07_D23_14	W24	HR
14	IO_L21P_T3_DQS_14	U22	HR
14	IO_L21N_T3_DQS_A06_D22_14	U23	HR
14	IO_L22P_T3_A05_D21_14	V21	HR
14	IO_L22N_T3_A04_D20_14	V22	HR
14	IO_L23P_T3_A03_D19_14	U24	HR
14	IO_L23N_T3_A02_D18_14	V24	HR
14	IO_L24P_T3_A01_D17_14	W21	HR
14	IO_L24N_T3_A00_D16_14	W22	HR
14	IO_25_14	W19	HR
15	IO_0_15	M19	HR
15	IO_L1P_T0_AD0P_15	J23	HR
15	IO_L1N_T0_AD0N_15	J24	HR
15	IO_L2P_T0_AD8P_15	L22	HR
15	IO_L2N_T0_AD8N_15	L23	HR
15	IO_L3P_T0_DQS_AD1P_15	K23	HR
15	IO_L3N_T0_DQS_AD1N_15	K24	HR
15	IO_L4P_T0_AD9P_15	L21	HR
15	IO_L4N_T0_AD9N_15	K21	HR
15	IO_L5P_T0_AD2P_15	J21	HR
15	IO_L5N_T0_AD2N_15	J22	HR
15	IO_L6P_T0_15	M20	HR
15	IO_L6N_T0_VREF_15	L20	HR
15	IO_L7P_T1_AD10P_15	J29	HR
15	IO_L7N_T1_AD10N_15	H29	HR
15	IO_L8P_T1_AD3P_15	J27	HR
15	IO_L8N_T1_AD3N_15	J28	HR
15	IO_L9P_T1_DQS_AD11P_15	L30	HR
15	IO_L9N_T1_DQS_AD11N_15	K30	HR
15	IO_L10P_T1_AD4P_15	K26	HR
15	IO_L10N_T1_AD4N_15	J26	HR
15	IO_L11P_T1_SRCC_AD12P_15	L26	HR
15	IO_L11N_T1_SRCC_AD12N_15	L27	HR
15	IO_L12P_T1_MRCC_AD5P_15	L25	HR
15	IO_L12N_T1_MRCC_AD5N_15	K25	HR
15	IO_L13P_T2_MRCC_15	K28	HR
15	IO_L13N_T2_MRCC_15	K29	HR
15	IO_L14P_T2_SRCC_15	M28	HR

Bank	Pin name	Pin	I/O Type
15	IO_L14N_T2_SRCC_15	L28	HR
15	IO_L15P_T2_DQS_15	M29	HR
15	IO_L15N_T2_DQS_ADV_B_15	M30	HR
15	IO_L16P_T2_A28_15	N27	HR
15	IO_L16N_T2_A27_15	M27	HR
15	IO_L17P_T2_A26_15	N29	HR
15	IO_L17N_T2_A25_15	N30	HR
15	IO_L18P_T2_A24_15	N25	HR
15	IO_L18N_T2_A23_15	N26	HR
15	IO_L19P_T3_A22_15	N19	HR
15	IO_L19N_T3_A21_VREF_15	N20	HR
15	IO_L20P_T3_A20_15	N21	HR
15	IO_L20N_T3_A19_15	N22	HR
15	IO_L21P_T3_DQS_15	P23	HR
15	IO_L21N_T3_DQS_A18_15	N24	HR
15	IO_L22P_T3_A17_15	P21	HR
15	IO_L22N_T3_A16_15	P22	HR
15	IO_L23P_T3_FOE_B_15	M24	HR
15	IO_L23N_T3_FWE_B_15	M25	HR
15	IO_L24P_T3_RS1_15	M22	HR
15	IO_L24N_T3_RS0_15	M23	HR
15	IO_25_15	P19	HR
16	IO_0_16	F23	HR
16	IO_L1P_T0_16	B23	HR
16	IO_L1N_T0_16	A23	HR
16	IO_L2P_T0_16	E23	HR
16	IO_L2N_T0_16	D23	HR
16	IO_L3P_T0_DQS_16	F25	HR
16	IO_L3N_T0_DQS_16	E25	HR
16	IO_L4P_T0_16	E24	HR
16	IO_L4N_T0_16	D24	HR
16	IO_L5P_T0_16	F26	HR
16	IO_L5N_T0_16	E26	HR
16	IO_L6P_T0_16	G23	HR
16	IO_L6N_T0_VREF_16	G24	HR
16	IO_L7P_T1_16	B27	HR
16	IO_L7N_T1_16	A27	HR
16	IO_L8P_T1_16	C24	HR
16	IO_L8N_T1_16	B24	HR
16	IO_L9P_T1_DQS_16	B28	HR

Bank	Pin name	Pin	I/O Type
16	IO_L9N_T1_DQS_16	A28	HR
16	IO_L10P_T1_16	A25	HR
16	IO_L10N_T1_16	A26	HR
16	IO_L11P_T1_SRCC_16	D26	HR
16	IO_L11N_T1_SRCC_16	C26	HR
16	IO_L12P_T1_MRCC_16	C25	HR
16	IO_L12N_T1_MRCC_16	B25	HR
16	IO_L13P_T2_MRCC_16	D27	HR
16	IO_L13N_T2_MRCC_16	C27	HR
16	IO_L14P_T2_SRCC_16	E28	HR
16	IO_L14N_T2_SRCC_16	D28	HR
16	IO_L15P_T2_DQS_16	C29	HR
16	IO_L15N_T2_DQS_16	B29	HR
16	IO_L16P_T2_16	D29	HR
16	IO_L16N_T2_16	C30	HR
16	IO_L17P_T2_16	B30	HR
16	IO_L17N_T2_16	A30	HR
16	IO_L18P_T2_16	E29	HR
16	IO_L18N_T2_16	E30	HR
16	IO_L19P_T3_16	H24	HR
16	IO_L19N_T3_VREF_16	H25	HR
16	IO_L20P_T3_16	G28	HR
16	IO_L20N_T3_16	F28	HR
16	IO_L21P_T3_DQS_16	G27	HR
16	IO_L21N_T3_DQS_16	F27	HR
16	IO_L22P_T3_16	G29	HR
16	IO_L22N_T3_16	F30	HR
16	IO_L23P_T3_16	H26	HR
16	IO_L23N_T3_16	H27	HR
16	IO_L24P_T3_16	H30	HR
16	IO_L24N_T3_16	G30	HR
16	IO_25_16	G25	HR
17	IO_0_17	G19	HR
17	IO_L1P_T0_17	K18	HR
17	IO_L1N_T0_17	J18	HR
17	IO_L2P_T0_17	H20	HR
17	IO_L2N_T0_17	G20	HR
17	IO_L3P_T0_DQS_17	J17	HR
17	IO_L3N_T0_DQS_17	H17	HR
17	IO_L4P_T0_17	J19	HR

Bank	Pin name	Pin	I/O Type
17	IO_L4N_T0_17	H19	HR
17	IO_L5P_T0_17	L17	HR
17	IO_L5N_T0_17	L18	HR
17	IO_L6P_T0_17	K19	HR
17	IO_L6N_T0_VREF_17	K20	HR
17	IO_L7P_T1_17	H21	HR
17	IO_L7N_T1_17	H22	HR
17	IO_L8P_T1_17	D21	HR
17	IO_L8N_T1_17	C21	HR
17	IO_L9P_T1_DQS_17	G22	HR
17	IO_L9N_T1_DQS_17	F22	HR
17	IO_L10P_T1_17	D22	HR
17	IO_L10N_T1_17	C22	HR
17	IO_L11P_T1_SRCC_17	F21	HR
17	IO_L11N_T1_SRCC_17	E21	HR
17	IO_L12P_T1_MRCC_17	F20	HR
17	IO_L12N_T1_MRCC_17	E20	HR
17	IO_L13P_T2_MRCC_17	D17	HR
17	IO_L13N_T2_MRCC_17	D18	HR
17	IO_L14P_T2_SRCC_17	E19	HR
17	IO_L14N_T2_SRCC_17	D19	HR
17	IO_L15P_T2_DQS_17	D16	HR
17	IO_L15N_T2_DQS_17	C16	HR
17	IO_L16P_T2_17	G18	HR
17	IO_L16N_T2_17	F18	HR
17	IO_L17P_T2_17	C17	HR
17	IO_L17N_T2_17	B17	HR
17	IO_L18P_T2_17	G17	HR
17	IO_L18N_T2_17	F17	HR
17	IO_L19P_T3_17	C20	HR
17	IO_L19N_T3_VREF_17	B20	HR
17	IO_L20P_T3_17	A16	HR
17	IO_L20N_T3_17	A17	HR
17	IO_L21P_T3_DQS_17	A20	HR
17	IO_L21N_T3_DQS_17	A21	HR
17	IO_L22P_T3_17	B18	HR
17	IO_L22N_T3_17	A18	HR
17	IO_L23P_T3_17	B22	HR
17	IO_L23N_T3_17	A22	HR
17	IO_L24P_T3_17	C19	HR

Bank	Pin name	Pin	I/O Type
17	IO_L24N_T3_17	B19	HR
17	IO_25_17	E18	HR
18	IO_0_18	G12	HR
18	IO_L1P_T0_18	L16	HR
18	IO_L1N_T0_18	K16	HR
18	IO_L2P_T0_18	L15	HR
18	IO_L2N_T0_18	K15	HR
18	IO_L3P_T0_DQS_18	L12	HR
18	IO_L3N_T0_DQS_18	L13	HR
18	IO_L4P_T0_18	K13	HR
18	IO_L4N_T0_18	J13	HR
18	IO_L5P_T0_18	K14	HR
18	IO_L5N_T0_18	J14	HR
18	IO_L6P_T0_18	L11	HR
18	IO_L6N_T0_VREF_18	K11	HR
18	IO_L7P_T1_18	H15	HR
18	IO_L7N_T1_18	G15	HR
18	IO_L8P_T1_18	J11	HR
18	IO_L8N_T1_18	J12	HR
18	IO_L9P_T1_DQS_18	J16	HR
18	IO_L9N_T1_DQS_18	H16	HR
18	IO_L10P_T1_18	H11	HR
18	IO_L10N_T1_18	H12	HR
18	IO_L11P_T1_SRCC_18	H14	HR
18	IO_L11N_T1_SRCC_18	G14	HR
18	IO_L12P_T1_MRCC_18	G13	HR
18	IO_L12N_T1_MRCC_18	F13	HR
18	IO_L13P_T2_MRCC_18	D12	HR
18	IO_L13N_T2_MRCC_18	D13	HR
18	IO_L14P_T2_SRCC_18	F12	HR
18	IO_L14N_T2_SRCC_18	E13	HR
18	IO_L15P_T2_DQS_18	C12	HR
18	IO_L15N_T2_DQS_18	B12	HR
18	IO_L16P_T2_18	F11	HR
18	IO_L16N_T2_18	E11	HR
18	IO_L17P_T2_18	A11	HR
18	IO_L17N_T2_18	A12	HR
18	IO_L18P_T2_18	D11	HR
18	IO_L18N_T2_18	C11	HR
18	IO_L19P_T3_18	F15	HR

Bank	Pin name	Pin	I/O Type
18	IO_L19N_T3_VREF_18	E16	HR
18	IO_L20P_T3_18	E14	HR
18	IO_L20N_T3_18	E15	HR
18	IO_L21P_T3_DQS_18	D14	HR
18	IO_L21N_T3_DQS_18	C14	HR
18	IO_L22P_T3_18	B13	HR
18	IO_L22N_T3_18	A13	HR
18	IO_L23P_T3_18	C15	HR
18	IO_L23N_T3_18	B15	HR
18	IO_L24P_T3_18	B14	HR
18	IO_L24N_T3_18	A15	HR
18	IO_25_18	F16	HR
32	IO_0_VRN_32	Y14	HP
32	IO_L1P_T0_32	AK16	HP
32	IO_L1N_T0_32	AK15	HP
32	IO_L2P_T0_32	AG15	HP
32	IO_L2N_T0_32	AH15	HP
32	IO_L3P_T0_DQS_32	AH16	HP
32	IO_L3N_T0_DQS_32	AJ16	HP
32	IO_L4P_T0_32	AF15	HP
32	IO_L4N_T0_32	AG14	HP
32	IO_L5P_T0_32	AH17	HP
32	IO_L5N_T0_32	AJ17	HP
32	IO_L6P_T0_32	AE16	HP
32	IO_L6N_T0_VREF_32	AF16	HP
32	IO_L7P_T1_32	AJ19	HP
32	IO_L7N_T1_32	AK19	HP
32	IO_L8P_T1_32	AG19	HP
32	IO_L8N_T1_32	AH19	HP
32	IO_L9P_T1_DQS_32	AJ18	HP
32	IO_L9N_T1_DQS_32	AK18	HP
32	IO_L10P_T1_32	AD19	HP
32	IO_L10N_T1_32	AE19	HP
32	IO_L11P_T1_SRCC_32	AF18	HP
32	IO_L11N_T1_SRCC_32	AG18	HP
32	IO_L12P_T1_MRCC_32	AF17	HP
32	IO_L12N_T1_MRCC_32	AG17	HP
32	IO_L13P_T2_MRCC_32	AD18	HP
32	IO_L13N_T2_MRCC_32	AE18	HP
32	IO_L14P_T2_SRCC_32	AD17	HP

Bank	Pin name	Pin	I/O Type
32	IO_L14N_T2_SRCC_32	AD16	HP
32	IO_L15P_T2_DQS_32	Y19	HP
32	IO_L15N_T2_DQS_32	Y18	HP
32	IO_L16P_T2_32	AA18	HP
32	IO_L16N_T2_32	AB18	HP
32	IO_L17P_T2_32	AB19	HP
32	IO_L17N_T2_32	AC19	HP
32	IO_L18P_T2_32	AB17	HP
32	IO_L18N_T2_32	AC17	HP
32	IO_L19P_T3_32	AE15	HP
32	IO_L19N_T3_VREF_32	AE14	HP
32	IO_L20P_T3_32	AA15	HP
32	IO_L20N_T3_32	AB15	HP
32	IO_L21P_T3_DQS_32	AC16	HP
32	IO_L21N_T3_DQS_32	AC15	HP
32	IO_L22P_T3_32	AC14	HP
32	IO_L22N_T3_32	AD14	HP
32	IO_L23P_T3_32	AA17	HP
32	IO_L23N_T3_32	AA16	HP
32	IO_L24P_T3_32	Y16	HP
32	IO_L24N_T3_32	Y15	HP
32	IO_25_VRP_32	AB14	HP
33	IO_0_VRN_33	Y13	HP
33	IO_L1P_T0_33	AA12	HP
33	IO_L1N_T0_33	AB12	HP
33	IO_L2P_T0_33	AA8	HP
33	IO_L2N_T0_33	AB8	HP
33	IO_L3P_T0_DQS_33	AB9	HP
33	IO_L3N_T0_DQS_33	AC9	HP
33	IO_L4P_T0_33	Y11	HP
33	IO_L4N_T0_33	Y10	HP
33	IO_L5P_T0_33	AA11	HP
33	IO_L5N_T0_33	AA10	HP
33	IO_L6P_T0_33	AA13	HP
33	IO_L6N_T0_VREF_33	AB13	HP
33	IO_L7P_T1_33	AB10	HP
33	IO_L7N_T1_33	AC10	HP
33	IO_L8P_T1_33	AD8	HP
33	IO_L8N_T1_33	AE8	HP
33	IO_L9P_T1_DQS_33	AC12	HP

Bank	Pin name	Pin	I/O Type
33	IO_L9N_T1_DQS_33	AC11	HP
33	IO_L10P_T1_33	AD9	HP
33	IO_L10N_T1_33	AE9	HP
33	IO_L11P_T1_SRCC_33	AE11	HP
33	IO_L11N_T1_SRCC_33	AF11	HP
33	IO_L12P_T1_MRCC_33	AD12	HP
33	IO_L12N_T1_MRCC_33	AD11	HP
33	IO_L13P_T2_MRCC_33	AG10	HP
33	IO_L13N_T2_MRCC_33	AH10	HP
33	IO_L14P_T2_SRCC_33	AE10	HP
33	IO_L14N_T2_SRCC_33	AF10	HP
33	IO_L15P_T2_DQS_33	AJ9	HP
33	IO_L15N_T2_DQS_33	AK9	HP
33	IO_L16P_T2_33	AG9	HP
33	IO_L16N_T2_33	AH9	HP
33	IO_L17P_T2_33	AK11	HP
33	IO_L17N_T2_33	AK10	HP
33	IO_L18P_T2_33	AH11	HP
33	IO_L18N_T2_33	AJ11	HP
33	IO_L19P_T3_33	AE13	HP
33	IO_L19N_T3_VREF_33	AF13	HP
33	IO_L20P_T3_33	AK14	HP
33	IO_L20N_T3_33	AK13	HP
33	IO_L21P_T3_DQS_33	AH14	HP
33	IO_L21N_T3_DQS_33	AJ14	HP
33	IO_L22P_T3_33	AJ13	HP
33	IO_L22N_T3_33	AJ12	HP
33	IO_L23P_T3_33	AF12	HP
33	IO_L23N_T3_33	AG12	HP
33	IO_L24P_T3_33	AG13	HP
33	IO_L24N_T3_33	AH12	HP
33	IO_25_VRP_33	AD13	HP
34	IO_0_VRN_34	AC6	HP
34	IO_L1P_T0_34	AD4	HP
34	IO_L1N_T0_34	AD3	HP
34	IO_L2P_T0_34	AC2	HP
34	IO_L2N_T0_34	AC1	HP
34	IO_L3P_T0_DQS_34	AD2	HP
34	IO_L3N_T0_DQS_34	AD1	HP
34	IO_L4P_T0_34	AC5	HP

Bank	Pin name	Pin	I/O Type
34	IO_L4N_T0_34	AC4	HP
34	IO_L5P_T0_34	AD6	HP
34	IO_L5N_T0_34	AE6	HP
34	IO_L6P_T0_34	AC7	HP
34	IO_L6N_T0_VREF_34	AD7	HP
34	IO_L7P_T1_34	AF3	HP
34	IO_L7N_T1_34	AF2	HP
34	IO_L8P_T1_34	AE1	HP
34	IO_L8N_T1_34	AF1	HP
34	IO_L9P_T1_DQS_34	AG4	HP
34	IO_L9N_T1_DQS_34	AG3	HP
34	IO_L10P_T1_34	AE4	HP
34	IO_L10N_T1_34	AE3	HP
34	IO_L11P_T1_SRCC_34	AE5	HP
34	IO_L11N_T1_SRCC_34	AF5	HP
34	IO_L12P_T1_MRCC_34	AF6	HP
34	IO_L12N_T1_MRCC_34	AG5	HP
34	IO_L13P_T2_MRCC_34	AH4	HP
34	IO_L13N_T2_MRCC_34	AJ4	HP
34	IO_L14P_T2_SRCC_34	AH6	HP
34	IO_L14N_T2_SRCC_34	AH5	HP
34	IO_L15P_T2_DQS_34	AG2	HP
34	IO_L15N_T2_DQS_34	AH1	HP
34	IO_L16P_T2_34	AH2	HP
34	IO_L16N_T2_34	AJ2	HP
34	IO_L17P_T2_34	AJ1	HP
34	IO_L17N_T2_34	AK1	HP
34	IO_L18P_T2_34	AJ3	HP
34	IO_L18N_T2_34	AK3	HP
34	IO_L19P_T3_34	AF8	HP
34	IO_L19N_T3_VREF_34	AG8	HP
34	IO_L20P_T3_34	AF7	HP
34	IO_L20N_T3_34	AG7	HP
34	IO_L21P_T3_DQS_34	AH7	HP
34	IO_L21N_T3_DQS_34	AJ7	HP
34	IO_L22P_T3_34	AJ6	HP
34	IO_L22N_T3_34	AK6	HP
34	IO_L23P_T3_34	AJ8	HP
34	IO_L23N_T3_34	AK8	HP
34	IO_L24P_T3_34	AK5	HP

Bank	Pin name	Pin	I/O Type
34	IO_L24N_T3_34	AK4	HP
34	IO_25_VRP_34	AB7	HP
115	MGTXTXP3_115	T2	GTX
115	MGTXRXP3_115	V6	GTX
115	MGTXTXN3_115	T1	GTX
115	MGTXRXN3_115	V5	GTX
115	MGTXTXP2_115	U4	GTX
115	MGTXRXP2_115	W4	GTX
115	MGTXTXN2_115	U3	GTX
115	MGTREFCLK0P_115	R8	GTX
115	MGTXRXN2_115	W3	GTX
115	MGTAVTTRCAL_115	W7	GTX
115	MGTREFCLK0N_115	R7	GTX
115	MGTRREF_115	W8	GTX
115	MGTREFCLK1N_115	U7	GTX
115	MGTREFCLK1P_115	U8	GTX
115	MGTXTXP1_115	V2	GTX
115	MGTXRXP1_115	Y6	GTX
115	MGTXTXN1_115	V1	GTX
115	MGTXRXN1_115	Y5	GTX
115	MGTXTXP0_115	Y2	GTX
115	MGTXRXP0_115	AA4	GTX
115	MGTXTXN0_115	Y1	GTX
115	MGTXRXN0_115	AA3	GTX
116	MGTXTXP3_116	L4	GTX
116	MGTXRXP3_116	M6	GTX
116	MGTXTXN3_116	L3	GTX
116	MGTXRXN3_116	M5	GTX
116	MGTXTXP2_116	M2	GTX
116	MGTXRXP2_116	P6	GTX
116	MGTXTXN2_116	M1	GTX
116	MGTREFCLK0P_116	L8	GTX
116	MGTXRXN2_116	P5	GTX
116	MGTREFCLK0N_116	L7	GTX
116	MGTREFCLK1N_116	N7	GTX
116	MGTREFCLK1P_116	N8	GTX
116	MGTXTXP1_116	N4	GTX
116	MGTXRXP1_116	R4	GTX
116	MGTXTXN1_116	N3	GTX
116	MGTXRXN1_116	R3	GTX

Bank	Pin name	Pin	I/O Type
116	MGTXTXP0_116	P2	GTX
116	MGTXRXP0_116	T6	GTX
116	MGTXTXN0_116	P1	GTX
116	MGTXRXN0_116	T5	GTX
117	MGTXTXP3_117	F2	GTX
117	MGTXRXP3_117	F6	GTX
117	MGTXTXN3_117	F1	GTX
117	MGTXRXN3_117	F5	GTX
117	MGTXTXP2_117	H2	GTX
117	MGTXRXP2_117	G4	GTX
117	MGTXTXN2_117	H1	GTX
117	MGTREFCLK0P_117	G8	GTX
117	MGTXRXN2_117	G3	GTX
117	MGTREFCLK0N_117	G7	GTX
117	MGTREFCLK1N_117	J7	GTX
117	MGTREFCLK1P_117	J8	GTX
117	MGTXTXP1_117	J4	GTX
117	MGTXRXP1_117	H6	GTX
117	MGTXTXN1_117	J3	GTX
117	MGTXRXN1_117	H5	GTX
117	MGTXTXP0_117	K2	GTX
117	MGTXRXP0_117	K6	GTX
117	MGTXTXN0_117	K1	GTX
117	MGTXRXN0_117	K5	GTX
118	MGTXTXP3_118	A4	GTX
118	MGTXRXP3_118	A8	GTX
118	MGTXTXN3_118	A3	GTX
118	MGTXRXN3_118	A7	GTX
118	MGTXTXP2_118	B2	GTX
118	MGTXRXP2_118	B6	GTX
118	MGTXTXN2_118	B1	GTX
118	MGTREFCLK0P_118	C8	GTX
118	MGTXRXN2_118	B5	GTX
118	MGTREFCLK0N_118	C7	GTX
118	MGTREFCLK1N_118	E7	GTX
118	MGTREFCLK1P_118	E8	GTX
118	MGTXTXP1_118	C4	GTX
118	MGTXRXP1_118	D6	GTX
118	MGTXTXN1_118	C3	GTX
118	MGTXRXN1_118	D5	GTX

Bank	Pin name	Pin	I/O Type
118	MGTXTXP0_118	D2	GTX
118	MGTXRXP0_118	E4	GTX
118	MGTXTXN0_118	D1	GTX
118	MGTXRXN0_118	E3	GTX
NA	MGTAVCC	B7	NA
NA	MGTAVCC	D7	NA
NA	MGTAVCC	F7	NA
NA	MGTAVCC	H7	NA
NA	MGTAVCC	K7	NA
NA	MGTAVCC	M7	NA
NA	MGTAVCC	P7	NA
NA	MGTVCCAUX	T7	NA
NA	MGTVCCAUX	V7	NA
NA	MGTAVTT	B3	NA
NA	MGTAVTT	C5	NA
NA	MGTAVTT	D3	NA
NA	MGTAVTT	E5	NA
NA	MGTAVTT	F3	NA
NA	MGTAVTT	G5	NA
NA	MGTAVTT	H3	NA
NA	MGTAVTT	J5	NA
NA	MGTAVTT	K3	NA
NA	MGTAVTT	L5	NA
NA	MGTAVTT	M3	NA
NA	MGTAVTT	N5	NA
NA	MGTAVTT	P3	NA
NA	MGTAVTT	R5	NA
NA	MGTAVTT	T3	NA
NA	MGTAVTT	U5	NA
NA	MGTAVTT	V3	NA
NA	MGTAVTT	W5	NA
NA	VCCBRAM	N16	NA
NA	VCCBRAM	R16	NA
NA	VCCBRAM	U16	NA
NA	VCCBRAM	W16	NA
NA	GND	A1	NA
NA	GND	A14	NA
NA	GND	A2	NA
NA	GND	A24	NA
NA	GND	A5	NA

Bank	Pin name	Pin	I/O Type
NA	GND	A6	NA
NA	GND	A9	NA
NA	GND	AA1	NA
NA	GND	AA14	NA
NA	GND	AA2	NA
NA	GND	AA24	NA
NA	GND	AA5	NA
NA	GND	AA6	NA
NA	GND	AA7	NA
NA	GND	AB11	NA
NA	GND	AB21	NA
NA	GND	AB3	NA
NA	GND	AB4	NA
NA	GND	AC18	NA
NA	GND	AC28	NA
NA	GND	AC8	NA
NA	GND	AD15	NA
NA	GND	AD25	NA
NA	GND	AD5	NA
NA	GND	AE12	NA
NA	GND	AE2	NA
NA	GND	AE22	NA
NA	GND	AF19	NA
NA	GND	AF29	NA
NA	GND	AF9	NA
NA	GND	AG16	NA
NA	GND	AG26	NA
NA	GND	AG6	NA
NA	GND	AH13	NA
NA	GND	AH23	NA
NA	GND	AH3	NA
NA	GND	AJ10	NA
NA	GND	AJ20	NA
NA	GND	AJ30	NA
NA	GND	AK17	NA
NA	GND	AK27	NA
NA	GND	AK7	NA
NA	GND	B11	NA
NA	GND	B21	NA
NA	GND	B4	NA

Bank	Pin name	Pin	I/O Type
NA	GND	B8	NA
NA	GND	B9	NA
NA	GND	C1	NA
NA	GND	C18	NA
NA	GND	C2	NA
NA	GND	C28	NA
NA	GND	C6	NA
NA	GND	C9	NA
NA	GND	D15	NA
NA	GND	D25	NA
NA	GND	D4	NA
NA	GND	D8	NA
NA	GND	D9	NA
NA	GND	E1	NA
NA	GND	E12	NA
NA	GND	E2	NA
NA	GND	E22	NA
NA	GND	E6	NA
NA	GND	E9	NA
NA	GND	F19	NA
NA	GND	F29	NA
NA	GND	F4	NA
NA	GND	F8	NA
NA	GND	F9	NA
NA	GND	G1	NA
NA	GND	G16	NA
NA	GND	G2	NA
NA	GND	G26	NA
NA	GND	G6	NA
NA	GND	G9	NA
NA	GND	H13	NA
NA	GND	H23	NA
NA	GND	H4	NA
NA	GND	H8	NA
NA	GND	H9	NA
NA	GND	J1	NA
NA	GND	J10	NA
NA	GND	J2	NA
NA	GND	J20	NA
NA	GND	J30	NA

Bank	Pin name	Pin	I/O Type
NA	GND	J6	NA
NA	GND	J9	NA
NA	GND	K17	NA
NA	GND	K27	NA
NA	GND	K4	NA
NA	GND	K8	NA
NA	GND	K9	NA
NA	GND	L1	NA
NA	GND	L14	NA
NA	GND	L2	NA
NA	GND	L24	NA
NA	GND	L6	NA
NA	GND	L9	NA
NA	GND	M12	NA
NA	GND	M14	NA
NA	GND	M16	NA
NA	GND	M18	NA
NA	GND	M21	NA
NA	GND	M4	NA
NA	GND	M8	NA
NA	GND	M9	NA
NA	GND	N1	NA
NA	GND	N11	NA
NA	GND	N13	NA
NA	GND	N15	NA
NA	GND	N17	NA
NA	GND	N2	NA
NA	GND	N28	NA
NA	GND	N6	NA
NA	GND	N9	NA
NA	GND	P10	NA
NA	GND	P12	NA
NA	GND	P16	NA
NA	GND	P18	NA
NA	GND	P25	NA
NA	GND	P4	NA
NA	GND	P8	NA
NA	GND	P9	NA
NA	GND	R1	NA
NA	GND	R11	NA

Bank	Pin name	Pin	I/O Type
NA	GND	R13	NA
NA	GND	R17	NA
NA	GND	R2	NA
NA	GND	R22	NA
NA	GND	R6	NA
NA	GND	R9	NA
NA	GND	T10	NA
NA	GND	T12	NA
NA	GND	T16	NA
NA	GND	T18	NA
NA	GND	T19	NA
NA	GND	T29	NA
NA	GND	T4	NA
NA	GND	T8	NA
NA	GND	U1	NA
NA	GND	U11	NA
NA	GND	U13	NA
NA	GND	U17	NA
NA	GND	U2	NA
NA	GND	U26	NA
NA	GND	U6	NA
NA	GND	U9	NA
NA	GND	V10	NA
NA	GND	V12	NA
NA	GND	V14	NA
NA	GND	V16	NA
NA	GND	V18	NA
NA	GND	V23	NA
NA	GND	V4	NA
NA	GND	V8	NA
NA	GND	V9	NA
NA	GND	W1	NA
NA	GND	W11	NA
NA	GND	W13	NA
NA	GND	W15	NA
NA	GND	W17	NA
NA	GND	W2	NA
NA	GND	W20	NA
NA	GND	W30	NA
NA	GND	W6	NA

Bank	Pin name	Pin	I/O Type
NA	GND	W9	NA
NA	GND	Y17	NA
NA	GND	Y27	NA
NA	GND	Y3	NA
NA	GND	Y4	NA
NA	GND	Y7	NA
NA	GND	Y8	NA
NA	GND	Y9	NA
NA	VCCINT	M11	NA
NA	VCCINT	M13	NA
NA	VCCINT	M15	NA
NA	VCCINT	M17	NA
NA	VCCINT	N10	NA
NA	VCCINT	N12	NA
NA	VCCINT	N14	NA
NA	VCCINT	N18	NA
NA	VCCINT	P11	NA
NA	VCCINT	P17	NA
NA	VCCINT	R10	NA
NA	VCCINT	R12	NA
NA	VCCINT	R18	NA
NA	VCCINT	T11	NA
NA	VCCINT	T17	NA
NA	VCCINT	U10	NA
NA	VCCINT	U12	NA
NA	VCCINT	U18	NA
NA	VCCINT	V17	NA
NA	VCCINT	W18	NA
NA	VCCAUX	P13	NA
NA	VCCAUX	T13	NA
NA	VCCAUX	V13	NA
NA	VCCAUX	V15	NA
NA	VCCAUX	W14	NA
NA	VCCAUX_IO_G0	W12	NA
NA	VCCAUX_IO_G0	V11	NA
NA	VCCAUX_IO_G0	W10	NA
32	VCCO_32	AA19	NA
32	VCCO_32	AB16	NA
32	VCCO_32	AE17	NA
32	VCCO_32	AF14	NA

Bank	Pin name	Pin	I/O Type
32	VCCO_32	AH18	NA
32	VCCO_32	AJ15	NA
33	VCCO_33	AA9	NA
33	VCCO_33	AC13	NA
33	VCCO_33	AD10	NA
33	VCCO_33	AG11	NA
33	VCCO_33	AK12	NA
33	VCCO_33	Y12	NA
34	VCCO_34	AC3	NA
34	VCCO_34	AE7	NA
34	VCCO_34	AF4	NA
34	VCCO_34	AG1	NA
34	VCCO_34	AH8	NA
34	VCCO_34	AJ5	NA
34	VCCO_34	AK2	NA
12	VCCO_12	AC23	NA
12	VCCO_12	AD20	NA
12	VCCO_12	AF24	NA
12	VCCO_12	AG21	NA
12	VCCO_12	AK22	NA
12	VCCO_12	Y22	NA
13	VCCO_13	AA29	NA
13	VCCO_13	AB26	NA
13	VCCO_13	AD30	NA
13	VCCO_13	AE27	NA
13	VCCO_13	AH28	NA
13	VCCO_13	AJ25	NA
14	VCCO_14	P30	NA
14	VCCO_14	R27	NA
14	VCCO_14	T24	NA
14	VCCO_14	U21	NA
14	VCCO_14	V28	NA
14	VCCO_14	W25	NA
15	VCCO_15	J25	NA
15	VCCO_15	K22	NA
15	VCCO_15	L29	NA
15	VCCO_15	M26	NA
15	VCCO_15	N23	NA
15	VCCO_15	P20	NA
16	VCCO_16	A29	NA

Bank	Pin name	Pin	I/O Type
16	VCCO_16	B26	NA
16	VCCO_16	C23	NA
16	VCCO_16	D30	NA
16	VCCO_16	E27	NA
16	VCCO_16	F24	NA
16	VCCO_16	H28	NA
17	VCCO_17	A19	NA
17	VCCO_17	B16	NA
17	VCCO_17	D20	NA
17	VCCO_17	E17	NA
17	VCCO_17	G21	NA
17	VCCO_17	H18	NA
17	VCCO_17	L19	NA
18	VCCO_18	C13	NA
18	VCCO_18	D10	NA
18	VCCO_18	F14	NA
18	VCCO_18	G11	NA
18	VCCO_18	J15	NA
18	VCCO_18	K12	NA
0	VCCO_0	AB6	NA
0	VCCO_0	T9	NA

Service & Supply

Address： No.2, North Siyingmen Road, Donggaodi Street, Fengtai District, Beijing, P.R.China
Department： International Cooperation Department
Telephone： +86 (10) 68757343
Fax： +86 (10) 68757706
Post code： 100076