MMY DDR5 8GB-4800 / 5200 / 5600 / 6000 / 6400 SO-DIMM

General Description

This chapter gives an overview of the 262–pin DDR5 small outline dual in-line memory modules product family and describes its main characteristics.

Features

1. 262-Pin SO-DIMM (Lead-Free) DDR5 SDRAM Memory Module.
2. Data transfer rates: PC5-38400 / 41600 / 44800 / 48000 / 51200.
3. Power supply: VDD: 1.067V ~ 1.166V.
4. Module organization: 1024Meg × 64.
5. DRAM organization: 1024Mb × 16.
6. 16 internal banks; 4 groups of 4 banks each.
7. 16-bit prefetch.
8. BL16, BC8 OTF, BL32, BL32 OTF supported.
9. DFE (Decision Feedback Equalization) for DQ.
10. On-Die ECC.
11. Same Bank Refresh.
12. On Die Termination(ODT) via Mode Register setting.
13. Connectivity Test (CT)

Ordering Information for Compliant Products

Part Number	Compliance Code	Number of Ranks	DRAM Organisation	# of SDRAMs
MM5S8GE4PG-4800C-A00	8GB / PC5-38400 / 40-40-40	1	1Gb x16	4
MM5S8GE4PG-5200C-A00	8GB / PC5-41600 / 42-42-42	1	1Gb x16	4
MM5S8GE4PG-5600C-A00	8GB / PC5-44800 / 46-46-46	1	1Gb x16	4
MM5S8GE4PG-6000C-A00	8GB / PC5-48000 / 48-48-48	1	1Gb x16	4
MM5S8GE4PG-6400C-A00	8GB / PC5-51200 / 52-52-52	1	1Gb x16	4

Pin Assignments

262-Pin DDR5 SO-DIMM							
Front Side		Back Side		Front Side		Back Side	
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	*V*in_BULK	2	HSA	67	*V*SS	68	DQ21_A
3	*V*in_BULK	4	HSCL	69	DQ22_A	70	*V*SS
5	RFU	6	HSDA	71	*V*SS	72	DQ23_A
7	PWR_GOOD	8	PWR_EN	73	DQ24_A	74	*V*SS
9	*V*SS	10	*V*SS	75	*V*SS	76	DQ25_A
11	DQ0_A	12	DQ1_A	77	DQ26_A	78	*V*SS
13	*V*SS	14	*V*SS	79	*V*SS	80	DQ27_A
15	DQ2_A	16	DQ3_A	81	DQS3_A_c	82	*V*SS
17	*V*SS	18	*V*SS	83	DQS3_A_t	84	DM3_A_n
19	DM0_A_n	20	DQS0_A_c	85	*V*SS	86	*V*SS
21	*V*SS	22	DQS0_A_t	87	DQ28_A	88	DQ29_A
23	DQ4_A	24	*V*SS	89	*V*SS	90	*V*SS
25	*V*SS	26	DQ5_A	91	DQ30_A	92	DQ31_A
27	DQ6_A	28	*V*SS	93	*V*SS	94	*V*SS
29	*V*SS	30	DQ7_A	95	CB0_A	96	CB1_A
31	DQ8_A	32	*V*SS	97	*V*SS	98	*V*SS
33	*V*SS	34	DQ9_A	99	CB2_A	100	DQS4_A_c
35	DQ10_A	36	*V*SS	101	*V*SS	102	DQS4_A_t
37	*V*SS	38	DQ11_A	103	CB3_A	104	*V*SS
39	DQS1_A_c	40	*V*SS	105	*V*SS	106	CS0_A_n

41	DQS1_A_t	42	DM1_A_n	107	CA0_A	108	ALERT_n
43	*V*SS	44	*V*SS	109	CA1_A	110	CS1_A_n
45	DQ12_A	46	DQ13_A	111	*V*SS	112	*V*SS
47	*V*SS	48	*V*SS	113	CA2_A	114	CA3_A
49	DQ14_A	50	DQ15_A	115	CA4_A	116	CA5_A
51	*V*SS	52	*V*SS	117	*V*SS	118	*V*SS
53	DQ16_A	54	DQ17_A	119	CA6_A	120	CA7_A
55	*V*SS	56	*V*SS	121	CA8_A	122	CA9_A
57	DQ18_A	58	DQ19_A	123	*V*SS	124	*V*SS
59	*V*SS	60	*V*SS	125	CA10_A	126	CA11_A
61	DM2_A_n	62	DQS2_A_c	**Key**			
63	*V*SS	64	DQS2_A_t	127	CA12_A	128	RFU
65	DQ20_A	66	*V*SS	129	*V*SS	130	*V*SS

Pin Assignments (Continued)

262-Pin DDR5 SO-DIMM							
Front Side		Back Side		Front Side		Back Side	
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
131	CK0_A_t	132	CK1_A_t	197	V_{SS}	198	DQ7_B
133	CK0_A_c	134	CK1_A_c	199	DQ8_B	200	V_{SS}
135	V_{SS}	136	V_{SS}	201	V_{SS}	202	DQ9_B
137	CK0_B_t	138	CK1_B_t	203	DQ10_B	204	V_{SS}
139	CK0_B_c	140	CK1_B_c	205	V_{SS}	206	DQ11_B
141	V_{SS}	142	V_{SS}	207	DQS1_B_c	208	V_{SS}
143	RFU	144	CA12_B	209	DQS1_B_t	210	DM1_B_n
145	CA11_B	146	CA10_B	211	V_{SS}	212	V_{SS}
147	V_{SS}	148	V_{SS}	213	DQ12_B	214	DQ13_B
149	CA9_B	150	CA8_B	215	V_{SS}	216	V_{SS}
151	CA7_B	152	CA6_B	217	DQ14_B	218	DQ15_B
153	V_{SS}	154	V_{SS}	219	V_{SS}	220	V_{SS}
155	CA5_B	156	CA4_B	221	DQ16_B	222	DQ17_B
157	CA3_B	158	CA2_B	223	V_{SS}	224	V_{SS}
159	V_{SS}	160	V_{SS}	225	DQ18_B	226	DQ19_B
161	CS0_B_n	162	CA1_B	227	V_{SS}	228	V_{SS}
163	RESET_n	164	CA0_B	229	DM2_B_n	230	DQS2_B_c
165	CS1_B_n	166	V_{SS}	231	V_{SS}	232	DQS2_B_t
167	V_{SS}	168	CB0_B	233	DQ20_B	234	V_{SS}
169	DQS4_B_c	170	V_{SS}	235	V_{SS}	236	DQ21_B
171	DQS4_B_t	172	CB1_B	237	DQ22_B	238	V_{SS}
173	V_{SS}	174	V_{SS}	239	V_{SS}	240	DQ23_B

175	CB3_B	176	CB2_B	241	DQ24_B	242	V_{SS}
177	V_{SS}	178	V_{SS}	243	V_{SS}	244	DQ25_B
179	DQ0_B	180	DQ1_B	245	DQ26_B	246	V_{SS}
181	V_{SS}	182	V_{SS}	247	V_{SS}	248	DQ27_B
183	DQ2_B	184	DQ3_B	249	DQS3_B_c	250	V_{SS}
185	V_{SS}	186	V_{SS}	251	DQS3_B_t	252	DM3_B_n
187	DM0_B_n	188	DQS0_B_c	253	V_{SS}	254	V_{SS}
189	V_{SS}	190	DQS0_B_t	255	DQ28_B	256	DQ29_B
191	DQ4_B	192	V_{SS}	257	VSS	258	V_{SS}
193	V_{SS}	194	DQ5_B	259	DQ30_B	260	DQ31_B
195	DQ6_B	196	V_{SS}	261	V_{SS}	262	V_{SS}

Pin Descriptions

Symbol	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command / Address bus
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select
DQ0_A – DQ31_A, DQ0_B – DQ31_B,	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)

Symbol	Description
HSCL	SidebandBus clock
HSDA	SidebandBus data
HAS	SidebandBus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a known state
*Vin*_BULK	5V power input supply to the PMIC for analog circuits
Vss	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

Note:
DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.
The signals with suffix:_A (e.g. DQ0_A) are for channel-A, and the signals with suffix:_B (e.g. DQ0_B) are for channel-B

DIMM Voltage Requirements

Symbol	Parameter	Voltage Rating (V)			Maximum Expected Current (A)	Power State
		Min.	TYP.	Max.		
V_{IN}_BULK	Host Supply Voltage	4.25	5.0	5.5	2.5 / 2.0	Operational
SWA, SWB	PMIC Output Supply Voltage	-	1.1	-	6	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	12	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	2	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020	Operational

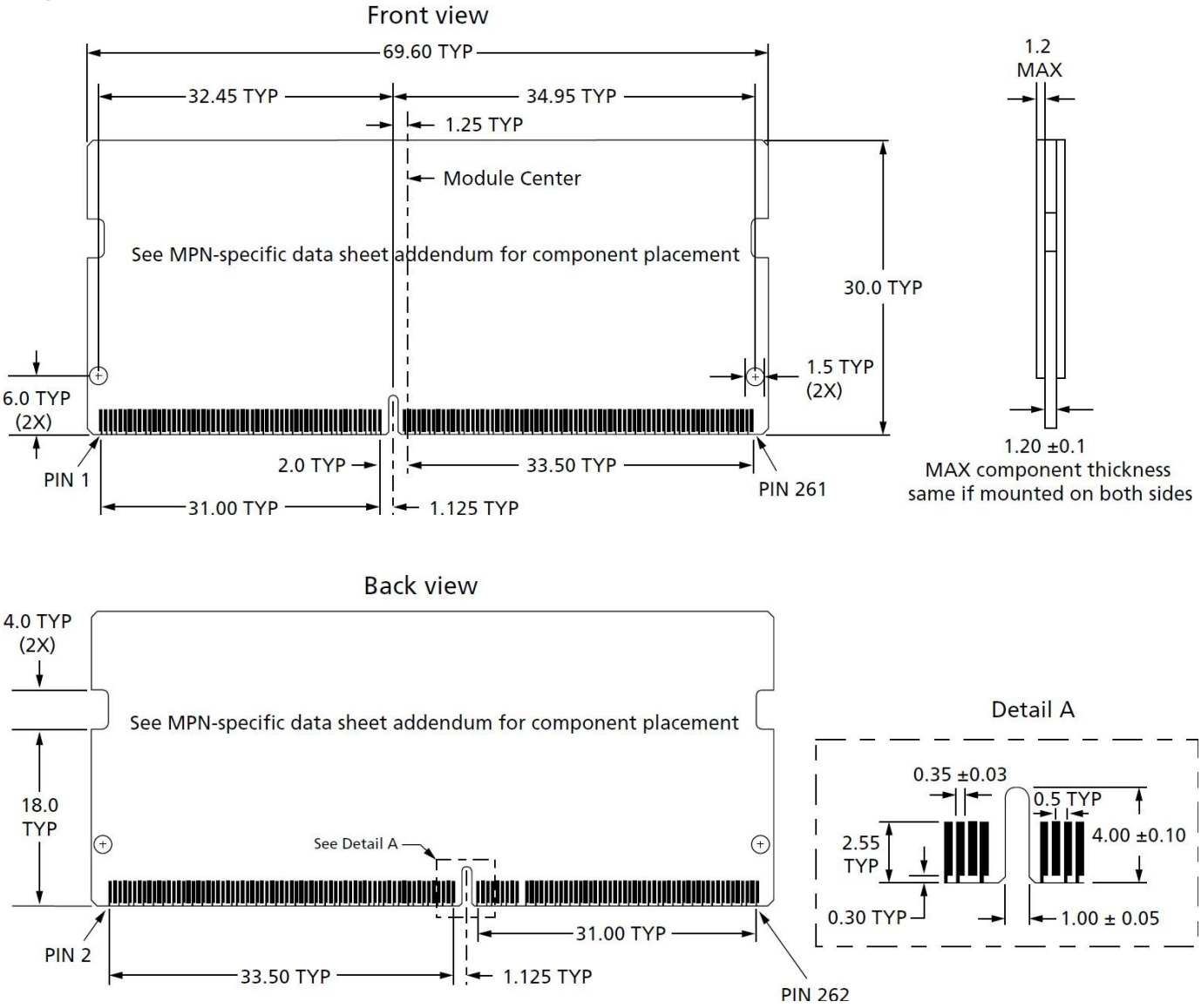
Note:
1. During first power on the input voltage supply must reach minimum 4.25V for PMIC to detect valid input supply.
2. The ramp up rate between 300 mV and 4.0V.
3. The ramp down rate between 4V and 300 mV.
4. The area under the curve above V_{IN}_Bulk = TBD V. V_{IN}_Bulk_AC spec must also be satisfied.
5. The minimum input current requirement is to deliver the maximum output current on V_{OUT}_1.8V and V_{OUT}_1.0V LDO plus the current.
6. V_{IN}_Bulk = 5.0V. Measured at room temperature. All circuitry including output requlators and LDOs are off. VR_EN signal is static.
7. V_{IN}_Bulk = 5.0V. Measured at room temperature. All output requlators and LDOs are on with 0 A output load.. VR_EN signal is static.
8. 20MHz bandwidth limited measurement for all voltage in the table.
9. Voltages are measured at the DIMM gold fingers and at PMIC output pins.
10. The SDRAM specification must be met and take precedence over this document.
11. Maximum current establishes the plaform maximum current regulation point. It provides a data point for DIMM developers ro set power plane impedances.
12. Typical voltage is platform dependent. This is a suggested calue only.
13. Follow JEDEC specification.

Recommended Operating Temperature Ranges

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,3

Note:
- The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer to JESD51-2.
- Normal is themaximum limit when device is operationg in the Normal Temperature Mode.
- Extended is the maximum limit when device is operating in the Extended Temperature Mode.

Physical Dimensions



Note: 1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15 unless otherwise specified.
3.The dimensional diagram is for referecce only.

MMY Part Number Rule