TE0713 TRM

Revision v.13

Exported on 2019-03-07

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0713+TRM

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4 Overview

Refer to https://wiki.trenz-electronic.de/display/PD/TE0713+TRM for the online version of this manual and the rest of available documentation.

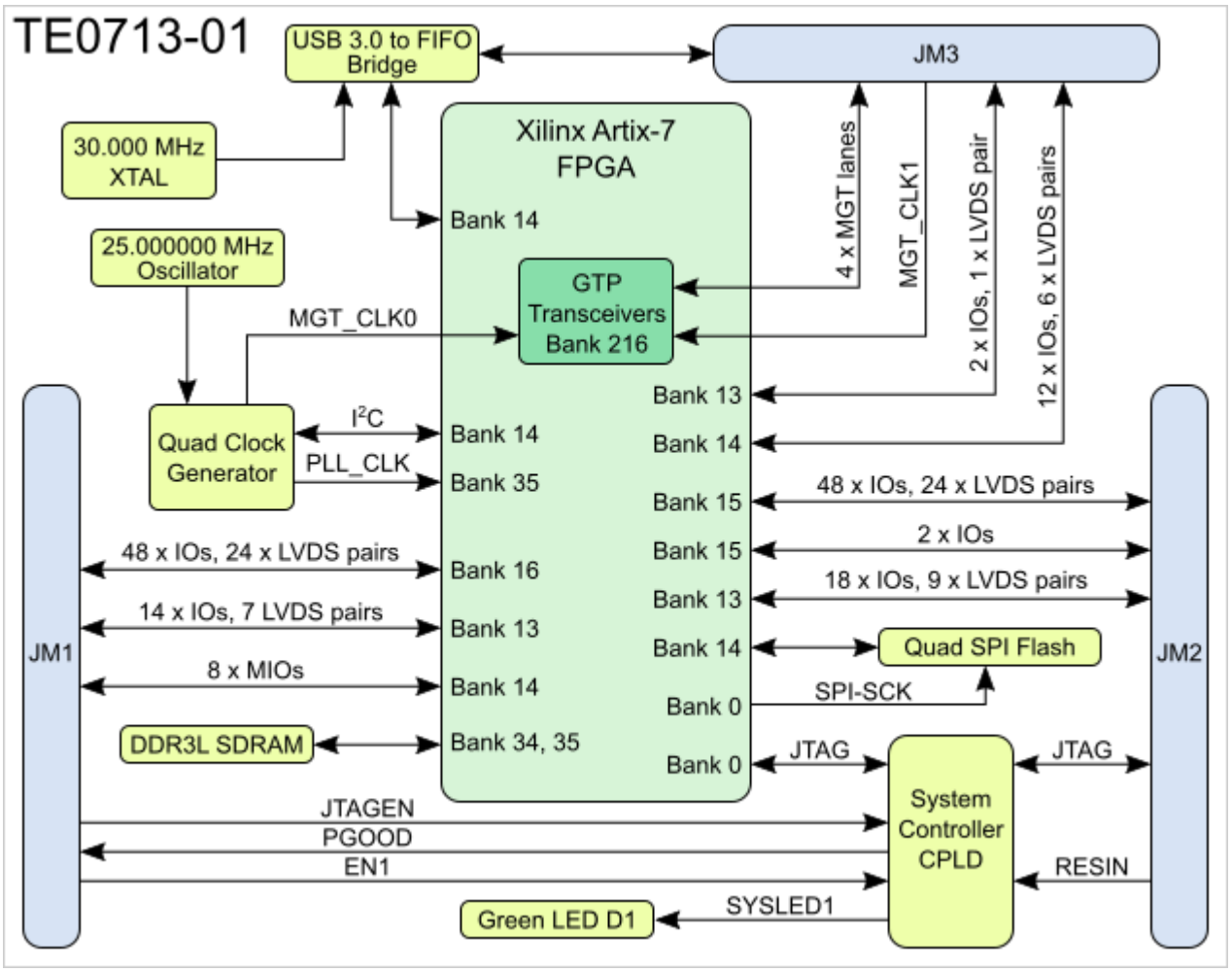
Trenz Electronic TE0713 is an industrial-grade FPGA module integrating Xilinx Artix-7 FPGA, USB 3.0 to FIFO bridge, 1 GByte of DDR3L SDRAM, 32 MByte Flash memory for configuration and operation, and powerful switching-mode power supplies for all on-board voltages. Numerous configurable I/Os are provided via rugged high-speed strips. All this on a tiny footprint, smaller than a credit card size at very competitive price. All Trenz Electronic SoMs in 4 x 5 cm form factor are mechanically compatible.

4.1 Key Features

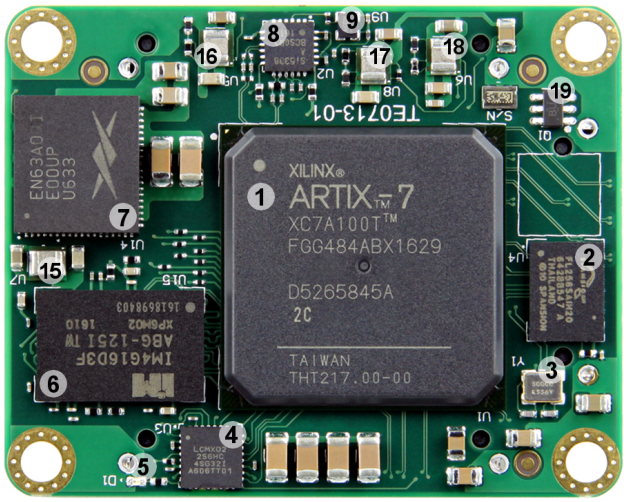
- Xilinx Artix-7 (15T to 200T) series FPGA
- Both industrial and commercial temperature ranges available
- Rugged for high shock and high vibration resistance
- 1 GByte DDR3L 32-bit SDRAM
- 32 MByte QSPI Flash memory (with XiP support)
- USB 3.0 to FIFO interface bridge
- Programmable clock quad generator
    - GTP transceiver clock (default 125 MHz)
    - Fabric clock (default 200 MHz)
- Plug-on module with 2 × 100-pin and 1 × 60-pin high-speed hermaphroditic strips
- 152 FPGA I/Os (75 differential pairs) available via B2B connectors
- 4 GTP (multi Gigabit transceiver) lanes
- External clock input for GTP transceivers via B2B connector
- On-board high-efficiency DC-DC converters
- System management and power sequencing
- eFUSE bit-stream encryption
- AES bit-stream encryption
- User configurable LED
- Evenly-spread supply pins for good signal integrity

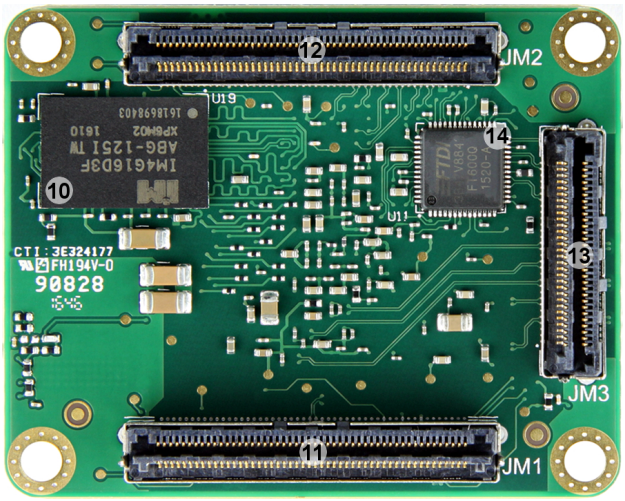
Additional assembly options are available for cost or performance optimization upon request.

4.2 Block Diagram



4.3 Main Components





1. Xilinx Artix-7 XC7A series FPGA, U1
2. 32 MByte QSPI Flash memory, U4
3. 30.000 MHz quartz crystal, Y1
4. System Controller CPLD, Lattice Semiconductor MachXO2-256HC, U3
5. Green LED (SYSLED1), D1
6. 4 Gbit DDR3L 256M x 16 SDRAM, U15
7. Altera Enpirion 12A PowerSoC DC-DC converter, U14
8. Silicon Labs programmable quad clock generator, U2
9. SiTime low-power programmable oscillator @ 25.000000 MHz, U9
10. 4 Gbit DDR3L 256M x 16 SDRAM, U19
11. Samtec Razor Beam™ LSHM-150 B2B connector, JM1
12. Samtec Razor Beam™ LSHM-150 B2B connector, JM2
13. Samtec Razor Beam™ LSHM-130 B2B connector, JM3
14. FTDI USB 3.0 to FIFO interface bridge, U11
15. Texas Instruments 3A step-down converter (DDR_PWR), U7
16. Texas Instruments 3A step-down converter (1.8V), U5
17. Texas Instruments 3A step-down converter (1.2V_MGT), U8
18. Texas Instruments 3A step-down converter (1V_MGT), U6
19. Texas Instruments PFET load switch, Q1

4.4 Initial Delivery State

Programmable unit	Content	Notes
Xilinx Artix-7 FPGA	Not programmed	U1
System Controller CPLD	Programmed	U3
SPI Flash OTP area	Empty	U4
SPI Flash main array	Empty	U4
SPI Flash Quad Enable bit	Set	U4

5 Signals, Interfaces and Pins

5.1 Board to Board (B2B) I/Os

FPGA banks and I/O signals connected to the B2B connectors:

FPGA Bank	B2B Connector	I/O Signal Count	Voltage Level	Notes
13	JM1	14	VCCIO13	Supplied by the baseboard.
13	JM2	18	VCCIO13	Supplied by the baseboard.
13	JM3	2	VCCIO13	Supplied by the baseboard.
14	JM1	8	3.3V	
14	JM3	12	3.3V	
15	JM2	48	VCCIO15	Supplied by the baseboard.
15	JM2	2	VCCIO15	Supplied by the baseboard.
16	JM1	48	VCCIO16	Supplied by the baseboard.

5.2 JTAG Interface

JTAG access to the Xilinx Artix-7 FPGA and System Controller CPLD devices is provided through B2B connector JM2.

JTAG Signal	B2B Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

JTAGEN pin in B2B connector JM1 is used to select JTAG access for FPGA or System Controller CPLD:

JTAGEN	JTAG Access To
Low	Artix-7 FPGA
High	System Controller CPLD

5.3 System Controller I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
PGOOD	Output	Power good	Power Good Pin is zero, if RESIN, EN1, PG_SENSE or PG_DDR_PWR are low, else high impedance. EN1 is also used to enable 1V Power (connected directly outside of the CPLD).
JTAGEN	Input	JTAG select	Low for normal operation, high for System Controller CPLD access.
EN1	Input	Power Enable	When forced low, pulls PROG_B low to emulate power on reset.
RESIN			When forced low, pulls PROG_B low to emulate power on reset.
NOSEQ	-	No function	Not used.
MODE	-	No function	Not used.

Note: Pin functionality depends on the running CPLD Firmware, newest one is described here TE0713 CPLD[1]

5.4 On-board LEDs

The TE0713-01 module has one LED which is connected to the System Controller CPLD. Once FPGA configuration has completed, it can be used by the user's design.

LED	Color	SC Signal	SC Pin	Notes
D1	Green	SYSLED1	8	Exact function is defined by SC CPLD firmware.

1 https://wiki.trenz-electronic.de/display/PD/TE0713+CPLD

5.5 Clocking

On-board Si5338 clock generator chip is used to generate clocks with 25 MHz oscillator connected to the pin IN3 as input reference. There is a I^2C bus connection between the FPGA bank 14 (master) and clock generator chip (slave) which can be used to program output frequencies. See the reference design for more information.

CLK Output	FPGA Bank	FPGA Pin	IO Standard	Net Name	Default Freq	Note
CLK0	-	-	-	-	--	N.C.
CLK1	-	-	-	-	--	N.C.
CLK2	216	F6/E6	Auto	MGT_CLK0_P/N	125 MHz	GTP transceiver clock.
CLK3	35	H4/G4	LVDS	PLL_CLK_P/N	200 MHz	AC coupled, board termination

6 On-board Peripherals

6.1 32 MByte Quad SPI Flash Memory

On-board QSPI flash memory S25FL256S (U14) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

6.2 System Controller CPLD

System Controller CPLD (Lattice Semiconductor MachXO2-256HC, U3) is used to control FPGA configuration process. The FPGA is held in reset (by driving the PROG_B signal low) until all power supplies have stabilized.

CPLD Firmware description:

- TE0713 CPLD Firmware[2]
  - TE0713 CPLD[3]

6.3 DDR3L SDRAM

The TE0713-01 SoM has two 4 Gbit volatile DDR3 SDRAM ICs (U15 and U19) for storing user application code and data.

- Part number: IM4G16D3FABG-125I
- Supply voltage: 1.35V
- Organization: 32M words x 16 bits x 8 banks
- Memory speed: limited by Xilinx Artix-7 speed grade and MIG

Configuration of the DDR3 memory controller in the FPGA should be done using the MIG tool in the Xilinx Vivado Design Suite IP catalog.

6.4 USB 3.0 to FIFO Bridge

TE0713-01 is equipped with the FTDI FT600Q high performance USB 3.0-to-FIFO interface bridge chip.

ⓘ
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SSTX_P and SSTX_N ar swapped on the PCB,this will be corrected
automatically on link training on USB3
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2 https://wiki.trenz-electronic.de/display/PD/TE0713+CPLD+Firmware
3 https://wiki.trenz-electronic.de/display/PD/TE0713+CPLD

7 Power and Power-On Sequence

7.1 Power Supply

Single 3.3V power supply (for both VIN and 3.3VIN power rails) with minimum current capability of 3A for system startup is recommended.

Power Consumption

Typical module power consumption is between 2-3W. Exact power consumption is to be determined.

TE0713-01 module can also be powered by split 5V/3.3V power sources if preferred. In such case apply 5V to B2B connectors VIN pins and 3.3V to 3.3VIN pins, although lowest power consumption is achieved when powering the module from single 3.3V supply. When using split 5V/3.3V supplies the power consumption (and heat dissipation) will rise due to the DC-DC converter efficiency (it decreases when VIN/VOUT ratio rises).

7.2 Power-On Sequence

For the highest efficiency of the on-board DC-DC regulators, it is recommended to use same 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

It is important that all baseboard I/Os are 3-stated at power-on until System Controller sets PGOOD signal high (B2B connector JM1, pin 30), or 3.3V is present on B2B connector JM2 pins 10 and 12, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet DS181 - "Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics" for additional information. User should also check related baseboard documentation when choosing baseboard design for TE0713 module.

7.3 Power Rails

Power Rail Name	B2B Connector JM1 Pin	B2B Connector JM2 Pin	Direction	Notes
VIN	1, 3, 5	2, 4, 6, 8	Input	SoM supply voltage (from the baseboard).
3.3VIN	13, 15	-	Input	SoM supply voltage (from the baseboard).
DDR_PWR	-	19	Output	Module internal supply of 1.35V level.
1V	-	-	-	Module internal supply of 1V level.
1V_MGT	-	-	-	Module internal supply of 1V for bank 216 transceivers.

Power Rail Name	B2B Connector JM1 Pin	B2B Connector JM2 Pin	Direction	Notes
1.2V_MGT	-	-	-	Module internal supply of 1.2V for bank 216 transceivers.
1.8V	39	-	Output	Module internal 1.8V level. Maximum 300mA available.
3.3V	-	10, 12	Output	Module internal 3.3V level.
VCCIO13	-	1, 3	Input	High-Range bank supply voltage (from the baseboard).
VCCIO15	-	7, 9	Input	High-Range bank supply voltage (from the baseboard).
VCCIO16	9, 11	-	Input	High-Range bank supply voltage (from the baseboard).
VREF_JTAG	-	91	Output	JTAG reference voltage (3.3V).

8 Board to Board Connectors

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors[4] on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

8.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Table 1: Connectors.
The module can be manufactured using other connectors upon request.

4 https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=LSHM

8.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Table 2: Speed rating.

8.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

8.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

9 Variants Currently In Production

Module Variant	FPGA	Junction Temperature	Temperature Range
TE0713-01-100-2C	XC7A100T-2FGG484C	0°C to 85°C	Commercial grade
TE0713-01-200-2C	XC7A200T-2FBG484C	0°C to 85°C	Commercial grade

10 Technical Specifications

10.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	-0.3	7.0	V	See EN63A0QI and TPS82085 datasheets.
3.3VIN supply voltage	-0.5	3.75	V	See LCMXO2-256HC datasheet.
HR I/O banks supply voltage (VCCO)	-0.5	3.6	V	Xilinx datasheet DS181[5]
HR I/O banks input voltage	-0.4	VCCO + 0.55	V	Xilinx datasheet DS181[6]
GTP transceivers Tx/Rx input voltage	-0.5	1.26	V	Xilinx datasheet DS181[7]
Storage temperature	-55	100	°C	See IM4G16D3FABG datasheet.

10.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	2.5	6.0	V	See TPS82085 datasheet.
3.3VIN supply voltage	2.375	3.6	V	See LCMXO2-256HC datasheet.
HR I/O banks supply voltage (VCCO)	1.14	3.465	V	Xilinx datasheet DS181[8]
HR I/O banks input voltage	-0.20	VCCO + 0.2	V	Xilinx datasheet DS181[9]

5 https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf
6 https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf
7 https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf
8 https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf
9 https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf

10.3 Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

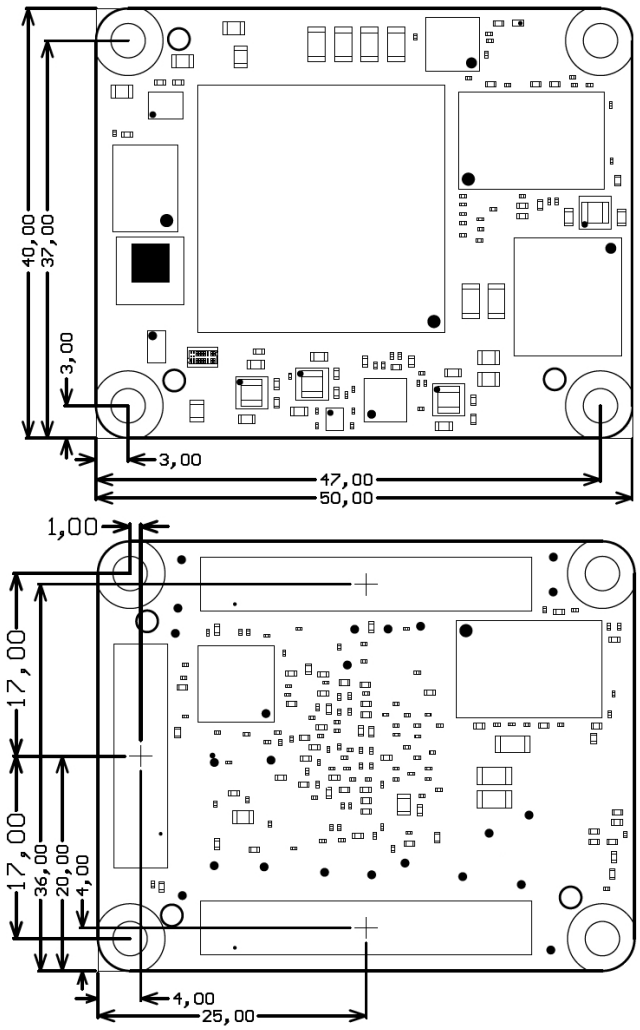
Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

> Assembly variants for higher storage temperature range are available on request.

10.4 Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 2.5mm. Please download the step model for exact numbers.

All dimensions are shown in millimeters.



10.5 Weight

21 g Plain module.

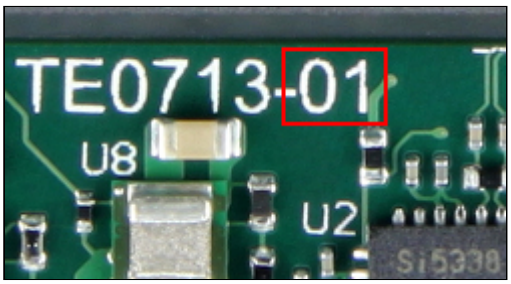
8.8 g Set of nuts and bolts.

11 Revision History

11.1 Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2016-06-30	01	First production revision		TE0713-01[10]

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.



11.2 Document Change History

Date	Revision	Contributors	Description
2019-03-07	v.13 (see page 6)	John Hartfiel[11], Jan Kumann[12], Susanne Kunath[13], Thorsten Trenz[14]	• History bugfix • Correction of System Controller IO description
24.10.2018	v.11	John Hartfiel	• Note USB3
19.09.2018	v.9	John Hartfiel	• add default SI5338 clk table

10 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/TE0713/REV01
11 https://wiki.trenz-electronic.de/display/~j.hartfiel
12 https://wiki.trenz-electronic.de/display/~j.kumann
13 https://wiki.trenz-electronic.de/display/~s.kunath
14 https://wiki.trenz-electronic.de/display/~tht

Date	Revision	Contributors	Description
08.06.2018	v.8	John Hartfiel	• replace B2B connector section
2017-05-28	v.6	Jan Kumann	• Absolute and recommended ratings added. • Main components section improved. New top PCB image. • Power rails section improved. • New physical dimensions images.
2017-02-07	v.1	Jan Kumann	• Initial document.

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

2018-09-18

15 http://guidance.echa.europa.eu/
16 https://echa.europa.eu/candidate-list-table
17 http://www.echa.europa.eu/

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