Shenzhen Leadtek Electronics Co.,Ltd

PRODUCT SPECIFICATION

TFT-LCD MODULE

Module No：LTK055HDHLM15-V0

☑ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
		

Final Approval by Customer

Approved by	Comment

※The specification of “TBD” should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

Record of Revisions

Rev.	Date	Sub-Model	Description of change
1.0	Jun.,28 ,2023	V0	new

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1.0 GENERAL DESCRIPTION

1.1 Introduction

Leadtek Display model LTK055HDHLM15-V0 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is a reflective type display. This TFT LCD has a 5.46 inch diagonally measured active display area with (720 horizontal by 1280 vertical pixel) resolution.

1.2 Features

- 5.46 (9:16 diagonal) inch configuration
- 16.7M color by 8 bit R.G.B. signal input
- RoHS Compliance &Halogen Free

1.3 Application

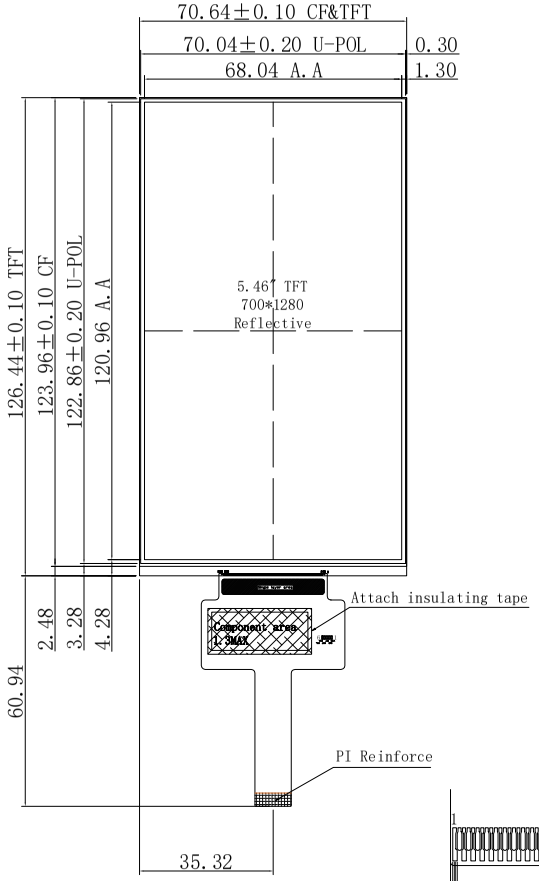
- Industrial Control Application

1.4 General Information

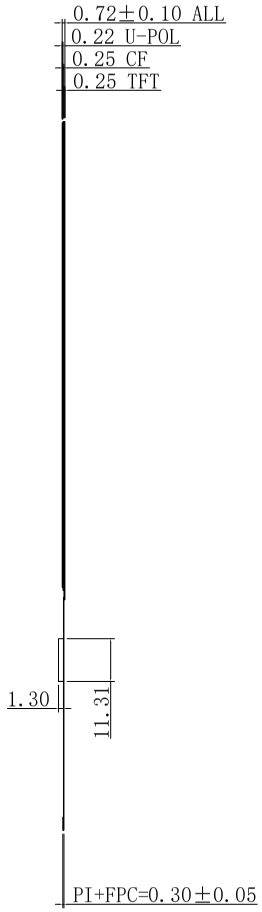
Item	Specification	Unit
Outline Dimension	70.64(H)x126.44(V) x0.72 (T) (Typ.)	mm
Display Area	68.04(H)x120.96(V)	mm
Number of Pixel	720x(RGB)x1280	pixel
Pixel Pitch	0.0945x0.0945	mm
Pixel Arrangement	RGB Vertical Stripe	
Display Mode	Normally White	

1.1 structural drawings

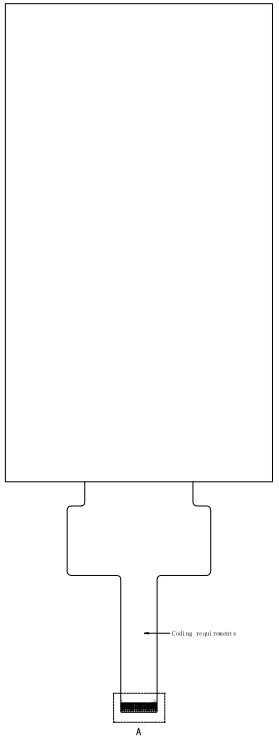
Front View

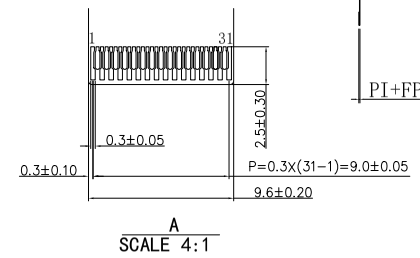


Side View



Back View





A
SCALE 4:1

Display Pin interface

1	GND
2	TOUCH_3V3
3	GND
4	TOUCH_INT
5	TOUCH_RST
6	TOUCH_SDA
7	TOUCH_SCL
8	GND
9	LED K
10	LED A
11	TE
12	RSTN
13	NC
14	IOVCC_3v3
15	VCC_3v3
16	GND
17	D3P
18	D3N
19	GND
20	D2P
21	D2N
22	GND
23	CKP
24	CKN
25	GND
26	D1P
27	D1N
28	GND
29	D0P
30	D0N
31	GND

Notes:
1. Display : 5.46", TFT
2. Resolution: 700xRGBx1280
3. LCD Viewing Direction: 60/60/60/60
4. Drive IC:ILI9881C
5. Display Mode: Normally White/Reflective/RBW
6. unmark Tolerance:±0.2
7. OPERATING TEMP: -20° C~ +70° C
8. STORAGE TEMP: -30° C~ +80° C
9. Requirements on Environmental Protection: ROHS

REV	DESCRIPTION	DATE	NAME
3			
2			
1			
0	NEW	2023.08.10	Jerry

LEADTEK DISPLAY

LEADTEK COMPANY LIMITED

SCALE:1/1	UNIT:mm	PAGE:1/1	Approve	Check	Drawn
Part No:	LTK055HDHLM15	VER:V0	Ian	Jack	Jerry
Customer No:					

1.2 INTERFACE SIGNAL

Pin No.	Symbol	Description
1	GND	Power Ground
2	TOUCH_3V3	Power supply for CTP.
3	GND	GND pin for CTP
4	TOUCH_INT	INT pin for CTP
5	TOUCH_RST	Reset pin for TP
6	TOUCH_SDA	SDA pin for CTP
7	TOUCH_SCL	SCL pin for CTP
8	GND	Power Ground
9	LED K	LED cathode.
10	LED A	LED anode.
11	TE	Tearingeffectoutput(Reserved)
12	RSTN	Reset signal（LowW Active)
13	NC	Not connect
14	IOVCC_3v3	A supply voltage to the digital circuit. (1.8V)
15	VCC_3v3	A supply voltage to the digital circuit. (3.3V)
16	GND	Power Ground
17	D3P	MIPI DSI differential data 3 postive
18	D3N	MIPI DSI differential data 3 negative
19	GND	Power Ground
20	D2P	MIPI DSI differential data 2 postive
21	D2N	MIPI DSI differential data 2 negative
22	GND	Power Ground
23	CKP	MIPI DSI differential clock postive
24	CKN	MIPI DSI differential clock negative
25	GND	Power Ground
26	D1P	MIPI DSI differential data 1 postive
27	D1N	MIPI DSI differential data 1 negative
28	GND	Power Ground
29	D0P	MIPI DSI differential data 0 postive
30	D0N	MIPI DSI differential data 0 negative
31	GND	Power Ground

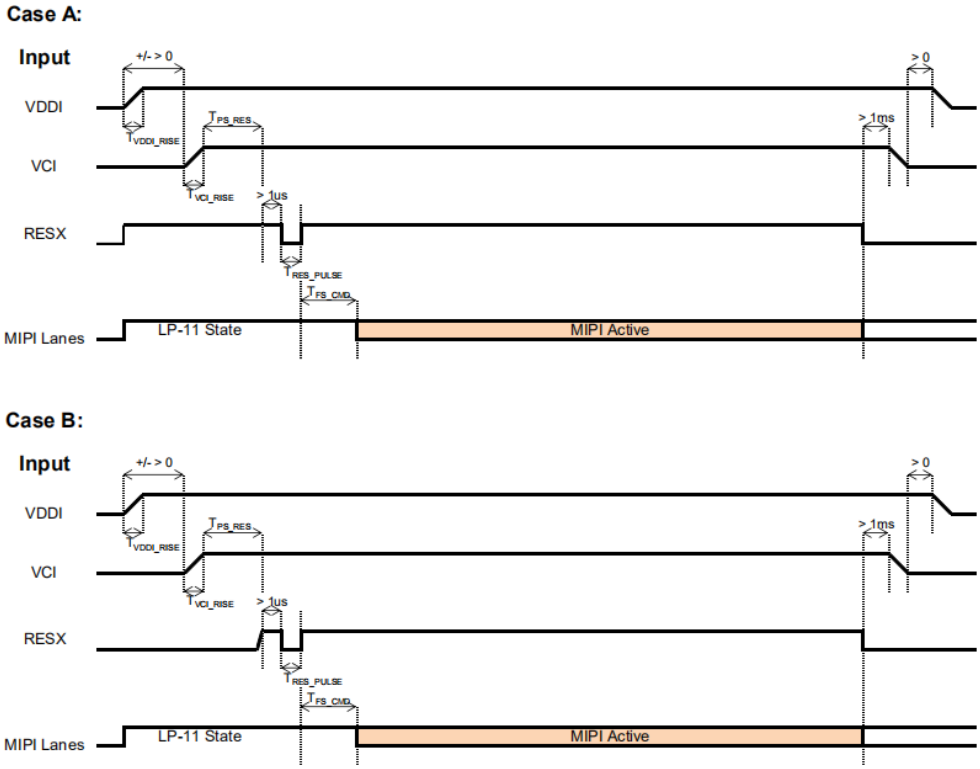
2.Electrical Specifications

2.1 Absolute Maximum Rating

Item	Sym	Value	Unit	Remark
I/O Power Supply	IOVCC1.8	1.65~3.6	V	-
Analog Power Supply Voltage	VCI 2.8V	2.5~6		-
TP Analog Power Supply Voltage	VCI 2.8V_CTP	2.5~3.3		-
Input high voltage	VIH	0.7*IOVCC1.8	V	-
Input low voltage	VIL	0	V	-

2.2 Timing Characterize

2.2.1 DSI Power On/Off Timing



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	20	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	200	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 105: Power on/off sequence with Power Mode 3

2.2.2 Reset Timing

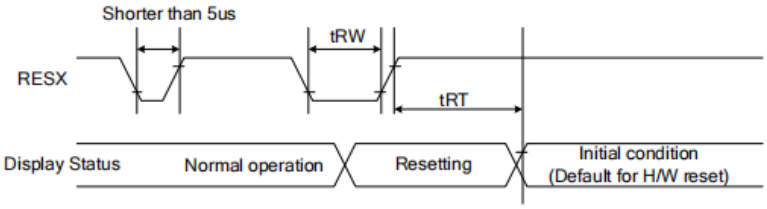


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

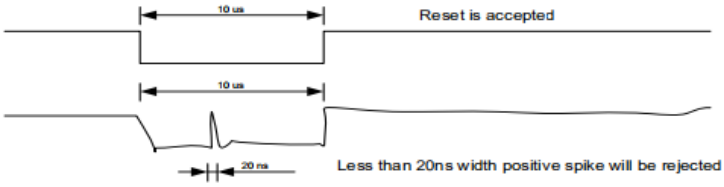


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

Note: *Ta = -30℃ to 70℃ (to +85℃ no damage)*

3.1. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Notes:

1.Ta = -30℃ to 70℃ (to +85℃ no damage)

2. DSI High Speed mode is off.

3.2 DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF

Notes:

1. Ta = -30℃ to 70℃ (to +85℃ no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V

2. Includes 50mV (-50mV to 50mV) ground difference

3. Without VCMRCLKM450/VCMRDATAM450

4. Without 50mV (-50mV to 50mV) ground difference

5. n = 0 and 1

6. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than VTHH (CLKP/DnP). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than VTHL (CLKN/DnN). There is undefined state if the differential voltage is less than VTHH (CLKP/DnP) and less than VTHL (CLKN/DnN). A reference figure is below.

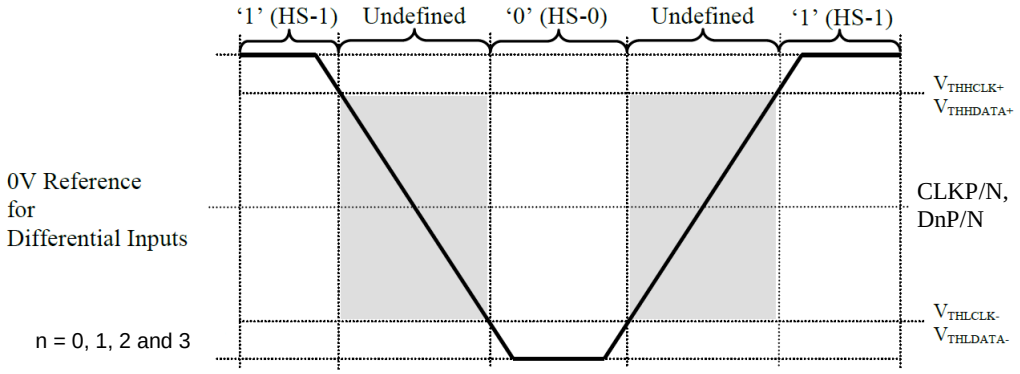
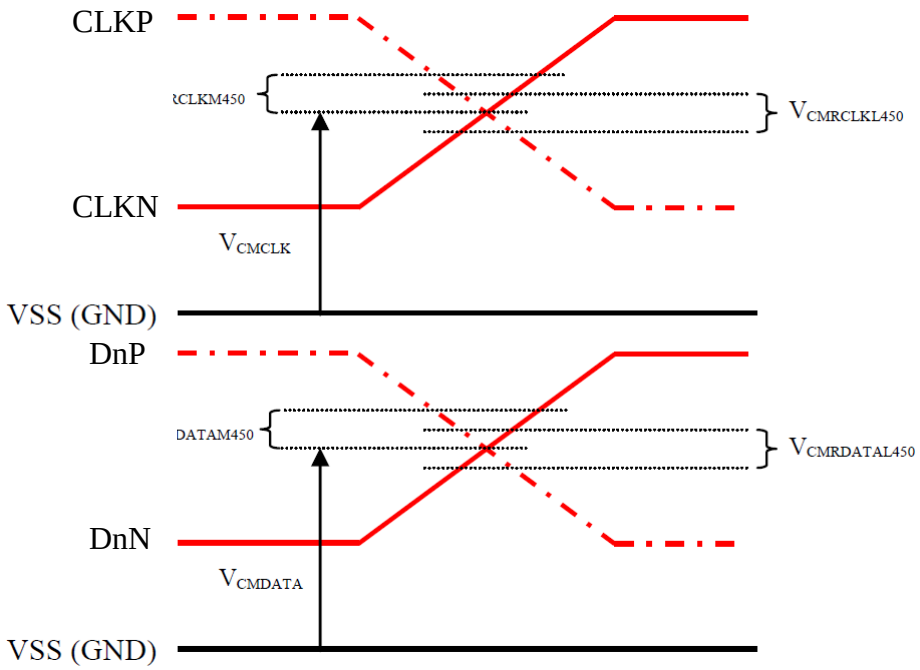


Figure 102: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range



Note: *n = 0, 1, 2 and 3*

Figure 103: Common Mode Voltage on Clock and Data Channels

4. AC Characteristics

4.1. DSI Timing Characteristics

4.2. High Speed Mode – Clock Channel Timing

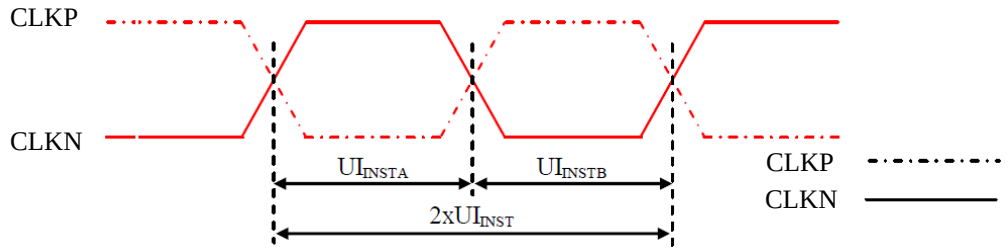


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. I = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

5.0 OPTICAL CHARACTERISTICS

5.1 Optical Specification (w/HSD FOG+ D65 light)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
White Reflectance (with Polarizer)		Rw (%)	Θ=0 Normal viewing angle —	—	20.10	—	%	(4) Measuring with HSD polarizer， Reference Only Base on Vop=4.2V
Contrast Ratio(CR>2)		CR		—	15	—	—	(1)(2) Base on Vop=4.2V
NCS		S%		—	35	—	%	
Response Time		ms		—	5	7		
Color Chromaticity (CIE1931)	White	W_x		—	(0.300)	—		(1)(4) Measuring with HSD polarizer， Reference Only
		W_y		—	(0.346)	—		
	Red	R_x		—	(0.405)	—		
		R_Y		—	(0.325)	—		
	Green	G_x		—	(0.298)	—		
		G_Y		—	(0.403)	—		
	Blue	B_x		—	(0.203)	—		
		B_Y		—	(0.275)	—		
Viewing Angle	Hor.	Θ_L	CR>2	—	60	—	—	(1)(4) Measuring with HSD polarizer， Reference Only
		Θ_R		—	60	—		
	Ver.	Θ_U		—	60	—		
		Θ_D		—	60	—		

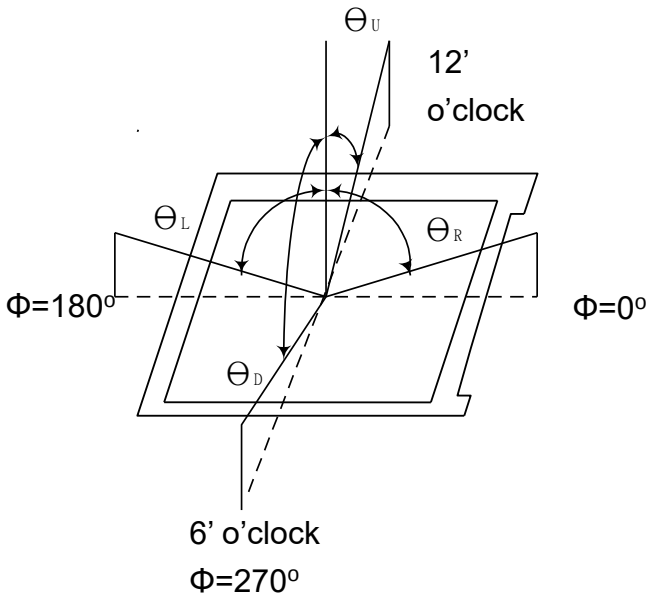
5.2 Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

5.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle:

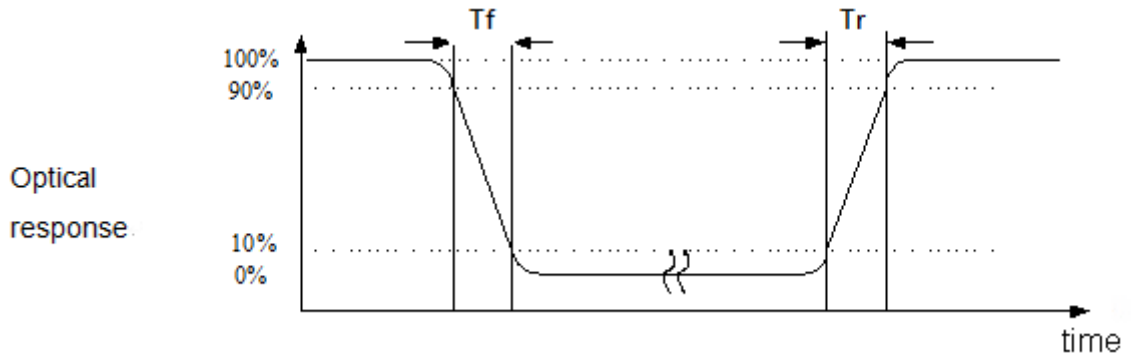


Note (2) Definition of Contrast Ratio (CR) :

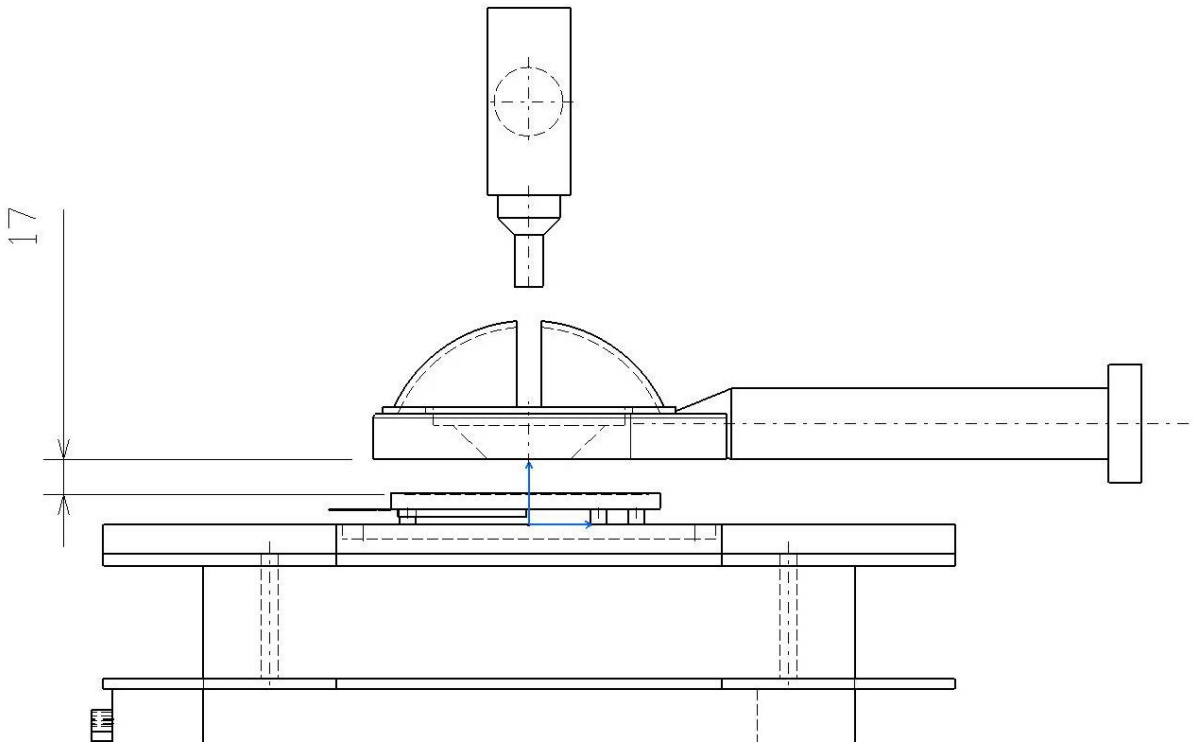
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

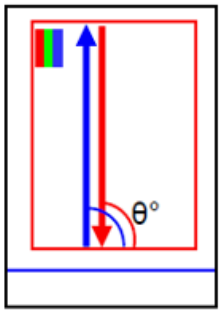
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup

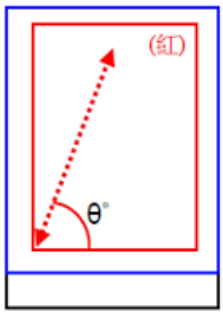


Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



Array Film up
CF Film down

Item	Specifications	Unit	Note
Rubbing Direction	90° (TFT)/ 270° (CF)	degree	Array Film up CF Film down
Absorption axis of Polarizer	15° (CF)	degree	Protective film on top Glue layer face down



CF side polarizing absorption angle θ=15° (Protective film on top, glue layer face down)

7.0 RELIABILITY TEST ITEMS

No.	Item	Conditions	Remark
1	High Temperature Storage	Ta=+80°C, 240hrs	-
2	Low Temperature Storage	Ta=-30°C, 240hrs	-
3	High Temperature Operation	Ta=+70°C, 240hrs	-
4	Low Temperature Operation	Ta=-20°C, 240hrs	-
5	High Temperature and High Humidity (Operating)	Ta=+60°C, 90%RH, 240hrs	-

Note: (1) All tests above are practiced at module type.

(2) There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

10.0 GENERAL PRECAUTION

10.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

10.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. Leadtek does not warrant the module, if customers disassemble or modify the module.

10.3 Breakage of LCD Panel

10.3.1. If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystals, and do not contact liquid crystal with skin.

10.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

10.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

10.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

10.4 Electric Shock

10.4.1. Disconnect power supply before handling LCD module.

10.4.2. Do not pull or fold the LED cable.

10.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

10.5 Absolute Maximum Ratings and Power Protection Circuit

10.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

10.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

10.5.3. It's recommended to employ protection circuit for power supply.

10.6 Operation

10.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

10.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

10.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft materials.

10.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

10.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

10.7 Mechanism

Please mount LCD module by using mounting holes arranged in four corners tightly.

10.8 Static Electricity

10.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

10.8.2 Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

10.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

10.10 Disposal

When disposing LCD module, obey the local environmental regulations.