

Shenzhen Leadtek Electronics Co.,Ltd

PRODUCT SPECIFICATION

TFT-LCD MODULE

Module No: LTK080FHBLM17-V0

☒ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
<i>jona</i>	<i>tom</i>	<i>lan</i>

Final Approval by Customer

Approved by	Comment

※The specification of "TBD" should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.



REVISION HISTORY

REV.	PAGE	DESCRIPTION OF CHANGES	DATE	PREPARED
V0		Initial Release	2023.07.04	



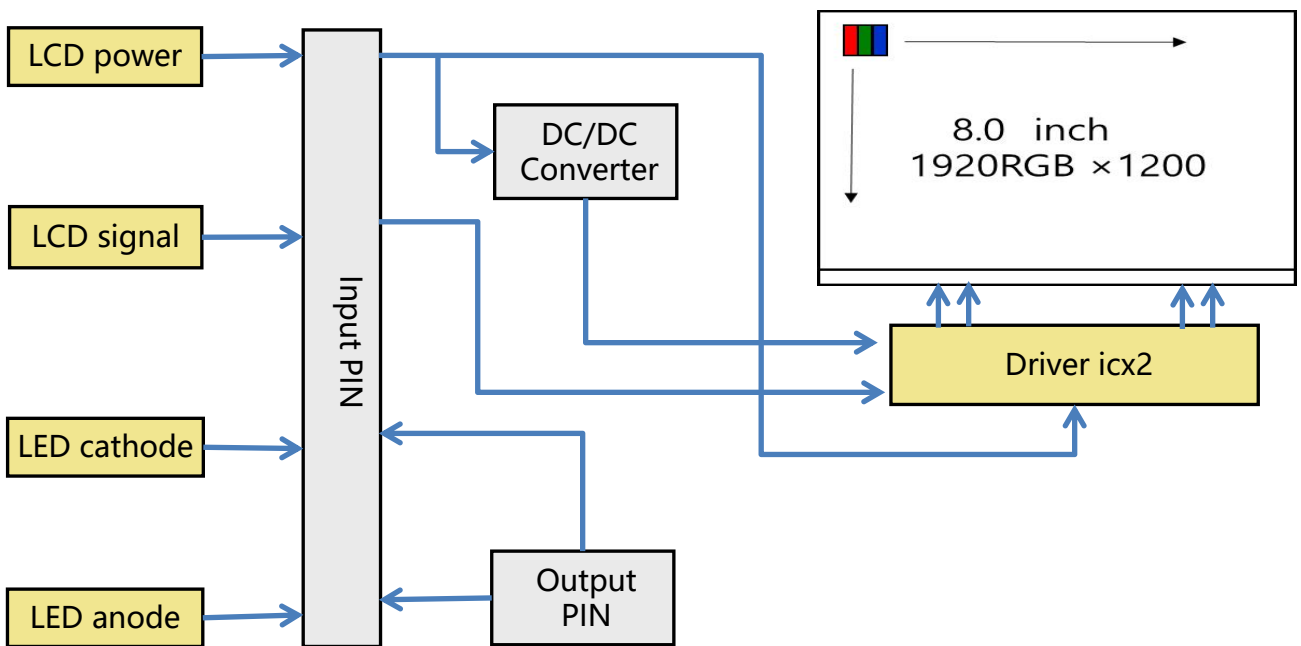
CONTENTS

NO.	ITEMS	PAGE
1.0	General Description	4
2.0	Absolute Maximum ratings	6
3.0	Electrical specifications.	7
4.0	Interface Connection	8
5.0	Power Sequence	13
6.0	Optical specifications.	14
7.0	LC Align Direction & Pol absorption axis	17
8.0	Outline Drawing	18
9.0	Reliability Test	19
10.0	Label	20
11.0	Precautions	22

1.0 GENERAL DESCRIPTION

LTK080FHBLM17-V0 is a color active matrix a-Si LCD , using a-Si (amorphous silicon) TFTs (Thin Film Transistors) as an active switching devices, has a 8.0 inch diagonally measured active area with 1920×1200 resolutions (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this TFT can display 16.7M colors.

<Figure 1. FOG>



1.2 Features

- PPI: 283
- Color Gamut: NTSC 75%(Typ.)
- 1920RGB*1200 LVDS
- RoHS Compliant

1.3 Application

- Outdoor photography



1.4 General Specification

The followings are general specifications of the LTK080FHBLM17-V0.

<Table 1. General Specifications>

[Ta= 25±2°C]

Parameter	Specification	Unit	Remark
Dimensional Outline	181.70(H) × 119.80(V) × 5.50(V)	mm	Note
Active Area	172.224(H) × 107.640(V)	mm	Note 1.1
Border(L/R/U/D)	2/2/2/7	mm	-
Number of Pixels	1920(H)×RGB× 1200 (V)	pixels	-
Pixel Pitch	29.9(H)×3×89.7(V)	μm	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Display Colors	16.7M	-	-
Color Gamut	70%(Min.), 75% (Typ.)		CF @C Light
Display Mode	Normally Black	-	-
Viewing Direction	85/85/85/85 (Typ.) 80/80/80/80 (Min.)	Deg.	CR>=10
Weight	TBD	gram	-
interface	2-port LVDS (8bit)	-	-
IC	FL5893DA		Note 1.2

Note 1.1: H: horizontal length, V: vertical length.

Note 1.2: Compatible ICs for this product include FL5893DA, Please contact IC manufacturer and vetify it when you choose any one of them. The information we suppose about IC just for reference.



2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage values are listed in Table 2. All the measurements should be operated with driver IC and FPC mounted.

<Table 2. Absolute Maximum Ratings>

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDDIN	-0.3	+6.0	V	Note 1&2
Operating Temperature (Humidity)	T _{OP}	-30	+85	°C	
	RH	-	90	%	At 60° C
Storage Temperature (Humidity)	T _{ST}	-30	+85	°C	
	RH	-	90	%	At 60° C

Note:

1. These range above is maximum value not the actual operating temperature . Actual Operating temperature is no more than 40°C and temperature refers to the LCM surface temperature;
2. Leadtek display is not responsible for product problems beyond the use conditions.

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

<Table 3. LCD TFT Electrical Specifications >

Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max.		
Power Supply Input Voltage		VDDI	3.0	3.3	3.6	V	Ta = 25 °C Note 1
Current Consumption	Operating	VDDI	-	TBD	-	mW	-
	Sleep in	VDDI	-	TBD	-	uW	

Note:

1. Stresses exceed the absolute maximum ratings listed above may cause permanent damage to IC. The IC should be operated under the condition of DC/AC characteristics for normal operation. If this condition is not met, the IC may be malfunctioned, or the reliability may drop. Parameters are valid in the operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

4.0 INTERFACE CONNECTION.

4.1 Electrical Interface Connection & Panel Pin Map

The Interface Connector assignments are listed in Table 4.

< Table 4. Pin Assignments for the Interface Connector >

No.	Symbol	Function	No.	Symbol	Function
1	VLED-	Power for LED backlighr (Cathode)	24	GND	ground
2	VLED-	Power for LED backlighr (Cathode)	25	OLV2P	LVDS differential data input Positive
3	VLED+	Power for LED backlighr (Anode)	26	OLV2N	LVDS differential data input Negative
4	VLED+	Power for LED backlighr (Anode)	27	GND	ground
5	NC	No connection	28	OLVCLKP	LVDS differential data input Positive
6	GND	ground	29	OLVCLKN	LVDS differential data input Negative
7	ELV3P	LVDS differential data input Positive	30	GND	ground
8	ELV3N	LVDS differential data input Negative	31	OLV1P	LVDS differential data input Positive
9	GND	ground	32	OLV1N	LVDS differential data input Negative
10	ELV2P	LVDS differential data input Positive	33	GND	ground
11	ELV2N	LVDS differential data input Negative	34	OLV0P	LVDS differential data input Positive
12	GND	ground	35	OLV0N	LVDS differential data input Negative
13	ELVCLKP	LVDS differential data input Positive	36	GND	ground
14	ELVCLK N	LVDS differential data input Negative	37	I2C _SDA	data input/output for I2C(please let these pins open.)
15	GND	ground	38	I2C _SCL	Clock signal for I2C(please let these pins open.)
16	ELV1P	LVDS differential data input Positive	39	VDD_OTP	Power supply for OTP circuit(please let these pins open.)
17	ELV1N	LVDS differential data input Negative	40	EEPEN	Only test Pin(please let these pins open.)
18	GND	ground	41	VDDIN	Power supply
19	ELV0P	LVDS differential data input Positive	42	VDDIN	Power supply
20	ELV0N	LVDS differential data input Negative	43	VDDIN	Power supply
21	GND	ground	44	VDDIN	Power supply
22	OLV3P	LVDS differential data input Positive	45	VDDIN	Power supply
23	OLV3N	LVDS differential data input Negative			

connector:FH34SRJ-45S-0.5SH(50)

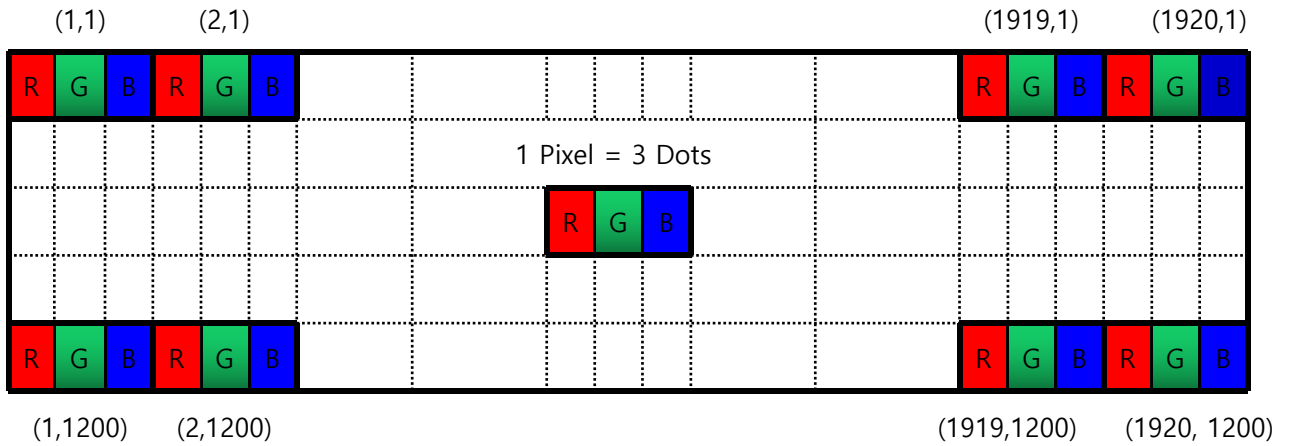
< Table 5. Panel Pin Map >

Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol
1	DUMMY	19	DUMMY	37	BIST	55	VSSP	73	ERR	91	VGMNMI	109	VSSRX	127	D1[7]	145	D2[3]	163	VDDI
2	NULL	20	VSSA	38	GDSEL	56	VSSI	74	TP_SYNC	92	VGMNMI	110	DE	128	D1[6]	146	D2[2]	164	VDDI
3	GND_AG	21	VSSI	39	HW_CTRL	57	VSSI	75	CPUS[1]	93	VGMNHI	111	VS	129	VSSRX	147	VSSRX	165	I2C_SPI_SEL
4	GND_AG	22	VCOM_L	40	CID[1]	58	VSSI	76	CPUS[0]	94	VGMNHI	112	HS	130	D1[5]	148	D2[1]	166	I2C_SCL
5	GND_AG	23	VCOM_L	41	CID[0]	59	VDDP	77	VGMNLO	95	VGMPLI	113	DCLK	131	D1[4]	149	D2[0]	167	I2C_SDA
6	GND	24	THROUGH_2	42	WRBYCID	60	VDDP	78	VGMNLO	96	VGMPLI	114	VSSRX	132	VSSRX	150	VSSRX	168	SPI_CSB
7	GND	25	THROUGH_2	43	ROM_RLD	61	VDDI	79	VGMNMO	97	VGMPMI	115	D0[7]	133	D1[3]	151	VSSRX	169	SPI_SCL
8	GND	26	VCOM	44	EXT_PWR_2	62	VDDI	80	VGMNMO	98	VGMPMI	116	D0[6]	134	D1[2]	152	VSSI	170	SPI_SDAI
9	VCOM	27	VCOM	45	IFSEL[1]	63	VDDI	81	VGMNHO	99	VGMPHI	117	VSSRX	135	VSSRX	153	VSSI	171	SPI_SDAO
10	VCOM	28	EXT_PWR	46	IFSEL[0]	64	VRSN	82	VGMNHO	100	VGMPHI	118	D0[5]	136	D1[1]	154	VSSI	172	VMONP
11	DY_GND	29	INV[1]	47	BIT8	65	VRSN	83	VGMPLI	101	V15D	119	D0[4]	137	D1[0]	155	V15D_RX	173	VMONP
12	DM_GND	30	INV[0]	48	MODE	66	VRSN	84	VGMPLI	102	V15D	120	VSSRX	138	VSSRX	156	V15D_RX	174	VSP
13	VGL	31	RES[3]	49	NB	67	VSSA	85	VGMPLI	103	V15D	121	D0[3]	139	D2[7]	157	V15D	175	VSP
14	VGL	32	RES[2]	50	RL	68	VSSA	86	VGMPLI	104	VSSI	122	D0[2]	140	D2[6]	158	V15D	176	VSP
15	DUMMY	33	RES[1]	51	UD	69	VSSA	87	VGMPLI	105	VSSI	123	VSSRX	141	VSSRX	159	V15D	177	DRVVP
16	VGH	34	RES[0]	52	RSTB	70	VRSP	88	VGMPLI	106	VSSI	124	D0[1]	142	D2[5]	160	VDDRX	178	DRVVP
17	VGH	35	GDPOS[1]	53	STBYB	71	VRSP	89	VGMNLI	107	VSSRX	125	D0[0]	143	D2[4]	161	VDDRX	179	VRSP
18	VGH	36	GDPOS[0]	54	VSSP	72	VRSP	90	VGMNLI	108	VSSRX	126	VSSRX	144	VSSRX	162	VDDI	180	VRSP

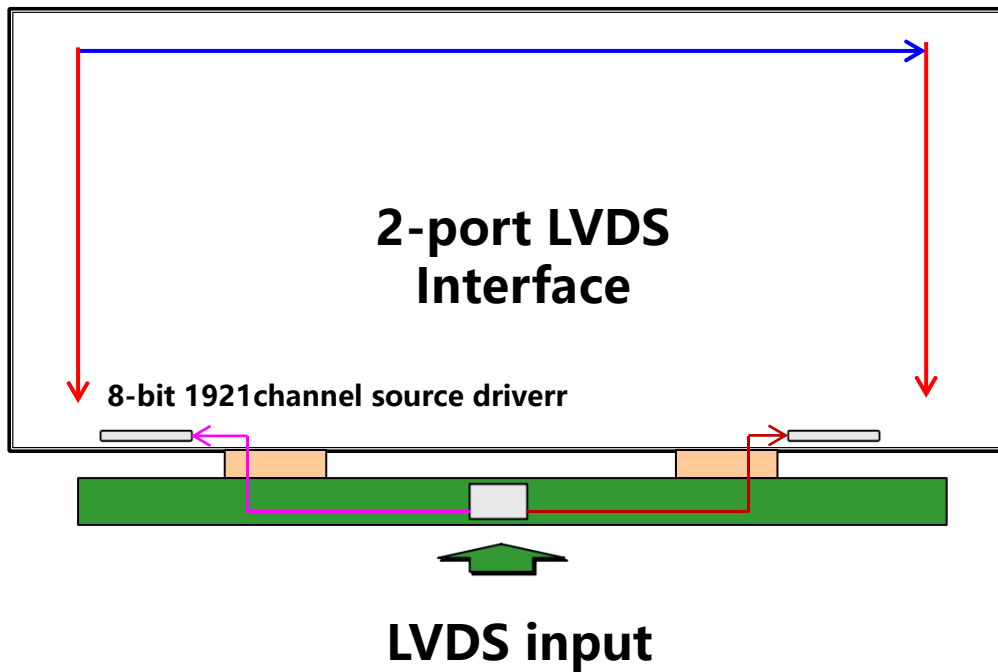
Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol	Pin No	Symbol
181	VRSP	199	VRNL	217	CHP3	235	CLN2	253	VGL
182	VSSA	200	VRNL	218	DUMMY	236	VDD_MTP	254	DC_GND
183	VSSA	201	VSS_PFM	219	VGH	237	VDD_MTP	255	SW_VGL
184	VSSA	202	VSS_PFM	220	VGH	238	VDD_MTP	256	VCOM
185	VRSN	203	VSS_PFM	221	VGH	239	THROUGH_1	257	VCOM
186	VRSN	204	VREGP	222	DUMMY	240	THROUGH_1	258	GND
187	VRSN	205	VREGP	223	VGL	241	VCOM_R	259	GND
188	VDD_PFM	206	CHN1	224	VGL	242	VCOM_R	260	GND
189	VDD_PFM	207	CHN1	225	VGL	243	VSSI	261	GND_AG
190	VDD_PFM	208	CHP1	226	VREGN	244	VSSI	262	GND_AG
191	DRVN	209	CHP1	227	VREGN	245	VSSA	263	GND_AG
192	DRVN	210	CHN2	228	CLN1	246	VSSA	264	NULL
193	VSN	211	CHN2	229	CLN1	247	DUMMY	265	DUMMY
194	VSN	212	CHP2	230	CLP1	248	VGH		
195	VSN	213	CHP2	231	CLP1	249	VGH		
196	VMONN	214	CHN3	232	CLP2	250	VGH		
197	VMONN	215	CHN3	233	CLP2	251	DUMMY		
198	VRNL	216	CHP3	234	CLN2	252	VGL		

4.2 Data Input Format

<Figure 2. Pixel Format>

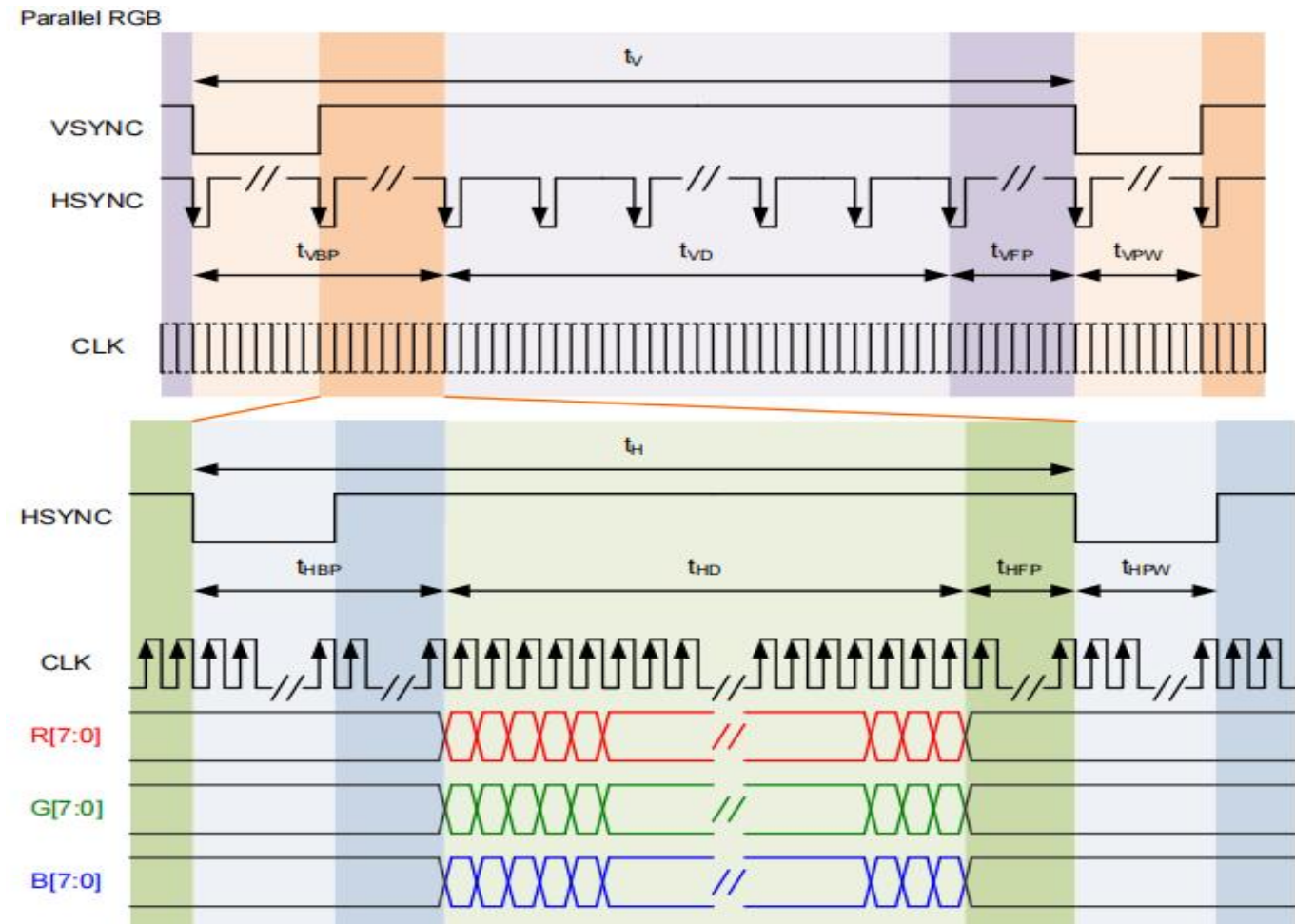


<Figure 3. Scan direction>



4.3 LVDS Interface Timing

< Figure 4. Timing Chart of Signals in LVDS Interface SYNC Mode>

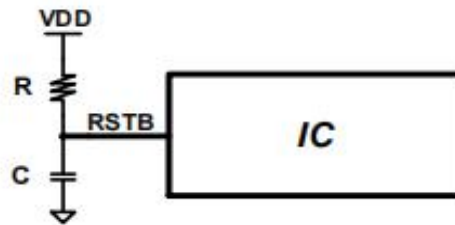


1920 x 1200(Only 2-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t _{CLK}	144.8	146.56	149.8	MHz	
Horizontal blanking time	t _{HBT}	48	50	96	t _{CLK}	t _{HBP} + t _{HFP}
Horizontal back porch	t _{HBP}	24	26	253	t _{CLK}	Include t _{HPW}
Horizontal display area	t _{HD}		1920		t _{CLK}	
Horizontal front porch	t _{HFP}	24	24	255	t _{CLK}	
Horizontal period	t _H	1968	1970	2019	t _{CLK}	
Horizontal pulse width	t _{HPW}	2	2	2	t _{CLK}	
Vertical blanking time	t _{VBT}	20	40	66	t _H	t _{VBP} + t _{VFP}
Vertical back porch	t _{VBP}	10	20	253	t _H	Include t _{VPW}
Vertical display area	t _{VD}		1200		t _H	
Vertical front porch	t _{VFP}	10	20	255	t _H	
Vertical period	t _V	1220	1240	1266	t _H	
Vertical pulse width	t _{VPW}	2	2	2	t _H	
Frame rate	FR	60	60	60	Hz	

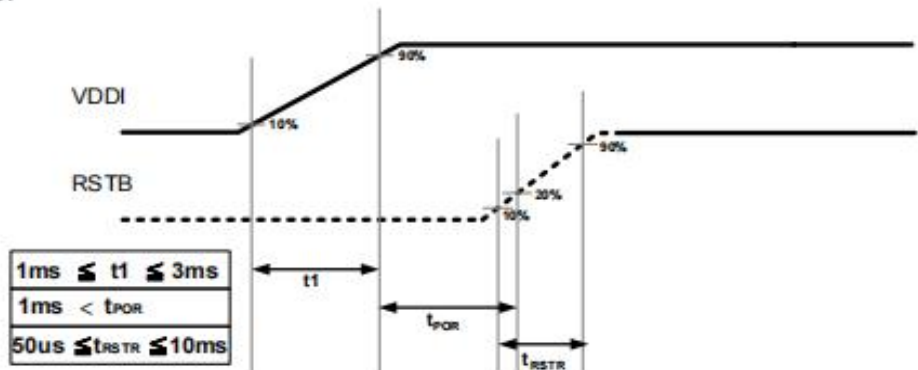
4.4 Reset Timing:

Setting RSTB pin to "L" (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset is required to initialize internal registers after VDDI is stable. Initialized by RSTB pin is essential before operating. There are two suggestions for the hardware reset connection. One is RSTB controlled by MCU. The other is connecting an external RC circuit with RSTB pin, and the recommended RC circuit is $47\text{ K}\Omega \sim 200\text{ K}\Omega + 0.47\mu\text{F}$. (For $1\text{ ms} \leq t_1 \leq 3\text{ ms}$)

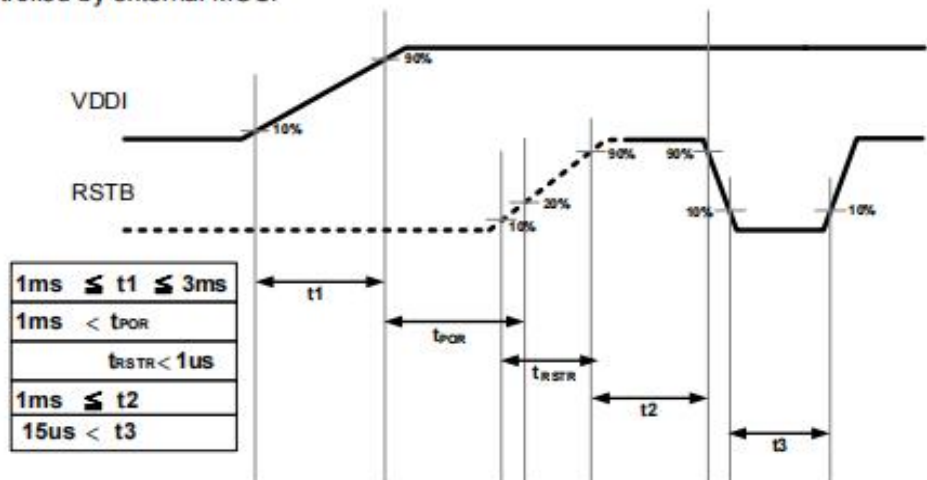


Recommend power on reset timing is shown as below.

* For RSTB pin +RC:



* For RSTB pin controlled by external MCU:



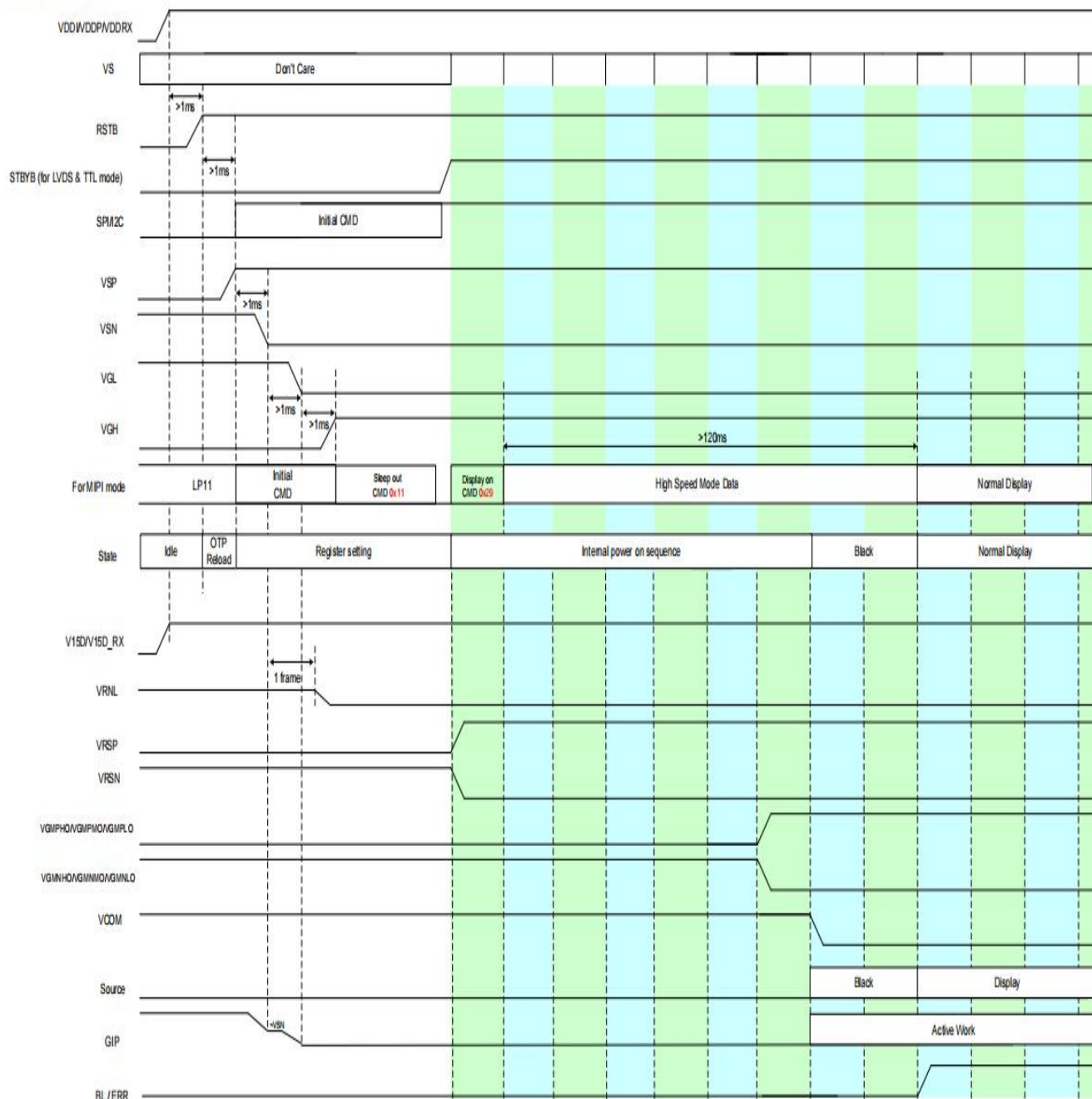
5.0 POWER SEQUENCE

5.1 Power ON/OFF Sequence

To prevent a latch-up or DC operation of the LCD TFT, the power on/off sequence shall be as shown in below.

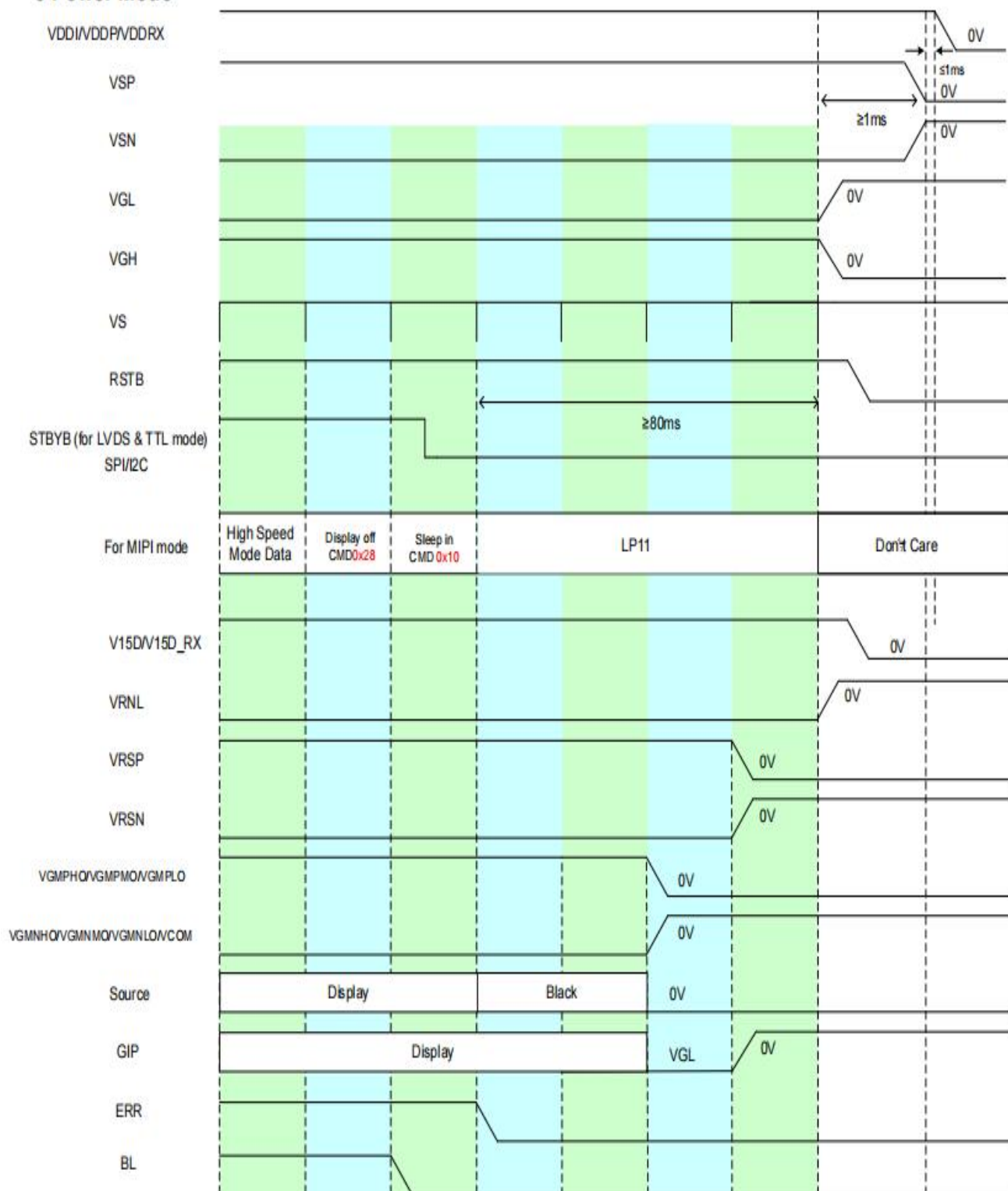
<Figure 5. Power on>

5 Power Mode



<Figure 6. Power off>

5 Power Mode



6.0 OPTICAL SPECIFICATIONS

6.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance <1lux and temperature= $25\pm 2^{\circ}\text{C}$) with the equipment of luminance meter system (Goniometer system and CS2000/CA310) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\varnothing=0$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\varnothing=90$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\varnothing=180$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\varnothing=270$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or \varnothing , the center of the measuring spot on the Display surface shall stay fixed.

The backlight should be operating for 30 minutes prior to measurement.

6.2 Optical Specifications

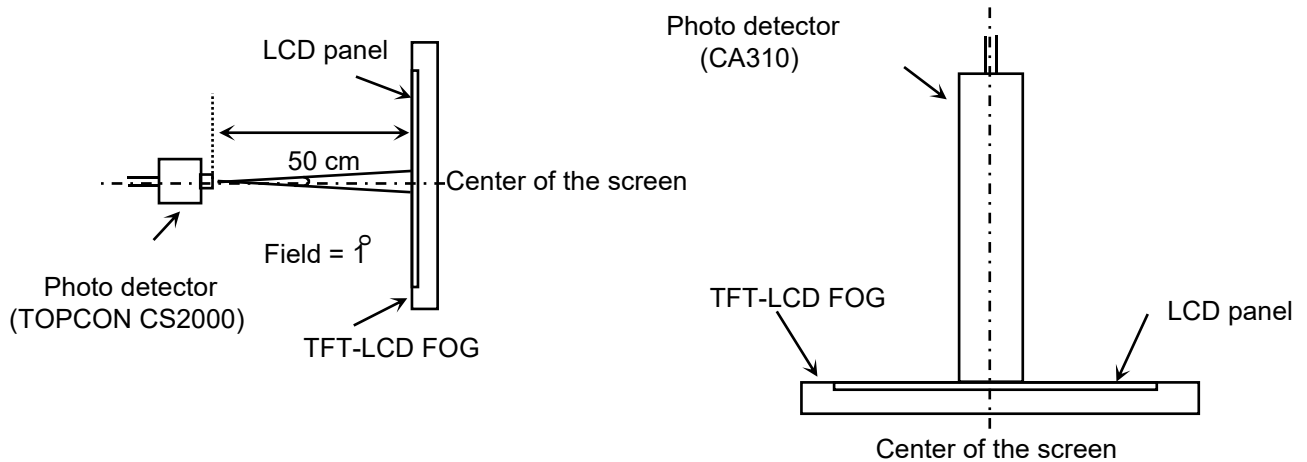
<Table 6. Optical Specifications>

[$T_a=25\pm 2^{\circ}\text{C}$]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 6.1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast Ratio		CR	$\Theta = 0^\circ$	1000	1200	-		HC+APF Note 6.2/6.3
Cell Transmittance		Tr		3.8	4.5	-	%	
Chroma@CIE1931		Rx	$\Theta = 0^\circ$	0.654	0.674	0.694		@C Light Note 6.4
		Ry		0.302	0.322	0.342		
		Gx		0.249	0.269	0.289		
		Gy		0.582	0.602	0.622		
		Bx		0.113	0.133	0.153		
		By		0.095	0.115	0.135		
		Wx		0.276	0.296	0.316		
		Wy		0.318	0.338	0.358		
Color Gamut			$\Theta = 0^\circ$	70	75	-	%	
Response Time		Tr+Tf	Ta= 25° C $\Theta = 0^\circ$	-	30	35	ms	Note 6.5

Note 6.1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

<Figure 7. Viewing Angle Range Is Defined As Follows>



View angel range, uniformity, etc. measurement setup

Flicker, measurement setup

Note 6.2: Contrast measurements shall be made at viewing angle of $\Theta=0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 6.3: Transmittance is the Value with Polarizer(HC+APF40%↑) (Film structure is on Table 7) .

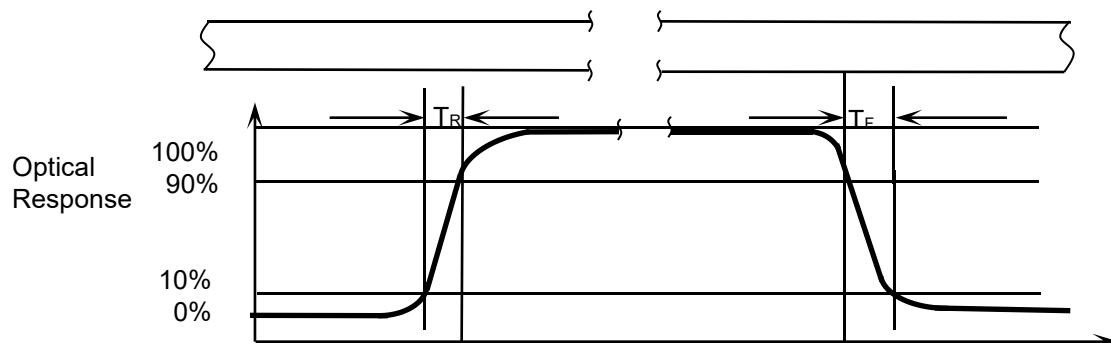
<Table 7. BLU Film structure>

遮光	Soken	SK8906B
BEF	光耀	SG43+QG42
DIF	Kimoto	38TMQ
LGP	住友	TR1801A
REF	丽光	75W28
胶铁	乐天	LB1010W
LED	AOT	3004 Silicate

Note 6.4: The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

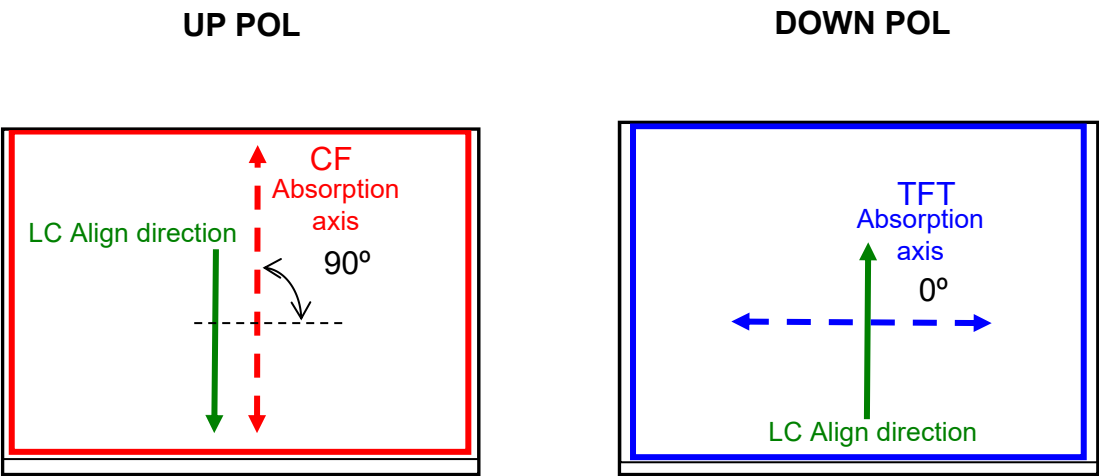
Note 6.5: The electro-optical response time measurements shall be made as Figure 8 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 8. Response Time Testing>



7.0 LC Align Direction & Pol absorption axis

<Figure 9. Graphic Description of Pol>



LC Align Direction

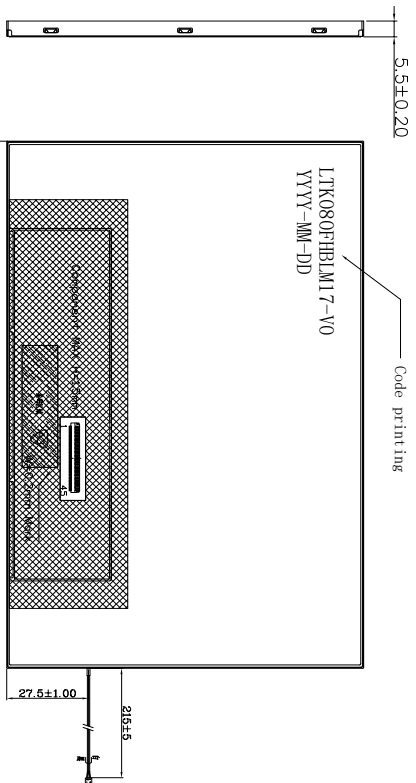
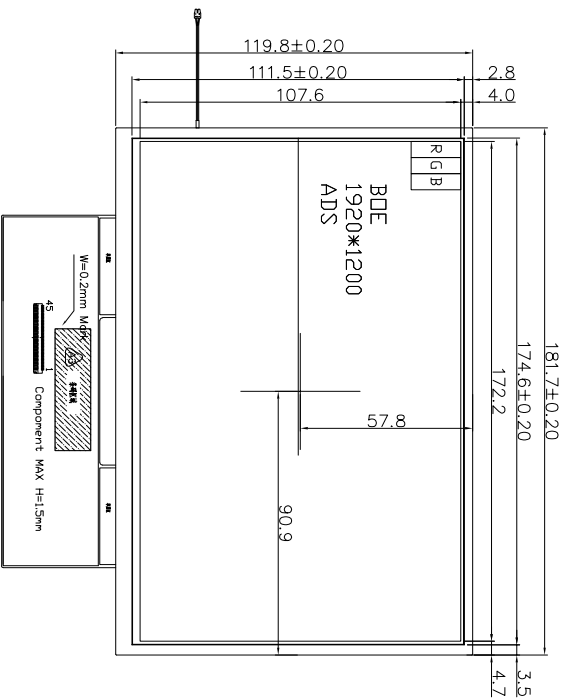
The positive LC align direction is shown in Figure 9.

POL detail

There is no Sunglass Free requirement.

Item	CF POL	TFT POL	Remark
Absorbance Axis	90°	0°	E-Mode
Material	HC+Clear	APF	-
Size (mm)	175.624*112.24	175.624*112.54	±0.15
Thickness(μm)	76	78	±0.05
Part NO	TBD	TBD	-

8.0 Outline Drawing



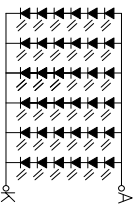
Front View

Side View

Back View



Notes:

1. Display: 8.0", TFT
 2. Resolution: 1920*RGB*1200
 3. LCD Viewing Direction: ALL
 4. LCD Driver: FL5893DA
 5. LCM Brightness: 1000cd / m² (Typ) , Uniformity $\geq 80\%$
 6. *: Critical dimension: () Reference dimension
 7. Operating Temperature: -30°C ~ +85 °C
 8. Storage Temperature: -30°C ~ +85 °C
9. Requirements on Environmental Protection: ROHS



Backlight LED Circuit

3		
2		
1		
1	NEW	
REV	DESCRIPTION	DATE NAME
		2023.07.04 Jerry

 <h1>LEADTEK COMPANY LIMITED</h1> <h2>LEADTEK DISPLAY</h2>				
SCALE: 1/	UNIT: mm	PAGE: 1/1		
Part No:	LT K080FHBLM17	VER: V00	Approve	Check
Customer No:			Ian	Jack
				Jerry

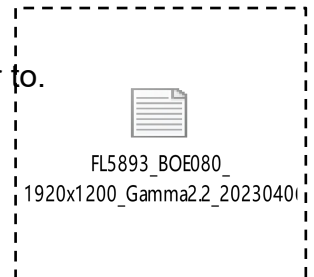
9.0 RELIABILITY

<Table 8. Reliability Test Parameters>

No	Items	Conditions	Remark
1	High Temperature Storage test(HTS)	85°C, 240hrs, Non-operational	Note 9.1
2	Low Temperature Storage test(LTS)	-30°C, 240hrs, Non-operational	
3	High Temperature Operating test(HTO)	85°C, 240hrs, operational	
4	Low Temperature Operating test(LTO)	-30°C, 240hrs, operational	
5	Thermal Humidity Operating test(THO)	60°C/90%RH, 240hrs, operational	
6	Thermal Cycle Storage test(TST)	-30~80°C, 100cycles, 1hr/cycle, Non-operational	
7	Image Sticking	5*5 Pattern, 1hr 25°C±2°C check pattern Gray 127, after 3 min, the mura must be disappeared completely	

Note 9.1:

- ①The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours.
- ②The Leadtek display reliability test is based on FL5893 IC.
- ③Other ICs can only be used after the reliability test is passed.
- ④Suitable operating time: under 12 hours a day. (Please contract Leadtek display in advance for 7*24hrs or more than suggested Operating time) Long-term lighting products recommended regular shutdown.
- ⑤Here is the Leadtek display debugging IC (FL5893) code to refer to.



10.0 PACKING

10.1 Packing Description

TBD

10.0 PACKING

10.2 Label

TBD

11.0 PRECAUTIONS

11.1 Handling

- (1) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (2) You must mount a FOG using specified mounting holes (Details refer to the drawings).
- (3) Please make sure to avoid external forces applied to the Source FPC and D-IC during the process of handling or assembling the MDL set. If not, It causes panel damage or malfunction.
- (4) Note that LCD surfaces are very fragile and could be easily damaged. Do not touch, push or rub the exposed LCD surfaces with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
- (5) Do not pull or fold the source D-IC which connect the source FPC and the panel. Do not pull or fold the LED wire.
- (6) After removing the protective film, when the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with alcohol or purified water. Do not strong polar solvent because they cause chemical damage to the LCD surface.
- (7) Wipe off saliva or water drops as soon as possible. Their long time contact with LCD surface causes deformations and color fading.
- (8) Protection film for LCD surface on the FOG shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (9) Since the LCD is made of glass, do not apply strong mechanical impact or static load onto it. Handling with care since shock, vibration, and careless handling may seriously affect the product. If it falls from a high place or receives a strong shock, the glass may be broken.
- (10) Do not disassemble the FOG.
- (11) To determine the optimum mounting angle, refer to the viewing angle range in the specification for each model.
- (12) If the customer's set presses the main parts of the LCD, the LCD may show the abnormal display. But this phenomenon does not mean the malfunction of the LCD and should be pressed by the way of mutual agreement.
- (13) Do not drop water or any chemicals onto the LCD's surface.
- (14) The ITO pad area needs special careful caution because it could be easily corroded. Do not contact the ITO pad area with HCFC, Soldering flux, Chlorine, Sulfur, saliva or fingerprint. To prevent the ITO corrosion, customers are recommended that the ITO area would be covered by UV or silicon.

11.2 Operating Precautions

- (1) Be careful for condensation at sudden temperature change. Condensation makes damage to LCD surface or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (2) FOG has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (3) The electrochemical reaction caused by DC voltage will lead to LCD degradation, so DC drive should be avoided.
- (4) The LCD FOGs use C-MOS LSI drivers, so customers are recommended that any unused input terminal would be connected to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly area, assembly equipment to protect against static electricity.
- (5) Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on) Otherwise the FOG may be damaged.
- (6) Do not connect or disconnect the cable to/ from the FOG at the "Power On" condition.
- (7) When the FOG is operating, do not lose MIPI(SPI/MCU8080), power. If any one of these inputs is lost, the LCD panel would be damaged.
- (8) Obey the supply voltage sequence. If wrong sequence is applied, the FOG would be damaged.
- (9) Do not re-adjust variable resistor or switch etc.

11.3 Electrostatic Discharge Control

- (1) Since a FOG is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Keep products as far away from static electricity as possible.
- (2) Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.

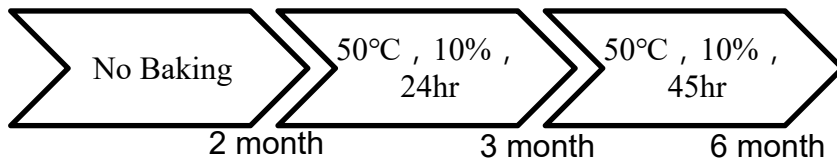
11.4 Precautions for Strong Light Exposure

Strong light exposure causes degradation of LCD surface and color filter. It is not allowed to store or run directly in strong light or in high temperature and humidity for a long time.

11.5 Storage Precautions

When storing FOGs as spares for a long time, the following precautions are necessary.

- (1) The LCD surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.
Temperature : 5 ~ 40 °C.
- (2) Humidity : 35 ~ 75 %RH/
- (3) Period : 6 months/
- (4) Control of ventilation and temperature is necessary.
- (5) Please make sure to protect the product from strong light exposure, water or moisture. Be careful for condensation.
- (6) Store in a polyethylene bag with sealed so as not to enter fresh air outside in it.
- (7) Do not store the LCD near organic solvents or corrosive gasses.
- (8) Please keep the FOGs at a circumstance shown below Fig.



11.6 Operation Condition Guide

- (1) Normal operating condition
 - Temperature: 0 ~ 40°C
 - Operating Ambient Humidity : 10 ~ 90 %
 - Display pattern: dynamic pattern (Real display)
- (2) Black image or moving image is strongly recommended as a screen save.
- (3) Lifetime in this spec. is guaranteed only when Commercial Display is used according to operating usages.
- (4) Please contact Leadtek display in advance when you display the same pattern for a long time.
- (5) If the FOG keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen. To avoid image sticking, it is recommended to use a screen saver.
- (6) Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on) Otherwise the FOG may be damaged.
- (7) Dew drop atmosphere should be avoided.
- (8) The storage room should be equipped with a good ventilation facility, which has a temperature controlling system.
- (9) When expose to drastic fluctuation of temperature (hot to cold or cold to hot) ,the LCD may be affected; Specifically, drastic temperature fluctuation from cold to hot ,produces dew on the LCD's surface which may affect the operation of the LCD surface and the LCD.

- (10) Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD may turn black at temperature above its operational range. However those phenomena do not mean malfunction or out of order with the LCD. The LCD will revert to normal operation once the temperature returns to the recommended temperature range for normal operation.

11.7 Others

- (1) When returning the TFT for repair or etc., Please pack the TFT not to be broken. We recommend to use the original shipping packages.
- (2) In order to prevent potential problems, flicker should be adjusted by optimizing the Vcom value in customer LCM Line.
- (3) (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (4) For the crash damaged or unnecessary LCD, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.
- (5) If you should swallow the liquid crystal, first, wash your mouth thoroughly with water, then drink a lot of water and induce vomiting, and then, consult a physician.
- (6) If the liquid crystal should get in your eyes, flush your eyes with running water for at least fifteen minutes.