Logos2 Series FPGA Device Data Sheet

(DS04001 , V1.6)

(2021.10.15)

revision history

Date	Revision	Description
2019.9.9	V0.1	Initial Alphab version released
2019.10.21	V0.2	Added hot-plug feature description, support hot -plug level 2 Table 5-1 LVDS performance parameters changed to TBD
2019.12.6	V0.3	1. Modify the V_{IN} signal description in Table 2-1 and Table 2-2 ; 2. Modify Table 7-7 Description of the clock interface rate of HSSTLP
2020.4.2	V1.0	1. Modify Logos2 series FPGA product overview and feature description; 2. Modify Table 1-1 and add SERDES to Table 1-2 LANE description; 3. Update the description of Figure 1-1 ; 4. Remove VCCA_IO in 3.1 power-on sequence 5. Modify AC characteristic parameters; 6. In the document, HSST is changed to HSSTLP , and HSSTLP related data is modified;
2020.5.12	V1.1	1. Revised Table 2-1 and Table 2-2 **V_{IN}** maximum and minimum; 2. Modify Table 2-3 data for n and r ; 3. Modify the typical values in Table 2-5 , and add notes 4. Modify Table 2-8 HBM_IO value is ±800 ; 5. Increase eFUSE programming conditions; 6. Modify Table 3-3 Voh value of SSTL18D_I and SSTL18D_II ; 7. Modify the performance parameters in Table 4-11 ; 8. Added Table 4-12 IOB AC characteristics; 9. Modify Table 6-1 AC characteristic parameters; 10. Add Table 8-1 PCIe hard core features;
2020.6.12	V1.2	1. Added CTC abbreviation description; 2. Modify 1.3.6 Clock resource description; 3. Tables 4-4 and 4-5 add input clock jitter data and modify output clock jitter data; 4. Table 2-8 ESD , Latch-Up indicators, the description of HBM_IO refers to all IO including power supply, delete the general IO in the description ; 5. Modify table 4-7 , table 4-8 maximum frequency; 6. Modify Table 4-11 AC characteristics of each download mode ; 7. Modify the minimum value of each characteristic of sinusoidal jitter tolerance in Table 7-9 ;
2020.6.22	V1.3	Modify Table 6-1 ADC Hard Core Features
2020.6.28	V1.4	Modify Table 4-4 and Table 4-5 Input Clock Duty Cycle
2020.11.10	V1.5	1. Added -5 speed grade stats 2. Added description -5 does not support temperature sensor function 3. Table 2-8 HBM_IO value changed to ±1000 4. Added I/O secondary hot plug does not support dedicated I/O and multiplexed I/O instructions
2021.10.15	V1.6	1. Added device information of PG2L25H and PG2L50H in Table 1-1 and Table 1-2 2. Added static power consumption data of PG2L25H and PG2L50H in Table 2-5 3. the relevant data of PG2L25H and PG2L50H in Table 4-10

Logos2 series FPGA devices , product model and resource scale list, AC & DC characteristics, etc. of Shenzhen Ziguang Tongchuang Electronics Co., Ltd. (hereinafter referred to as Ziguang Tongchuang) . Users can learn about Logos2 series FPGA devices through this article. features, which facilitates device selection.

1. Logos2 Series FPGA Overview

Logos2 series programmable logic devices are the second generation of new high-cost, low-power FPGA products of the Logos family launched by Shenzhen Ziguang Tongchuang Electronics Co., Ltd. It adopts the mainstream 28nm process. Logos2 series FPGAs include configurable logic module (CLM), dedicated 36Kb memory unit (DRM), arithmetic processing unit (APM), multi-functional high-performance IO, and rich on-chip clock resources, and integrates analog-to-digital conversion modules (ADC) and other hard core resources, support multiple configuration modes, and provide functions such as bit stream encryption and authentication, device ID (UID) to protect user design security. Based on the above characteristics, Logos2 series FPGA can be widely used in video, industrial control, automotive electronics, communication, computer, medical, LED display security monitoring, instrumentation, military and consumer electronics and other application fields.

1.1. Logos2 series FPGA product features

- Cost-effective, low power consumption
- Mature 28nm CMOS process
- Core voltage as low as 1.0V[1]

➢ **Support a variety of standard IO**

- Up to 500 user IOs supporting 1.2 V to 3.3V IO standards
- Support HSTL, SSTL storage interface standards
- Support differential standards such as LVDS, MINI LVDS, TMDS (applied to HDMI, DVI interface)
- Programmable IO BUFFER High-performance IO LOGIC
- Supports hot-pluggable level 2

➢ **Flexible programmable logic module CLM**

- LUT 6 logical structure
- Each CLM contains 4 multifunction LUTs 6, 8 registers
- Supports fast arithmetic carry logic
- Support for distributed RAM mode
- Support cascading chain

➢ **Supports DRM with multiple read and write modes**

- A single DRM provides 36Kb of memory, configurable as 2 independent 18Kb memory blocks
- Support a variety of working modes, including single port (SP)RAM , dual port (DP RAM) , simple dual port (SDP) RAM, ROM and FIFO mode
- Dual-port RAM and simple dual-port RAM support dual-port mixed data width
- Support ECC function
- Support Normal Write Transparent Write and Read before Write three write modes
- Support Byte Write function
- Optional address latches, output registers

➢ **Efficient Arithmetic Processing Unit APM**

- Each APM supports 1 25*18 operation or 2 12*9 operations
- Support input and output registers
- Support 48bit addition
- Support for signed data operations

➢ **Integrated ADC hard core**

- 12bit resolution, 1MSPS (independent ADC dual core) sampling rate
- Up to 17 input channels
- Integrated temperature sensor (-5 not supported)

➢ **Rich clock resources**

- Supports Class 3 clock network for flexible configuration
- Support global clock (GLOBAL CLOCK) network
- Support for REGIONAL CLOCK network
- Support I/O clock (I/O CLOCK) network
- Integrated Multiple PLLs Each PLL supports up to 5 clock outputs

➢ **Flexible configuration**

- Supports multiple programming modes
- JTAG mode conforms to IEEE 1149.1, IEEE1149.6 standards
- Master SPI can choose up to 8bit data width, effectively improve programming speed
- Support Slave Serial, Slave Parallel mode
- Support AES256 GCM bit stream encryption, support 96bit UID protection
- Support digital signature authentication for bitstream files
- Support for eFuse key storage
- Supports battery-backed RAM BB RAM key storage for chip-level security
- Support disable bitstream readback
- Supports JTAG security management
- Support anti-DPA attack
- Support SEU error detection and correction
- Support multi-version bitstream fallback function
- Support watchdog timeout detection
- Support programming download tool Fabric Configuration
- Support online debugging tool Fabric Debugger

➢ **High-performance high-speed serial transceiver HSSTLP**

- Supports Data Rates up to 6.6 Gbps
- Flexible configurable PCS, can support PCIe GEN1 GEN2, Gigabit Ethernet, XAUI, Gige and other protocols

Note: DR version supports VCC 0.9v

1.2. Logos2 series FPGA resource scale and packaging information

Logos2 series FPGA resource scale and package information are shown in Table 1-1 and Table 1-2

Table 1-1 Logos2 Number of FPGA resources

Resource name		PG2L25H	PG2L50H	PG2L100H
CLM	LUT6	17800	33400	66600
	Equivalent LUT4	26700	50100	99900
	FF	35600	66800	133200
	Distributed ram (Kb)	343	687	1273
DRM (36Kbits/ pc)		55	85	155
APM(units)		80	120	240
PLLs	GPLLs	3	5	6
	PPLLs	3	5	6
ADC （dual core ）	Dedicated analog channel (differential input pair)	1	1	1
	Multiplexed analog channels (differential input pair)	11	16	16
SERDES LANE (1)		4	4	8
PCIE GEN2×4 CORE		1	1	1

Notes: 1. 4 LANEs form a HSSTLP

Table 1-2 Logos2 FPGA package information and user IO quantity

Device / Package information	PG2L25H		PG2L50H		PG2L100H	
	SERDES LANE	I/O	SERDES LANE	I/O	SERDES LANE	I/O
FBG676 （ 27mm×27mm， 1.0mm ）					8	300
FBG484 （ 23mm×23mm， 1.0mm ）			4	250	4	285
MBG325 （ 15mm×15mm， 0.8mm ）	4	150				
MBG324 （ 15mm×15mm， 0.8mm ）					0	210
FBG256 （ 17mm×17mm， 1.0mm ）					0	170

1.3. Logos2 series FPGA brief description

1.3.1. CLM

CLM (Configurable Logic Module, Configurable Logic Module) is the basic logic unit of Logos2 series products. It is mainly composed of multi-function LUT6, registers and extended function selectors. CLM has two forms, CLMA and CLMS, in Logos2 series products. Both CLMA and CLMS support logic function, arithmetic function, shift register function and ROM function, only CLMS supports distributed RAM function.

The main functional features of CLM are as follows:

- Adopt innovative LUT6 logic structure

- Each CLM contains 4 multi-function LUT6
- Each CLM contains 8 registers
- Support arithmetic function mode
- Support fast arithmetic carry logic
- Efficient realization of multiplexing function
- Can realize ROM function
- Support distributed RAM mode
- Support cascading chain

For detailed CLM features and usage methods, please refer to "UG040001_Logos2 Series FPGA Configurable Logic Module (CLM) User Guide".

1.3.2. DRM

A single DRM has 36K bits storage unit, supports multiple operating modes, supports configurable data bit width, and supports dual-port mixed data bit width in DP RAM and SDP RAM modes. The main features of DRM are as follows:

- DRM storage capacity can be independently configured with two 18K or one 36K.
- The port data bit width of DP RAM is as high as 36bit, and its two ports are completely independent except for sharing the RAM content, and support different clock domains.
- The port data bit width of SDP RAM is as high as 72bit, and its two ports also support different clock domains, but one of its ports is limited to write operations, and the other port is limited to read operations.
- In ROM mode, the content of DRM is usually initialized during the process of downloading configuration data. Of course, other modes can also utilize programming configuration to initialize the content of the DRM. The port data bit width of ROM is up to 72bits.
- In synchronous or asynchronous FIFO mode, one port is dedicated to FIFO data writing, the other port is dedicated to FIFO data reading, and the read and write ports can use different clocks.
- Supports 64-bits ECC in 36K memory mode, and supports user insertion errors.

For detailed DRM features and usage methods, please refer to "UG040002_Logos2 Series FPGA Dedicated RAM Module (DRM) User Guide".

1.3.3. APM

Each APM consists of I/O Unit, Preadder, Mult and Postadder functional units, supporting each level of register pipeline. Each APM can implement one 25*18 multiplier or two 12*9 multipliers, support pre-add

function; support signed operation; can realize 1 48bit or 2 24bit add/subtract/accumulate operations. The APMs of Logos2 FPGAs support cascading, enabling filter and high-bit-width multiplier applications. The main features of APM are as follows:

- Signed multiplier 25*18; unsigned multiplication assigns 0 through high bits accomplish
- All calculations and output results are signed numbers, including the sign bit
- Support 1 48bits _ Add / Subtract / Accumulate or 2 24bits operations
- Pre-add for 25bits
- Standalone optional CE and RST
- Support input cascade
- Support output cascade
- Control / Data Signal Pipelining
- Support dynamic mode switching
- Support Rounding Function

For detailed APM features and usage methods, please refer to "UG040003_Logos2 Series FPGA Arithmetic Processing Module (APM) User Guide".

1.3.4. Input/Output

IOB

The IO of Logos2 FPGA is distributed according to Bank, and each Bank is powered by an independent IO power supply. The IO is flexible and configurable, supporting 1.2V~3.3V power supply voltage and different single-ended and differential interface standards to adapt to different application scenarios. All user IOs are bidirectional, including IBUF, OBUF and tri-state control TBUF. The IOB of Logos2 FPGA is powerful and can flexibly configure the interface standard, output drive strength, Slew Rate, input hysteresis, etc. For detailed IO features and usage methods, please refer to the Logos2 Series FPGA Input Output Interface (IO) User Guide.

IOL

The IOL module is located between the IOB and the Core, and manages the signals to be input to and output from the FPGA Core.

IOL supports various high-speed interfaces. In addition to supporting data direct input and output and IO register input and output modes, it also supports the following functions:

- ISERDES : For high-speed interfaces, input Deserializers such as 1:2; 1:4; 1:7; 1:8 are supported..
- OSERDES : For high-speed interfaces, support 2:1; 4:1; 7:1; 8:1, etc. output Serializer.
- Built-in IO delay function, you can adjust the input / output delay dynamically / statically.

Built-in input FIFO , mainly used to complete non-continuous DQS from external (for DDR

memory interface) to the clock domain conversion of the internal continuous clock and the skew compensation of the sampling clock and the internal clock in some special Generic DDR applications.

For detailed IO features and usage methods, please refer to "UG040006 Logos2 Series FPGA Input Output Interface (IO) User Guide".

1.3.5. ADC

Each Logos2 FPGA integrates an analog-to-digital converter (ADC) with a resolution of 12bit and a sampling rate of 1MSPS. Each ADC has 17 pairs of differential Channels, of which 16 pairs of Analog Input are multiplexed with GPIO, and the other pair uses dedicated analog input pins. The scanning method of the 17 pairs of Channels is completely controlled by the FPGA flexibly, and the user can decide through the User Logic to finally share the ADC sampling rate of 1MSPS with several pairs of Channels.

The ADC provides on-chip voltage and temperature monitoring functions. VCC, VCCA, VCC_DRM can be detected; see Table 6-1 for detailed characteristic parameters. For detailed use of ADC, please refer to "UG040009 Logos2 Series FPGA Analog-to-Digital Conversion Module (ADC) User Guide".

1.3.6. Clock

Logos2 series products include three types of clocks, namely Global Clock , Region Clock and I / O Clock . The global clock provides the clock for the synchronous logic units of each node of the chip. The global clock can be used as a synchronous clock for synchronous logic units in different clock regions. Regional clocks provide clocks to synchronous logic cells within a single clock region to which they belong. Two clock regions adjacent to the top and bottom can be driven synchronously. The I/O Clock provides a synchronous clock for I/O high-speed data.

In order to meet the user's needs for frequency change and phase adjustment, Logos2 series products also provide rich PLL resources, GPLL provides more frequency division and functions than PPLL, and PPLL can provide clock for DDR , etc. The overall clock resources of the PG2L100H are as follows:

- The chip has 32 GLOBAL CLOCK, the upper and lower parts of the chip each have 16 GLOBAL CLOCK .
- The chip has 96 HORIZONTAL CLOCK , each REGION 12 in HORIZONTAL _ CLOCK .

For the detailed characteristics and usage of the clock, please refer to " UG040004 Logos2 Series FPGA Clock Resources (Clock) User Guide".

1.3.7. Configuration

Configuration is the process of programming the FPGA . Logos2 FPGA uses SRAM cells to store configuration data, which needs to be reconfigured after each power-on; configuration data can be actively obtained by the chip from external flash , or downloaded to the chip through an external processor / controller.

Logos2 FPGA supports multiple configuration modes, including JTAG mode, Master SPI mode ,

Slave Parallel mode, Slave Serial mode. The configuration-related functions of Logos2 FPGA are as follows:

- JTAG mode, IEEE compliant 1149.1 , IEEE 1149.6 Standard
- Master SPI mode, support data bit width 1/2/4/8bit
- Slave Parallel mode, support data bit width 8/16/32bit
- Slave Serial mode
- Support configuration data stream compression, which can effectively reduce bit Stream size, saving storage space and programming time
- Configure data stream encryption to prevent malicious plagiarism and effectively protect customer design intellectual property
- SHA-3 support Digest, RSA-2048 Certified, AES256-GCM Self-authentication digitally signs the bitstream
- Key storage methods support eFuse and battery -backed RAM (BB-RAM) key storage, where BB-RAM provides chip-level security
- Supports security protection technology that prevents reverse bit stream reading
- JTAG support Safe management to permanently turn off JTAG Function
- Support anti- DPA Attacks to prevent encryption keys from being cracked by hackers
- Support SEU 1bit error correction and 2bit error detection
- Support watchdog timeout detection function
- In the main SPI In mode, support configuration bit stream version fallback function
- Support UID Function

For the detailed features and usage of the configuration, please refer to " UG040005 Logos2 Series FPGA Configuration User Guide .

1.3.8. High Speed Serial Transceiver HSSTLP

HSSTLP is a high-speed serial interface module built into Logos2 series products with a Data Rate of up to 6.6Gbps . In addition to PMA , HSSTLP integrates rich PCS functions, which can be flexibly applied to various serial protocol standards. Each HSSTLP supports one to four full-duplex transceiver lanes . The main features of HSSTLP include:

- Support DataRate rate: 0.6Gbps- 6.6Gbps
- Flexible reference clock selection
- Transmit channel and receive channel data rates are independently configurable
- Programmable output swing and de-emphasis
- Receiver Adaptive Linear Equalizer

- PMA Rx supports SSC
- Data channel supports data bit width: 8bit only , 10bit only , 8b10b, 16bit only , 20bit only , 32bit only , 40bit only, 64b66b/64b67b and other modes
- Flexibly configurable PCS to support PCI Express GEN1, PCI Express GEN2, XAUI, Gigabit Ethernet , CPRI, SRIO and other protocols
- Flexible Word Alignment function
- Support RxClock Slip function to ensure fixed Receive Latency
- Support protocol standard 8b10b encoding and decoding
- Support protocol standard 64b66b/64b67b data adaptation function
- Flexible CTC Solutions
- Channels that support x2 and x4 Bonding
- HSSTLP supports dynamic modification
- Near-end loopback and far-end loopback modes
- Built-in PRBS function
- Adaptive EQ

For detailed features and usage of HSSTLP, please refer to "Logos2 Series FPGA High-Speed Serial Transceiver (HSSTLP) User Guide"

1.4. Logos2 series FPGA reference materials

Section 1.3 briefly describes each module of Logos2 FPGA, as well as the clock and configuration system. For detailed information about the corresponding modules, please refer to the relevant user guide documents of Logos2 FPGA, as shown in the following table.

Table 1-3 Logos2 Column FPGA User Guide Documentation

Document number	File name	Document content
UG040001	Logos2 Series FPGA Configurable Logic Module (CLM) User Guide	Logos2 series FPGA configurable logic module function description
UG040002	Logos2 Series FPGA Dedicated RAM Module (DRM) User Guide	Logos2 series FPGA dedicated RAM module function description
UG040003	Logos2 Series FPGA Arithmetic Processing Module (APM) User Guide	Logos2 series FPGA arithmetic processing module function description
UG040004	Logos2 Series FPGA Clock Resources (Clock) User Guide	Logos2 series FPGA clock resources, including PLL functions with usage description
UG040005	Logos2 Series FPGA Configuration (configuration) User Guide	Logos2 series FPGA configuration interface, configuration mode, configuration description of process etc.
UG040006	Logos2 Series FPGA Input Output Interface (IO) User Guide	Logos2 series FPGA input and output interface function description

UG040007	Logos2 Series Product GTP User Guide	Logos2 series FPGA GTP function description and usage guide
UG040008	Logos2 Series FPGA High Speed Serial Transceiver (HSSTLP) User Guide	Logos2 series FPGA high-speed serial transceivers (HSSTLP) functional description
UG040009	Logos2 Series FPGA Analog-to-Digital Conversion Module (ADC) User Guide	Logos series FPGA analog-to-digital converter function description

1.5. Logos2 Series FPGA Ordering Information

The serial number content and meaning of the Logos2 series FPGA product model are shown in Figure 1 .

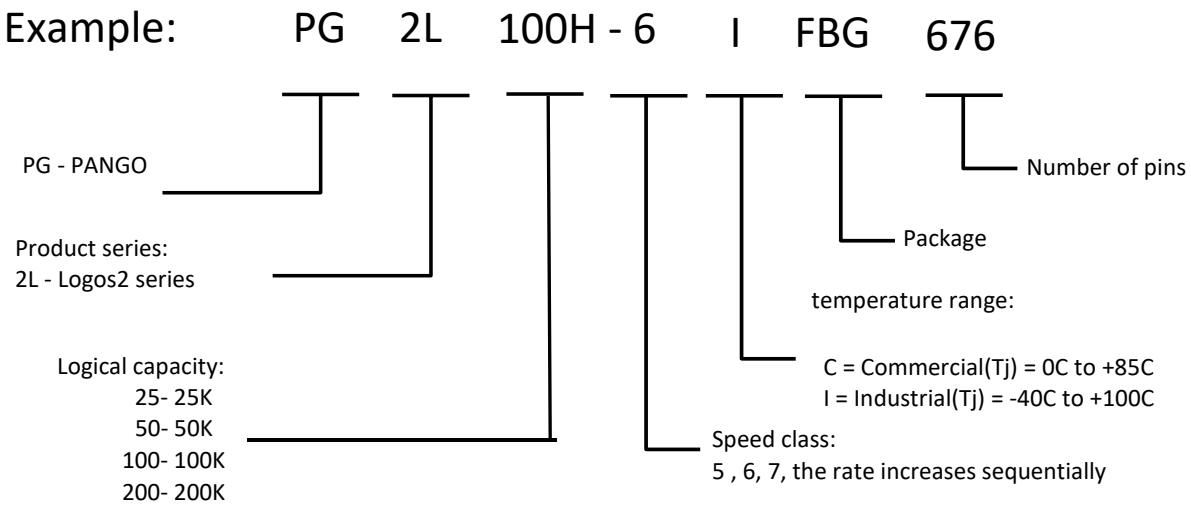

Figure 1-1 The content and meaning of the serial number of the Logos2 series FPGA product model

2. Working conditions

2.1. Device Absolute Maximum Voltage

Table 2-1 Device Maximum Absolute Voltage Values

Name	Minimum	Maximum value	Unit	Description
V_{REF}	- 0.5	2.0	V	Input reference voltage
V_{CCB}	- 0.5	2.0	V	Key memory backup battery power supply voltage
V_{CC}	- 0.5	1.1	V	Core logic power supply voltage
V_{CCA}	- 0.5	2.0	V	Auxiliary power supply voltage
V_{CCIO}	- 0.5	3.6	V	Supply voltage of the output driver power supply
V_{CC_DRM}	- 0.5	1.1	V	DRM power supply voltage
V_{IN}	- 0.3	V_{CCIO} +0.45	V	I/O Input voltage
	- 0.3	2.525	V	When V_{CCIO} is 3.3V, V_{REF} or I/O input voltage of differential I/O standard, except TMDS_33 standard

Note: Exceeding the above limit ratings may cause permanent damage to the device.

2.2. Device Recommended Operating Conditions

Table 2-2 Recommended working conditions

Name	Minimum	Typical value	Maximum value	Unit	Description
V_{CCB}	1.0	- -	1.89	V	Key memory backup battery power supply voltage
V_{CC}	0.95	1.0	1.05	V	Core supply voltage
V_{CCA}	1.71	1.8	1.89	V	Auxiliary power supply voltage
V_{CCIO}	1.14	- -	3.465	V	Supply voltage of the output driver power supply
V_{CC_DRM}	0.95	1.0	1.05	V	DRM power supply voltage
V_{IN}	- 0.2	- -	V_{CCIO} +0.2	V	I/O Input voltage
	- 0.2	- -	2.5	V	When V_{CCIO} is 3.3V, V_{REF} or I/O input voltage of differential I/O standard, except TMDS_33 standard
I_{IN}	- -	- -	10	mA	The maximum current allowed to flow through the forward-biased clamp diode of any PIN in a powered or unpowered Bank

Note: Recommended working voltage is within ±5% deviation from typical working voltage.

2.3. DC Characteristics at Recommended Device Operating Conditions

Table 2-3 DC characteristics under recommended operating conditions

Name	Minimum	Typical value	Maximum value	Description
V_{DRVCC}	0.75V	- -	- -	V_{CC} The configuration data hold voltage
V_{DRVCCA}	1.5V	- -	- -	V_{CCA} The configuration data hold voltage
I_L	-	- -	15uA	pin input or output leakage current
I_{REF}	-	- -	15uA	VREF _ pin leakage current
I_{PU}	90uA	- -	330uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=3.3V)
	68uA	- -	250uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=2.5V)
	34uA	- -	220uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=1.8V)
	23uA	- -	150uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=1.5V)
	12uA	- -	120uA	PAD pull-up current (V_{IN}=0 ; V_{CCIO}=1.2V)
I_{PD}	68uA	- -	330uA	PAD pull-down current (V_{IN}=3.3V)
	45uA	- -	180uA	PAD pull-down current (V_{IN}=1.8V)
I_{CCADC}	- -	- -	25mA	Analog circuit power-up state, ADC The current of the analog power supply
I_{VCCB}	-	- -	150nA	V_{CCB} supply current
R_{INTERM}	28Ω	40Ω	55Ω	Thevenin equivalent resistance of the programmable input terminal at VCCIO/2 voltage. (when set to 40Ω)
	35Ω	50Ω	65Ω	Thevenin equivalent resistance of the programmable input terminal at VCCIO/2 voltage. (when set to 50Ω)
	44Ω	60Ω	83Ω	Thevenin equivalent resistance of the programmable input terminal at VCCIO/2 voltage. (when set to 60Ω)
C_{IN}	-	- -	TBD	Die PAD input capacitance of the terminal
n	-	0.9988	- -	Ideality Factor for Temperature Diodes
r	-	2.5Ω	- -	Serial Resistance of Temperature Diodes

Note: Typical value refers to normal pressure, 25 ℃

2.4. Maximum allowable overshoot and undershoot voltage at VIN

Table 2-4 Maximum allowable overshoot and undershoot voltage at VIN

Overshoot Voltage (V)	%UI (-40 ℃ ~125 ℃)	Undershoot Voltage (V)	%UI (-40 ℃ ~125 ℃)
VCCIO+ 0.45	100	- 0.3	100
		- 0.35	55.5
		- 0.4	23.2
		- 0.45	9.9
VCCIO+ 0.5	42	- 0.5	4.3
VCCIO+ 0.55	19.08	- 0.55	1.89
VCCIO+ 0.6	8.77	- 0.60	0.84
VCCIO+ 0.65	4.1	- 0.65	0.387
VCCIO+ 0.7	1.9	- 0.7	0.18
VCCIO+ 0.75	0.918	- 0.75	0.08
VCCIO+ 0.80	0.44	- 0.8	0.04

VCCIO+ 0.85	0.21	- 0.85	0.017

2.5. Typical quiescent current

Table 2-5 Typical quiescent current

Name	Device	Typical value	Unit	Description
I_{CCQ}	PG2L25H	75.6	mA	V_{CC} quiescent current
	PG2L50H	125		
	PG2L100H	500		
I_{CC_DRMQ}	PG2L25H	1.71	mA	V_{CC_DRM} quiescent current
	PG2L50H	2.64		
	PG2L100H	11		
I_{CCIOQ}	PG2L25H	1.94	mA	V_{CCIO} quiescent current
	PG2L50H	3.23		
	PG2L100H	18		
I_{CCAQ}	PG2L25H	20.2	mA	V_{CCA} quiescent current
	PG2L50H	32.9		
	PG2L100H	120		

Notes: 1. Typical values refer to constant voltage, 85 °C junction temperature and all single-ended I/Os ; blank configuration devices with no output current load, no input pull-up resistors, all I/Os in tri-state and floating

2. For static power consumption evaluation under other specific conditions, please use the Pango integrated in the PDS Power Planner (PPP) tool.

2.6. Power up ramp-up time

Table 2-6 Power up ramp-up time

Name	Minimum	Maximum	Unit	Description
T_{VCC}	0.2	50	ms	V_{CC} from GND Rise to 90% V_{CC} time
T_{VCC_DRM}	0.2	50	ms	V_{CC_DRM} from GND Rise to 90% V_{CC_DRM} time
T_{VCCIO}	0.2	50	ms	V_{CCIO} from GND Rise to 90% V_{CCIO} time
T_{VCCA}	0.2	50	ms	V_{CCA} from GND Rise to 90% V_{CCA} time
$T_{VCCIO2VCCA}$	-	100	ms	V_{CCIO} - V_{CCA} >2V time

2.7. Minimum current required to start

Table 2-7 Minimum current required to start

Name	Maximum value	Unit	Description
I_{CCMIN}	I_{CCQ} +150	mA	V_{CC} Minimum current for power-up
I_{CC_DRMMIN}	I_{CC_DRMQ} +70	mA	V_{CC_DRM} Minimum current for power-up
$I_{CCIOMIN}$	I_{CCIOQ} +50	mA	V_{CCIO} Minimum current at power-up (per bank)
I_{CCAMIN}	I_{CCAQ} +40	mA	V_{CCA} Minimum current for power-up

2.8. ESD (HBM , CDM), Latch Up indicator

Table 2-8 ESD , Latch-Up indicators

Name	Value	Unit	Description
HBM_IO	±1000	V	Human Body Model (HBM)
HBM_SERDES	±1000	V	HBM , Serdes
CDM_IO	±350	V	Charge Device Model (CDM) , general IO
CDM_SERDES	±300	V	CDM , serdes , Logos2 100K and below devices

	±250	V	CDM,SERDES,Logos2 100k above devices
Latch- up	±100	mA	Current injection method

2.9. eFUSE programming conditions

Table 2-9 eFUSE programming conditions

Name	Minimum	Maximum value	Unit	Description
I_{eFUSE}		188	mA	V_{CCA} supplied current
T_j	15	125	° C	

3. DC characteristics under typical operating conditions

3.1. Power-on and power-off requirements

- In the case that VCCIO is powered on before VCCA, it must satisfy (VCCIO-VCCA)>2V for less than 100ms..
- Recommended power-on sequence: V_{CC}-> V_{CC_DRM}-> V_{CCA}-> V_{CCIO}, the power-on current is the smallest at this time.
- The recommended power-off sequence is the reverse of the power-on sequence.
- Except for dedicated I/O and multiplexed I/O , all other I/Os support secondary hot swap .

3.2. IO input and output DC

The standard input and output voltage ranges of each single-ended IO level are as follows:

Table 3-1 Single-ended IO level standard input and output voltage range

Standard	VIL		VIH		V_{OL} _ Max (v)	V_{OH} Min (v)	I_{OL} (mA)	I_{OH} (mA)
	Min(V)	Max(v)	Min(v)	Max(v)				
PCI33	- 0.3	0.3VCCIO	0. 5VCCIO	VCCIO+0.5	0.1VCCIO	0.9VCCIO	1.5	- 0.5
LVCMOS33	- 0.3	0.8	2.0	3.465	0.4	VCCIO- 0.4	4 8 12 16	- 4 - 8 - 12 - 16
LVTTL33	- 0.3	0.8	2.0	3.465	0.4	2.4	4 8 12 16 24	- 4 - 8 - 12 - 16 - 24
LVCMOS25	- 0.3	0.7	1.7	VCCIO+0.3	0.4	VCCIO- 0.4	4 8 12 16	- 4 - 8 - 12 - 16
LVCMOS18	- 0.3	0.35VCCIO	0.65VCCIO	VCCIO+0.3	0.4	VCCIO- 0.4	4 8 12 16 24	- 4 - 8 - 12 - 16 - 24
LVCMOS15	- 0.3	0.35VCCIO	0.65VCCIO	VCCIO+0.3	0.4	VCCIO- 0.4	4 8 12 16	- 4 - 8 12 16
LVCMOS12	- 0.3	0.35VCCIO	0.65VCCIO	VCCIO+0.3	0.4	VCCIO- 0.4	4 8 12	- 4 - 8 - 12
SSTL18_I	- 0.3	Vref - 0.125	Vref+0.125	VCCIO+0.3	0.5VCCIO- 0.47	0.5VCCIO+0.47	8	- 8

SSTL18_II	- 0.3	Vref - 0.125	Vref+0.125	VCCIO+0.3	0.5VCCIO- 0.6	0.5VCCIO+0.6	13.4	- 13.4
SSTL15_I	- 0.3	Vref- 0.10	Vref+0.10	VCCIO+0.3	0.5VCCIO- 0.175	0.5VCCIO+0.175	8.9	- 8.9
SSTL15_II	- 0.3	Vref- 0.10	Vref+0.10	VCCIO+0.3	0.5VCCIO- 0.175	0.5VCCIO+0.175	13	- 13
HSUL12	- 0.3	Vref- 0.13	Vref+0.13	VCCIO+0.3	0.2VCCIO	0.8VCCIO	0.1	- 0.1
HSTL18_I	- 0.3	Vref- 0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO - 0.40	8	- 8
HSTL18_II	- 0.3	Vref- 0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO - 0.40	16	- 16
HSTL15_I	- 0.3	Vref- 0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO - 0.40	8	- 8
HSTL15_II	- 0.3	Vref- 0.1	Vref+0.1	VCCIO+0.3	0.40	VCCIO - 0.40	16	- 16
SSTL135_I	- 0.3	Vref- 0.1	Vref+0.1	VCCIO+0.3	0.5VCCIO- 0.15	0.5VCCIO+0.15	8.9	- 8.9
SSTL135_II	- 0.3	Vref- 0.1	Vref+0.1	VCCIO+0.3	0.5VCCIO- 0.15	0.5VCCIO+0.15	13	- 13
LPDDR	- 0.3	0.2VCCIO	0.8VCCIO	VCCIO+0.3	0.1VCCIO	0.9VCCIO	0.1	- 0.1

The standard input and output voltage ranges of differential IO levels are shown in Table 3-2

Table 3-2 Parameter requirements for differential input and output standards

I/O Standard	Vicm(V)			Vid(V)			Vocm(V)			Vod(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVDS	1	1.2	1.425	0.1	0.35	0.6	1	1.25	1.425	0.25	0.35	0.6
BLVDS	0.3	1.2	1.425	0.1	–	–	–	1.25	–	–		
MINI_LVDS	0.3	1.2	VCCA_IO	0.2	0.4	0.6	1	1.2	1.4	0.3	0.40	0.6
PPDS	0.2	0.9	VCCA_IO	0.1	0.25	0.4	0.5	1.0	1.4	0.1	0.3	0.45
RSDS	0.3	0.9	1.5	0.1	0.35	0.6	1	1.2	1.4	0.1	0.35	0.6
TMDS	2.7	2.965	3.23	0.15	0.675	1.2	VCCIO-0.405	VCCIO- 0.3	VCCIO - 0.19	0.4	0.6	0.8

Table 3-3 Parameter requirements for differential-like input and output standards

IO standard	Vid(V)	Vicm（V）			Vol(V)	Voh(V)	Iol（mA）	Ioh（mA）
	min	min	typ	max	max	min	max	min
HSUL12D	0.1	0.3	0.6	0.85	0.2VCCIO	0.8VCCIO	0.1	- 0.1
SSTL135D_I	0.1	0.3	0.675	1	0.5VCCIO- 0.15	0.5VCCIO+0.15	8.9	- 8.9
SSTL135D_II	0.1	0.3	0.675	1	0.5VCCIO- 0.15	0.5VCCIO+0.15	13	- 13
HSTL15D_I	0.1	0.3	0.75	1.125	0.4	VCCIO- 0.4	8	- 8
HSTL15D_II	0.1	0.3	0.75	1.125	0.4	VCCIO- 0.4	16	- 16
HSTL18D_I	0.1	0.3	0.9	1.425	0.4	VCCIO- 0.4	8	- 8
HSTL18D_II	0.1	0.3	0.9	1.425	0.4	VCCIO- 0.4	16	- 16
LPDDRD	0.1	0.3	0.9	1.425	0.1VCCIO	0.9VCCIO	0.1	- 0.1
SSTL15D_I	0.1	0.3	0.75	1.125	0.5VCCIO-0.175	0.5VCCIO+0.175	0.89	- 0.89
SSTL15D_II	0.1	0.3	0.75	1.125	0.5VCCIO-0.175	0.5VCCIO+0.175	13	- 13
SSTL18D_I	0.1	0.3	0.9	1.425	0.5VCCIO- 0.47	0.5VCCIO+0.47	8	- 8
SSTL18D_II	0.1	0.3	0.9	1.425	0.5VCCIO- 0.6	0.5VCCIO+0.6	13.4	- 13.4

4. AC Characteristics under Typical Operating Conditions

This chapter mainly lists the AC characteristics of each logic unit of Logos2 series FPGA under typical working conditions.

4.1. Configurable logic module CLM AC characteristic parameters

Table 4-1 CLM Module AC Characteristics

Delay time			Unit	Parameter Description
- 5	- 6	- 7		
Logic delay				
0.24	0.196	TBD	ns,max	LUT6 Input Ax/Bx/Cx/Dx to Y0/Y1/Y2/Y3 delay
0.452	0.353	TBD	ns,max	LUT6 Input Ax/Bx/Cx/Dx to CR0/CR1 delay (LUT7)
0.445	0.395	TBD	ns,max	LUT6 Input Ax/Bx/Cx/Dx to CR2 delay to Y1 (LUT8)
0.449	0.357	TBD	ns,max	LUTs input Ax Delay to CYA(CR0)
0.446	0.371	TBD	ns,max	LUTs input Bx Delay to CYB(CR1)
0.452	0.358	TBD	ns,max	LUTs input Cx Delay to CYC (CR2)
0.434	0.353	TBD	ns,max	LUTs input Dx Delay to CYD(CR3)
0.105	0.065	TBD	ns,max	CIN input to COUT delay
Timing parameters				
0.227	0.198	TBD	ns,max	CLK Input relative to Q0/Q1/Q2/Q3 TCO
0.27	0.218	TBD	ns,max	CLK Input relative to CR0/CR1/CR2/CR3 TCO
0.288/- 0.08	0.22/- 0.16	TBD	ns,min	Ax/Bx/Cx/Dx relative to DFF setup /hold
0.16/- 0.1	0.12/0.04	TBD	ns,min	M relative to DFF setup /hold
0.224/- 0.07	0.13/- 0.04	TBD	ns,min	CE relative to DFF setup /hold
0.224/- 0.07	0.11/- 0.05	TBD	ns,min	RS relative to DFF setup /hold
Distributed RAM Timing parameters				
0.455	0.63	TBD	ns,max	CLK -> Y0/Y1/Y2/Y3 mem read delay
0.56	0.71	TBD	ns,max	CLK -> CR0/CR1/CR2/CR3 mem read delay
- 0.26/0.28	0.145/0.083	TBD	ns,min	CLK -> WE timing check, setup/hold
0.24/- 0.07	0.048/0.193	TBD	ns,min	CLK -> An address timing check, setup/hold
- 0.26/0.28	0.048/0.193	TBD	ns,min	CLK -> AD/BD/CD/DD data timing check,setup/hold

4.2. Dedicated RAM module DRM AC characteristic parameters

Table 4-2 DRM Module AC Characteristics

Name	Numerical value			Unit	AC characteristic parameter description
	- 5	- 6	- 7		
T_{co_18K}	1.75	1.529	TBD	ns,max	CLKA/CLKB->QA/QB (output register disabled, 18K mode)
$T_{co\_18K\_reg}$	0.718	0.625	TBD	ns,max	CLKA/CLKB->QA/QB (output register enabled, 18K mode)
T_{co_36K}	1.758	1.529	TBD	ns,max	CLKA/CLKB->QA/QB (output register disabled, 36K mode)

$T_{co\_36K\_reg}$	0.718	0.625	TBD	ns,max	CLKA/CLKB->QA/QB (output register enabled, 36K mode)
T_{co_ecc}	1.758	1.529	TBD	ns,max	CLKB->QA/QB (output register disabled, ECC mode)
$T_{co\_ecc\_reg}$	0.718	0.625	TBD	ns,max	CLKB->QA/QB (output register enabled, ECC mode)
$T_{co\_ecc\_err}$	0.718	0.625	TBD	ns,max	CLKB->ECC_S/DBITERR (output register enabled, ECC mode)
$T_{co\_flag\_full}$	1.11	0.966	TBD	ns,max	CLKA->FULL(ALMOST_FULL) (18K/36K FIFO mode)
$T_{co\_flag\_empty}$	0.652	0.567	TBD	ns,max	CLKB->EMPTY(ALMOST_EMPTY) (18K/36K FIFO mode)
$T_{co\_ecc\_parity}$	0.407	0.354	TBD	ns,max	CLKA->ECC_PARITY (ECC encoding mode)
$T_{co\_ecc\_rdaddr}$	0.834	0.726	TBD	ns,max	CLKA->ECC_RDADDR (output register disabled, ECC mode)
$T_{co\_ecc\_rdaddr\_reg}$	0.834	0.726	TBD	ns,max	CLKA->ECC_RDADDR (output register enabled, ECC mode)
$T_{su\_18K\_ad}$ / $T_{hd\_18K\_ad}$	- 0.077/0.097	- 0.067/0.085	TBD	ns,min	Address input Setup/Hold time (18K mode)
$T_{su\_18K\_d}$ / $T_{hd\_18K\_d}$	- 0.002/0.043	- 0.002/0.038	TBD	ns,min	Data input Setup/Hold time (18K mode)
$T_{su\_18K\_ce}$ / $T_{hd\_18K\_ce}$	0.034/0.029	0.03/0.026	TBD	ns,min	CE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_we}$ / $T_{hd\_18K\_we}$	- 0.065/0.086	- 0.057/0.075	TBD	ns,min	WE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_be}$ / $T_{hd\_18K\_be}$	- 0.010/0.029	- 0.009/0.026	TBD	ns,min	BE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_oe}$ / $T_{hd\_18K\_oe}$	- 0.060/0.080	- 0.053/0.070	TBD	ns,min	OCE Enter Setup/Hold time (18K mode)
$T_{su\_18K\_rst}$ / $T_{hd\_18K\_rst}$	0.001/0.017	0.001/0.015	TBD	ns,min	Synchronous reset input Setup/Hold time (18K mode)
$T_{su\_36K\_ad}$ / $T_{hd\_36K\_ad}$	- 0.077/0.097	- 0.067/0.085	TBD	ns,min	Address input Setup/Hold time (36K mode)
$T_{su\_36K\_d}$ / $T_{hd\_36K\_d}$	- 0.002/0.043	- 0.002/0.038	TBD	ns,min	Data input Setup/Hold time (36K mode)
$T_{su\_36K\_ce}$ / $T_{hd\_36K\_ce}$	0.034/-0.014	0.03/-0.013	TBD	ns,min	CE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_we}$ / $T_{hd\_36K\_we}$	- 0.033/0.054	- 0.029/0.047	TBD	ns,min	WE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_be}$ / $T_{hd\_36K\_be}$	- 0.01/0.029	- 0.009/0.026	TBD	ns,min	BWE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_oe}$ / $T_{hd\_36K\_oe}$	- 0.027/0.047	- 0.024/0.041	TBD	ns,min	OCE Enter Setup/Hold time (36K mode)
$T_{su\_36K\_rst}$ / $T_{hd\_36K\_rst}$	0.001/0.017	0.001/0.015	TBD	ns,min	Synchronous reset input Setup/Hold time (36K mode)
$T_{su\_ecc\_d}$ / $T_{hd\_ecc\_d}$	0.021/0.018	0.019/0.016	TBD	ns,min	Data input Setup/Hold time (ECC mode)

$T_{su\_fifo\_wctl}$ / $T_{hd\_fifo\_wctl}$	- 0.065/0.086	- 0.057/0.075	TBD	ns,min	WREN Enter (Setup/Hold time) (18K/36K FIFO mode)
$T_{su\_fifo\_rctl}$ / $T_{hd\_fifo\_rctl}$	0.03/-0.014	0.03/-0.013	TBD	ns,min	RDEN Enter (Setup/Hold time (18K/36K FIFO mode)
$T_{su\_ecc\_injerr}$ / $T_{hd\_ecc\_injerr}$	0.021/0.018	0.019/0.016	TBD	ns,min	INJECT_S/DBITERR Enter Setup/Hold time (ECC mode)
T_{mpw_norm}	1.104	0.960	TBD	ns,min	CLKA/CLKB MPW (NW/TW mode)
T_{mpw_rbw}	1.546	1.345	TBD	ns,min	CLKA/CLKB MPW (RBW mode)
T_{mpw_fifo}	1.104	0.960	TBD	ns,min	CLKA/CLKB MPW (FIFO mode)
T_{mpw_ecc}	1.104	0.960	TBD	ns,min	CLKA/CLKB MPW (ECC mode)

4.3. Arithmetic Processing Unit APM AC characteristic parameters

Table 4-3 APM Module AC Characteristics

AC characteristic parameter description	Pre-dder	Multiplier	Post-adder	Numerical value			Unit
				- 5	- 6	- 7	
Setup and hold time from data/control Pin to input register clk							
H → preadd unit register CLK setup/hold	Yes	NA	NA	1.376/- 0.1	1.197/-0.141	TBD	ns
X → preadd unit register CLK setup/hold	Yes	NA	NA	1.58/- 0.16	1.376/-0.147	TBD	ns
X → input unit register CLK setup/hold	NA	NA	NA	0.38/- 0.02	0.336/-0.020	TBD	ns
Y → input unit register CLK setup/hold	NA	NA	NA	0.22/- 0.03	0.196/-0.028	TBD	ns
H → input unit register CLK setup/hold	NA	NA	NA	0.28/- 0.04	0.248/-0.042	TBD	ns
Z → input unit register CLK setup/hold	NA	NA	NA	0.16/0.01	0.146/0.010	TBD	ns
INCTRL → input unit register CLK setup/hold	NA	NA	NA	0.16/0	0.144/0.000	TBD	ns
MODEY → input unit register CLK setup/hold	NA	NA	NA	0.16/- 0.009	0.147/-0.008	TBD	ns
MODEZ → input unit register CLK setup/hold	NA	NA	NA	0.25/- 0.01	0.220/-0.014	TBD	ns
Setup and hold time from data Pin to pipeline register clk							
Y → Multiplier unit register CLK setup/hold	NA	Yes	No	1.47/- 0.25	1.281/-0.226	TBD	ns
X → Multiplier unit register CLK setup/hold	Yes	Yes	No	2.76/- 0.38	2.402/-0.333	TBD	ns
X → Multiplier unit register CLK setup/hold	No	Yes	No	1.57/- 0.26	1.373/-0.233	TBD	ns
H-> Multiplier unit register CLK setup/hold	Yes	Yes	No	2.55/- 0.36	2.224/-0.316	TBD	ns
Setup and hold time from data/control Pin to output register clk							
Y → postadd unit register CLK setup/hold	NA	Yes	Yes	2.51/- 0.512	2.190/-0.446	TBD	ns

X → postadd unit register CLK setup/hold	No	Yes	Yes	2.636/- 0.52	2.293/-0.454	TBD	ns
X → postadd unit register CLK setup/hold	Yes	Yes	Yes	3.82/- 0.63	3.322/-0.554	TBD	ns
H → postadd unit register CLK setup/hold	Yes	Yes	Yes	3.61/- 0.617	3.144/-0.537	TBD	ns
Z → postadd unit register CLK setup/hold	NA	NA	Yes	1.411/- 0.23	1.227/-0.208	TBD	ns
Y → postadd unit register CLK setup/hold	NA	No	Yes	1.447/- 0.27	1.259/-0.242	TBD	ns
X → postadd unit register CLK setup/hold	No	No	Yes	1.342/- 0.28	1.167/-0.247	TBD	ns
PI → postadd unit register CLK setup/hold	NA	NA	Yes	1.314/- 0.04	1.143/-0.035	TBD	ns
From register clk at all levels to APM output Pin time							
postadd unit register CLK → P output	NA	NA	NA	0.380	0.331	TBD	ns
Multiplier unit register CLK → Poutput	NA	NA	Yes	1.703	1.481	TBD	ns
Multiplier unit register CLK → Poutput	NA	NA	No	0.488	0.425	TBD	ns
pretadd unit register CLK → D PO output	Yes	Yes	Yes	2.58	2.248	TBD	ns
Z input unit register CLK → D PO output	NA	NA	Yes	1.59	1.390	TBD	ns
Combination logic delay from data/control pin to APM output pin							
Y → P output	NA	Yes	No	1.86	1.619	TBD	ns
Y → P output	NA	Yes	Yes	2.75	2.399	TBD	ns
Y → P output	NA	No	Yes	1.66	1.444	TBD	ns
X → P output	No	Yes	No	1.93	1.680	TBD	ns
X → P output	Yes	Yes	No	2.94	2.564	TBD	ns
X → P output	Yes	Yes	Yes	4.03	3.512	TBD	ns
X → P output	No	No	Yes	1.50	1.308	TBD	ns
H → P output	Yes	Yes	No	2.95	2.568	TBD	ns
H → P output	Yes	Yes	Yes	3.84	3.347	TBD	ns
Z → P output	NA	NA	Yes	1.62	1.410	TBD	ns
PI → P output	NA	NA	Yes	1.53	1.339	TBD	ns

4.4. GPLL AC (AC) Characteristics Parameters

Table 4-4 GPLL AC Characteristics

Name	Minimum	Maximum value	Unit	Description
F_{IN}	10	800	MHz	input clock frequency
F_{INJIT}	300		ps	Input Clock Jitter (F_{IN} < 200MHz)
	0.06		UI	Input Clock Jitter (F_{IN} ≥ 200MHz)
F_{INDT}	10-49MHz： 25% 50-199MHz： 30% 200-399MHz： 35% 400-499MHz： 40% 500-800MHz： 45%			Input clock duty cycle
F_{PFD}	10	450	MHz	PFD operating frequency range
F_{VCO}	600	1200	MHz	VCO operating frequency range
F_{OUT}	4.69	800	MHz	Output clock frequency range
F_{OUTCAS}	0.0366	800	MHz	Output Cascade Frequency Range
T_{PHO}	0.12		ns	static phase offset
T_{OUTJIT}	180		ps	Output Clock Jitter (F_{OUT} ≥ 100MHz)
	0.018		UI	Output Clock Jitter (F_{OUT} < 100MHz)
$T_{OUTDUTY}$	50% ± 5%			Output Clock Duty Cycle Accuracy (50% Case)
F_{BW}	1	4	MHz	loop bandwidth
T_{LOCK}	-- -	200	us	lock time
F_{DPS_CLK}	0.01	450	MHz	Dynamic Phase Shift Clock Frequency
T_{RST}	10	-- -	ns	Reset signal width

4.5. PPLL AC (AC) Characteristics Parameters

Table 4-5 PPLL AC Characteristics

Name	Minimum	Maximum value	Unit	Description
F_{IN}	19	800	MHz	input clock frequency
F_{INJIT}	200		ps	Input Clock Jitter (F_{IN} < 200MHz)
	0.04		UI	Input Clock Jitter (F_{IN} ≥ 200MHz)
F_{INDT}	10-49MHz： 25% 50-199MHz： 30% 200-399MHz： 35% 400-499MHz： 40% 500-800MHz： 45%			Input clock duty cycle
F_{PFD}	19	450	MHz	PFD operating frequency range
F_{VCO}	1330	2133	MHz	VCO operating frequency range
F_{OUT}	10.39	2133	MHz	Output clock frequency range
T_{PHO}	0.12		ns	static phase offset
T_{OUTJTT}	180		ps	Output Clock Jitter (F_{OUT} ≥ 100MHz)
	0.018		UI	Output Clock Jitter (F_{OUT} < 100MHz)
T_{OUTDT}	50% ± 5%			Output Clock Duty Cycle Accuracy (50% Case)
F_{BW}	1	4	MHz	bandwidth

T_{LOCK}	-- -	120	us	lock time
T_{RST}	10	-- -	ns	Reset signal width

4.6. DQS AC AC characteristic parameters

DQS phase adjustment are as follows :

Table 4-6 DQS AC characteristics

Name	Speed class	AC characteristic parameter description			Unit
		Min	Typical value	Max	
DQS	**-5, - 6**	4	7	10	ps

4.7. Global Clock Network AC characteristic parameters

Table 4-7 Global Clock Network AC Characteristics

Name	Maximum frequency	Unit	Description
	-5, - 6		
GLOBAL CLK	600	MHz	global clock network

4.8. Regional clock network AC characteristic parameters

Table 4-8 Regional Clock Network AC Characteristics

Name	Maximum frequency	Unit	Description
	-5, - 6		
REGIONAL CLK	350	MHz	regional clock network

Note: The maximum input frequency is 650 MHz

4.9. IO Clock Network AC characteristic parameters

Table 4-9 IO Clock Network AC Characteristics

Name	Maximum frequency	Unit	Description
	-5, - 6		
IO CLK	680	MHz	IO clock network

4.10. Configuration and programming AC characteristic parameters

4.10.1. Power-up Timing feature

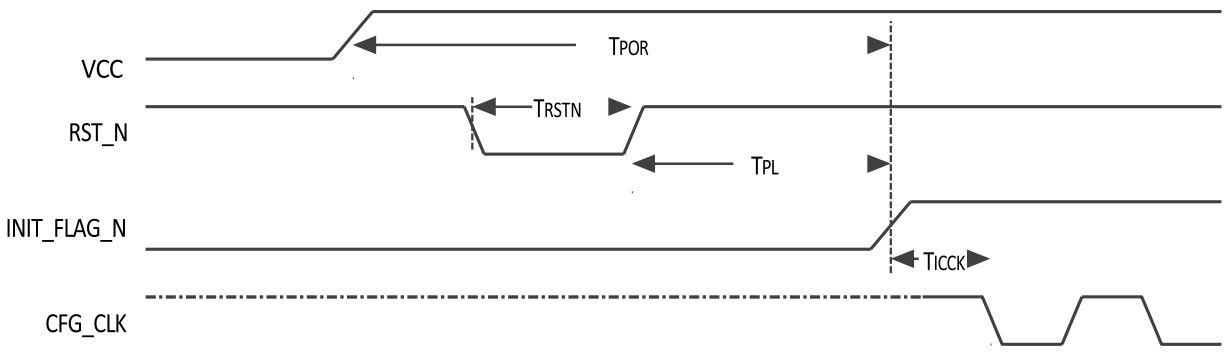

Figure 4-1 Device Power-up Timing Characteristics

Table 4-10 Power-up Timing characteristic parameters

Name	Device	Value	Unit	Description
T_{PL}	PG2L25H	3.6	ms, Max	Program Latency
	PG2L50H	6		
	PG2L100H	11		
T_{POR}	PG2L25H	63.6	ms, Max	Power-on-Reset
	PG2L50H	66		
	PG2L100H	71		
T_{ICCK}	Logos2	400	ns,Min	CFG_CLK output delay
T_{RSTN}		384	ns,Min	RST_N low pulse width

4.10.2. AC Characteristics for Each Download Mode

Table 4-11 AC Characteristics of Each Download Mode Supported by Logos2 Series FPGAs

Interface	Description	Numerical value	Attributes
JTAG	TCK frequency	50M	maximum
	TCK duty cycle	45%/55%	min / max
	TCK high pulse width	10ns	minimum
	TMS/TDI setup time (rising edge of TCK)	3.5ns	minimum
	TMS/TDI hold time (TCK rising edge)	1.5ns	minimum
	TCK falling edge to TDO output valid	6ns	maximum
Master SPI Mode	CFG_CLK frequency	40M	maximum
	CFG_CLK frequency (low speed)	15.38M	maximum
	CFG_CLK frequency (daisy chain)	25M	maximum
	CFG_CLK frequency initial value	2.99M	typical
	CFG_CLK duty cycle	45%/55%	min / max
	CFG_CLK frequency deviation	50 %	maximum
	ECCLKIN frequency	66M	maximum
	ECCLKIN frequency (low speed)	33M	maximum
	ECCLKIN duty cycle	45%/55%	min / max
	D[7:0] setup time (CFG_CLK rising edge)	9.5ns	minimum
	D[7:0] hold time (CFG_CLK rising edge)	0ns	minimum
	D[7:0] setup time (CFG_CLK falling edge)	9.5ns	minimum
	D[7:0] hold time (CFG_CLK falling edge)	0ns	minimum
	CFG_CLK falling edge to D[0]/D[4] output valid	3.5ns	maximum
	CFG_CLK falling edge to FCS_N/FCS2_N output valid	4ns	maximum
	CFG_CLK falling edge to CSO_DOUT output valid	3.5ns	maximum
Slave Serial	CFG_CLK frequency	80M	maximum
	CFG_CLK frequency (daisy chain)	50M	maximum

	CFG_CLK low pulse width	6ns	minimum
	CFG_CLK high pulse width	6ns	minimum
	DI setup time (CFG_CLK rising edge)	3.5ns	minimum
	DI hold time (CFG_CLK rising edge)	0ns	minimum
	CFG_CLK falling edge to CSO_DOUT output valid	7ns	maximum
Slave Parallel	CFG_CLK frequency	80M	maximum
	CFG_CLK low pulse width	6ns	minimum
	CFG_CLK high pulse width	6ns	minimum
	D[31:0] setup time (CFG_CLK rising edge)	5.5ns	minimum
	D[31:0] hold time (CFG_CLK rising edge)	0.5ns	minimum
	CS_N/RWSEL setup time (CFG_CLK rising edge)	4.5ns	minimum
	CS_N/RWSEL hold time (CFG_CLK rising edge)	0.5ns	minimum
	CFG_CLK rising edge to D[31:0] output valid	9ns	maximum
	CS_N to CSO_DOUT output delay	8.5ns	maximum
Internal slave parallel interface	CLK frequency	80M	maximum
	CLK low pulse width	2.5ns	minimum
	CLK high pulse width	2.5ns	minimum
	CS_N/RW_SEL/DI[31:0] setup time (CLK rising edge)	2ns	minimum
	CS_N/RW_SEL/DI[31:0] hold time (CLK rising edge)	1ns	minimum
	CLK rising edge to DO[31:0] output valid	4ns	maximum
	CLK rising edge to RBCRC_VALID/ECC_VALID/DRCFG_OVER/PRCFG_OVER output is valid	2ns	maximum
	CLK rising edge to RBCRC_ERR/ECC_INDEX/SERROR/DERROR/SEU_FRAME_ADDR/SEU_FRAME_NADDR SEU_COLUMN_ADDR/SEU_COLUMN_NADDR SEU_REGION_ADDR/SEU_REGION_NADDR DRCFG_ERR/PRCFG_ERR output valid	0	maximum

4.11. IOB High Range(HR) AC characteristic parameters

The AC characteristic parameters of IOB High Range(HR) are shown in the table below, where DO=>PAD is the delay from IOB port DO through OBUF to PAD; PAD=>DIN is the delay from PAD through IBUF to IOB port DIN.

Table 4-12 IOB High Range(HR)AC Characteristics Parameters

I/O standard	Delay(DO=>PAD)/ns	Delay(PAD=>DIN)/ns
LVCMOS33 STRENGTH"4" MODE"F"	1.705	0.8347
LVCMOS33 STRENGTH "4" MODE"S"	2.376	0.8347
LVCMOS33 STRENGTH "8" MODE"F"	1.688	0.8347
LVCMOS33 STRENGTH "8" MODE"S"	2.369	0.8347
LVCMOS33 STRENGTH"12" MODE"F"	1.466	0.8347
LVCMOS33 STRENGTH"12" MODE"S"	2.172	0.8347
LVCMOS33 STRENGTH"16" MODE"F"	1.266	0.8347
LVCMOS33 STRENGTH"16" MODE"S"	1.913	0.8347
LVTTL33 STRENGTH "4" MODE"F"	1.705	0.8347
LVTTL33 STRENGTH"4" MODE"S"	2.376	0.8347
LVTTL33 STRENGTH "8" MODE"F"	1.688	0.8347
LVTTL33 STRENGTH "8" MODE"S"	2.369	0.8347
LVTTL33 STRENGTH"12" MODE"F"	1.466	0.8347
LVTTL33 STRENGTH "12" MODE "S"	2.172	0.8347
LVTTL33 STRENGTH"16" MODE"F"	1.266	0.8347
LVTTL33 STRENGTH"16" MODE"S"	1.913	0.8347
LVTTL33 STRENGTH"24" MODE"F"	1.266	0.8347
LVTTL33 STRENGTH"24" MODE"S"	1.913	0.8347

LVCMOS25 STRENGTH"4" MODE"F"	1.49	0.8982
LVCMOS25 STRENGTH"4" MODE"S"	2.084	0.8982
LVCMOS25 STRENGTH"8" MODE"F"	1.525	0.8982
LVCMOS25 STRENGTH"8" MODE"S"	2.325	0.8982
LVCMOS25 STRENGTH"12" MODE"F"	1.354	0.8982
LVCMOS25 STRENGTH"12" MODE"S"	2.115	0.8982
LVCMOS25 STRENGTH"16" MODE"F"	1.23	0.8982
LVCMOS25 STRENGTH"16" MODE"S"	1.903	0.8982
LVCMOS18 STRENGTH"4" MODE"F"	1.068	0.996
LVCMOS18 STRENGTH"4" MODE"S"	1.274	0.996
LVCMOS18 STRENGTH"8" MODE"F"	0.9271	0.996
LVCMOS18 STRENGTH"8" MODE"S"	1.151	0.996
LVCMOS18 STRENGTH"12" MODE"F"	0.8111	0.996
LVCMOS18 STRENGTH"12" MODE"S"	0.9624	0.996
LVCMOS18 STRENGTH"16" MODE"F"	0.8024	0.996
LVCMOS18 STRENGTH"16" MODE"S"	0.9805	0.996
LVCMOS18 STRENGTH"24" MODE"F"	0.8218	0.996
LVCMOS18 STRENGTH"24" MODE"S"	0.9408	0.996
LVCMOS15 STRENGTH "4" MODE"F"	1.003	1.091

LVCMOS15 STRENGTH "4" MODE"S"	1.214	1.091
LVCMOS15 STRENGTH"8" MODE"F"	1.003	1.091
LVCMOS15 STRENGTH"8" MODE"S"	1.214	1.091
LVCMOS15 STRENGTH"12" MODE"F"	0.7844	1.091
LVCMOS15 STRENGTH"12" MODE"S"	0.9222	1.091
LVCMOS15 STRENGTH"16" MODE"F"	0.8026	1.091
LVCMOS15 STRENGTH"16" MODE"S"	0.9151	1.091
LVCMOS12 STRENGTH"4" MODE"F"	0.9499	1.238
LVCMOS12 STRENGTH"4" MODE"S"	1.156	1.238
LVCMOS12 STRENGTH"8" MODE"F"	0.9499	1.238
LVCMOS12 STRENGTH"8" MODE"S"	1.156	1.238
LVCMOS12 STRENGTH"12" MODE"F"	0.9118	1.238
LVCMOS12 STRENGTH "12" MODE "S"	1.034	1.238
SSTL18_I STRENGTH"8" MODE"F"	0.7247	0.871
SSTL18_I STRENGTH"8" MODE"S"	0.8676	0.871
SSTL18_I STRENGTH "13.4" MODE "F"	0.6479	0.871
SSTL18_I STRENGTH "13.4" MODE "S"	0.7475	0.871
SSTL18_II STRENGTH"8" MODE"F"	0.7247	0.871
SSTL18_II STRENGTH"8" MODE"S"	0.8676	0.871

SSTL18_II STRENGTH "13.4" MODE "F"	0.6479	0.871
SSTL18_II STRENGTH "13.4" MODE "S"	0.7475	0.871
SSTL18D_I STRENGTH"8" MODE"F"	0.7247	0.871
SSTL18D_I STRENGTH"8" MODE"S"	0.8676	0.871
SSTL18D_I STRENGTH "13.4" MODE "F"	0.6479	0.871
SSTL18D_I STRENGTH "13.4" MODE "S"	0.7475	0.871
SSTL18D_II STRENGTH"8" MODE"F"	0.7247	0.871
SSTL18D_II STRENGTH"8" MODE"S"	0.8676	0.871
SSTL18D_II STRENGTH"13.4" MODE"F"	0.6479	0.871
SSTL18D_II STRENGTH"13.4" MODE"S"	0.7475	0.871
HSTL18_I STRENGTH"8" MODE"F"	0.7247	0.871
HSTL18_I STRENGTH"8" MODE"S"	0.8676	0.871
HSTL18_I STRENGTH"16" MODE"F"	0.6479	0.871
HSTL18_I STRENGTH"16" MODE"S"	0.7475	0.871
HSTL18_II STRENGTH"8" MODE"F"	0.7247	0.871
HSTL18_II STRENGTH"8" MODE"S"	0.8676	0.871
HSTL18_II STRENGTH"16" MODE"F"	0.6479	0.871
HSTL18_II STRENGTH"16" MODE"S"	0.7475	0.871
HSTL18D_I STRENGTH"8" MODE"F"	0.7247	0.871

HSTL18D_I STRENGTH"8" MODE"S"	0.8676	0.871
HSTL18D_I STRENGTH"16" MODE"F"	0.6479	0.871
HSTL18D_I STRENGTH"16" MODE"S"	0.7475	0.871
HSTL18D_II STRENGTH"8" MODE"F"	0.7247	0.871
HSTL18D_II STRENGTH"8" MODE"S"	0.8676	0.871
HSTL18D_II STRENGTH"16" MODE"F"	0.6479	0.871
HSTL18D_II STRENGTH"16" MODE"S"	0.7475	0.871
SSTL15_I STRENGTH"8.9" MODE"F"	0.7278	0.9481
SSTL15_I STRENGTH"8.9" MODE"S"	0.8599	0.9481
SSTL15_I STRENGTH"13" MODE"F"	0.7295	0.9481
SSTL15_I STRENGTH"13" MODE"S"	0.8726	0.9481
SSTL15_II STRENGTH"8.9" MODE"F"	0.7278	0.9481
SSTL15_II STRENGTH"8.9" MODE"S"	0.8599	0.9481
SSTL15_II STRENGTH"13" MODE"F"	0.7295	0.9481
SSTL15_II STRENGTH"13" MODE"S"	0.8726	0.9481
SSTL15D_I STRENGTH "8.9" MODE"F"	0.7278	0.9481
SSTL15D_I STRENGTH "8.9" MODE"S"	0.8599	0.9481
SSTL15D_I STRENGTH"13" MODE"F"	0.7295	0.9481
SSTL15D_I STRENGTH"13" MODE"S"	0.8726	0.9481

SSTL15D_II STRENGTH"8.9" MODE"F"	0.7278	0.9481
SSTL15D_II STRENGTH"8.9" MODE"S"	0.8599	0.9481
SSTL15D_II STRENGTH"13" MODE"F"	0.7295	0.9481
SSTL15D_II STRENGTH"13" MODE"S"	0.8726	0.9481
HSTL15_I STRENGTH"8" MODE"F"	0.7278	0.9481
HSTL15_I STRENGTH"8" MODE"S"	0.8599	0.9481
HSTL15_I STRENGTH"16" MODE"F"	0.7295	0.9481
HSTL15_I STRENGTH"16" MODE"S"	0.8726	0.9481
HSTL15_II STRENGTH"8" MODE"F"	0.7278	0.9481
HSTL15_II STRENGTH"8" MODE"S"	0.8599	0.9481
HSTL15_II STRENGTH"16" MODE"F"	0.7295	0.9481
HSTL15_II STRENGTH"16" MODE"S"	0.8726	0.9481
HSTL15D_I STRENGTH"8" MODE"F"	0.7278	0.9481
HSTL15D_I STRENGTH"8" MODE"S"	0.8599	0.9481
HSTL15D_I STRENGTH"16" MODE"F"	0.7295	0.9481
HSTL15D_I STRENGTH"16" MODE"S"	0.8726	0.9481
HSTL15D_II STRENGTH"8" MODE"F"	0.7278	0.9481
HSTL15D_II STRENGTH"8" MODE"S"	0.8599	0.9481
HSTL15D_II STRENGTH"16" MODE"F"	0.7295	0.9481

HSTL15D_II STRENGTH"16" MODE"S"	0.8726	0.9481
SSTL135_I STRENGTH "8.9" MODE "F"	0.7459	1.071
SSTL135_I STRENGTH "8.9" MODE "S"	0.8795	1.071
SSTL135_I STRENGTH "13" MODE "F"	0.7036	1.071
SSTL135_I STRENGTH"13" MODE"S"	0.8431	1.071
SSTL135_II STRENGTH "8.9" MODE "F"	0.7459	1.071
SSTL135_II STRENGTH"8.9" MODE"S"	0.8795	1.071
SSTL135_II STRENGTH"13" MODE"F"	0.7036	1.071
SSTL135_II STRENGTH"13" MODE"S"	0.8431	1.071
SSTL135D_I STRENGTH "8.9" MODE"F"	0.7459	1.071
SSTL135D_I STRENGTH "8.9" MODE "S"	0.8795	1.071
SSTL135D_I STRENGTH"13" MODE"F"	0.7036	1.071
SSTL135D_I STRENGTH"13" MODE"S"	0.8431	1.071
SSTL135D_II STRENGTH"8.9" MODE"F"	0.7459	1.071
SSTL135D_II STRENGTH"8.9" MODE"S"	0.8795	1.071
SSTL135D_II STRENGTH"13" MODE"F"	0.7036	1.071
SSTL135D_II STRENGTH"13" MODE"S"	0.8431	1.071
LPDDR MODE "F"	0.9499	1.238
LPDDR MODE "S"	1.156	1.238
HSUL12 MODE "F"	0.9499	1.238
HSUL12 MODE "S"	1.156	1.238
TMDS	0.9883	0.9481
LVDS25	0.9883	0.9481
MINI- LVDS	0.9883	0.9481

RSDS	0.9883	0.9481
PPDS	0.9883	0.9481

5. Performance parameters under typical working conditions (Fabric Performance)

This chapter lists the performance features that implement common applications of Logos2 series FPGAs .

5.1. LVDS performance parameters

Table 5-1 LVDS performance

Description	Maximum rate		Unit	IO resource
	- 5	- 6		
SDR LVDS Transmitter	400	450	Mbps	OSERDES(DATA _WIDTH =4 TO 8)
DDR LVDS Transmitter	800	900	Mbps	OSERDES(DATA _WIDTH =4 TO 8)
SDR LVDS Receiver	400	450	Mbps	ISERDES(DATA _WIDTH =4 TO 8)
DDR LVDS Receiver	800	900	Mbps	ISERDES(DATA _WIDTH =4 TO 8)

5.2. Memory interface performance parameters (Memory Interface Performance)

Table 5-2 Storage Interface Performance

Name	Maximum rate	Unit
	-5, - 6	
DDR3	800	Mbps
DDR3L	667	Mbps
DDR2	667	Mbps
LPDDR2	667	Mbps
LPDDR	400	Mbps
QDR2	500	Mbps

5.3. Dedicated RAM module DRM performance parameters

Table 5-3 DRM performance

Pattern	Performance (MHz)
	-5, - 6
DRM(NW mode & read register enable) @ 18K memory mode	400
DRM(TW mode & read register enable) @ 18K memory mode	400
DRM (RBW mode & read register enable) @ 18K memory mode	350
DRM (synchronous FIFO mode & read register enable)	400
DRM (ECC mode)	300

5.4. Arithmetic Process Module APM performance parameters

Table 5-4 APM performance

Condition	Performance (MHz)
	-5, - 6
All registers used (using the registers of each level of the APM)	460
Only use INREG and PREG (use only APM's input and output registers)	190

6. Analog-to-Digital Converter (ADC) Characteristics

This chapter mainly introduces the characteristic parameters of the ADC hard core of Logos2 series FPGA , as shown in the following table.

Table 6-1 ADC Hard Core Features

Parameter	Minimum	Typical value	Maximum value	Unit	Description / condition	
VCCADC = 1.8V ± 5 %, VREFP = 1.255V , VREFN = 0V , ADCCLK = 26 MHz, Tj:–40°C ~125°C, dedicated channel; Typical values at Tj=+40°C Vinp -p=-0.45dB Full Scale ;						
VCCADC	1.71	1.8	1.89	V	Analog supply voltage	
Resolution	12	- -	- -	Bits	Resolution	
Sample Rate	- -	- -	1	MSPS	Sampling Rate	
Channel	- -	- -	17		aisle	
Voltage Reference	1.205	1.255	1.305	V	External reference voltage	
	1.230	1.255	1.280	V	Internal reference voltage	Ground VREFP pin to AGND, –40°C≤ Tj ≤125°C
Offset Error	- -	- -	±4	LSB	Bipolar	–40°C≤ Tj <125°C
	- -	- -	±12	LSB	Unipolar	–40°C≤ Tj ≤125°C
Gain Error	- -	±1	- -	%FS	Gain error calibration Post gain error	
DNL	- -	- -	- 1<DNL<5	LSB	Differential Nonlinear ; Nomissing codes	
INL	- -	- -	±4	LSB	Integeral Nonlinear	–40°C≤ T_j ≤125°C
SNR_1		58	- -	dB	Signal to Noise Ratio	F_{SAMPLE} = 500KS/s, F_{IN} = 20kHz dedicated channel
SNR_2		58		dB	Signal to Noise Ratio	F_{SAMPLE} = 500KS/s, F_{IN} = 20kHz Auxiliary channel
THD_1	- -	64		dB	2nd - to 7th - total harmonic distortion	F_{SAMPLE} = 500KS/s, F_{IN} = 20 kHz dedicated channel
THD_2	- -	62		dB	2nd - to 7th - total harmonic distortion	F_{SAMPLE} = 500KS/s, F_{IN} = 20 kHz Auxiliary channel
Temperature Sensor ccuracy	- -	- -	±4	°C	Temperature detection accuracy	–40°C≤ Tj ≤100°C
	- -	- -	±6	°C		100°C< Tj ≤125°C

Note: 1. The typical data in the table above are the test results of different bias voltages at room temperature;
2. ADC samples the auxiliary IO channel, and the auxiliary IO needs to be constrained in the 1.8V power domain;
3. -5 does not support temperature sensor function

7. High Speed Serial Transceiver (HSSTLP) Features

This chapter mainly introduces the characteristics of the HSSTLP hard core of the Logos2 series FPGA, including the absolute limit rated voltage/current, recommended operating conditions, AC/DC characteristics, and characteristics that support typical protocol operating modes.

7.1. HSSTLP hard core absolute limit voltage, current rating

Table 7-1 HSSTLP absolute limit voltage, current rating

Name	Minimum	Maximum value	Unit	Description
HSSTAVCC	–0.5	1.21	V	HSST analog power supply 1.0V voltage
HSSTAVCCPLL	–0.5	1.32	V	HSST PLL analog power supply 1.2V voltage

Note: Exceeding the above limit ratings may cause permanent damage to the device.

7.2. HSSTLP Hardcore Recommended Operating Conditions

The following table lists the recommended working voltage of the HSSTLP hard core for Logos2 series FPGAs .

Table 7-2 HSSTLP Hardcore Recommended Operating Conditions

Name	Minimum	Typical value	Maximum value	Unit	Description
Voltage value					
HSSTAVCC	0.97	1.0	1.03	V	HSST analog power supply 1.0V voltage
HSSTAVCCPLL	1.17	1.2	1.23	V	HSST PLL analog power supply 1.2V voltage

7.3. HSSTLP hard core DC DC characteristic parameters

Table 7-3 HSSTLP hard core DC DC characteristics

Name	Min	Typical	Max	Unit	Condition	Description
Input and output signal DC characteristics						
HSST_V $_{DINPP}$	150	-	1000	mV	External AC AC Coupling	Differential input peak-to-peak voltage
HSST_VDIN _	0	-	HSSTAVCC	mV	DC coupled , HSSTAVCC=1V	Enter the absolute voltage value
HSST_V $_{INCM}$	-	3/4 HSSTAVCC	-	mV	DC coupled , HSSTAVCC=1V	Common mode input voltage value
HSST_V $_{DOUTPP}$	900	-	-	mV	Swing setting max	Differential output peak-to-peak power pressure
HSST_V $_{OUTCMDC}$	HSSTAVCC– DV $_{OUTPP}$ /4			mV	The DC common mode output voltage is the case when the transmitting end is floating	
HSST_V $_{OUTCMAC}$	1/2 HSSTAVCC			mV	Common mode output voltage value : external AC coupling	

HSST_R DIN	-	100	-	Ω	Differential input resistance
HSST_R DOUT	-	100	-	Ω	Differential output resistance
HSST_TX SKEW	-	-	14	ps	P -side and N -side skew of Tx output
HSST_C DEXT	-	100	-	nF	Recommended External AC Coupling Capacitor Values
Reference Clock Input DC Characteristics					
HSST_V RCLKPP	400	-	2000	mV	Differential input peak-to-peak voltage
HSST_R RCLK	-	100	-	Ω	Differential input resistance
HSST_C RCLKEXT	-	100	-	nF	Recommended External AC Coupling Capacitor Values

7.4. AC Characteristics of High Speed Serial Transceiver HSSTLP

AC characteristics of the HSSTLP hard core are shown in Table 7-6 to Table 7-11 .

Table 7-4 HSST hard core performance parameters

Name	Numerical value			Unit	Description
	- 5	- 6	- 7		
HSST_Fmax	6.6	6.6	TBD	Gbps	HSST maximum data rate
HSST_Fmin	0.6	0.6	TBD	Gbps	HSST minimum data rate
HSST_Fpllmax	6.6	6.6	TBD	GHz	HSST Maximum frequency of PLL
HSST_Fpllmin	1.6	1.6	TBD	GHz	HSST Minimum frequency of PLL

The HSSTLP reference clock switching characteristics are shown in the table below .

Table 7-5 HSSTLP Hard Reference Clock Switching Characteristics

Name	Numerical value			Unit	Condition	Description
	Min	Typical value	Max			
HSST_F REFCLK	60	-	330	MHz	Reference clock frequency range	
HSST_T RCLK	-	225	-	ps	20%- 80%	Reference Clock Rise Time
HSST_T FCLK	-	225	-	ps	80%- 20%	Reference clock fall time
HSST_T RATIO	45	50	55	%	PLL	Reference clock duty cycle

Table 7-6 HSSTLP hard core PLL/Lock lock time characteristics

Name	Numerical value			Unit	Condition	Description
	Min	Typical value	Max			
HSST_T PLLLOCK	-	-	1.5	ms		PLL lock time, time from reset release to lock
HSST_T CDRLOCK	-	60,000	2,500,000	UI	After the PLL is locked to the reference clock, and after switching to the external input data, the time for the CDR to lock	CDR lock time

HSST hard core user clock switch characteristics are shown in the table below

Table 7-7 HSSTLP Hard User Clock Switch Features

Name	Frequency	Unit	Description
Data Interface Clock Switch Characteristics			
HSST_F $_{T2C}$	206.25	MHz	Maximum frequency of P_CLK2CORE_TX
HSST_F $_{R2C}$	206.25	MHz	Maximum frequency of P_CLK2CORE_RX
HSST_F $_{TFC}$	206.25	MHz	Maximum frequency of P_TX_CLK_FR_CORE
HSST_F $_{RFC}$	206.25	MHz	Maximum frequency of P_RX_CLK_FR_CORE
APB Dynamic configuration interface clock switch characteristics			
HSST_F $_{APB}$	100	MHz	APB CLK maximum frequency

HSST hard core Transmitter transmit side switch characteristics are shown in the table below.

Table 7-8 HSSTLP hard core Transmitter transmit side switch characteristics

Name	Min	Typical	Max	Unit	Condition	Description
HSST_T $_{TXR}$	-	100	-	ps	20%- 80%	TX Rise Time
HSST_T $_{TXF}$	-	100	-	ps	80%- 20%	TX fall time
HSST_T $_{CHSKEW}$	-	-	500	ps	-	TX Skew between channels
HSST_V $_{TXIDLEAMP}$	-	-	30	mV	-	Electrical idle Amplitude
HSST_V $_{TXIDLETIME}$	-	-	150	ns	-	Electrical idle transition time
HSST_TJ $_{0.6G}$	-	-	0.1	UI	0.6Gbps	Total Jitter
HSST_DJ $_{0.6G}$	-	-	0.05	UI		Deterministic Jitter
HSST_TJ $_{1.25G}$	-	-	0.1	UI	1.25Gbps	Total Jitter
HSST_DJ $_{1.25G}$	-	-	0.05	UI		Deterministic Jitter
HSST_TJ $_{2.5G}$	-	-	0.2	UI	2.5Gbps	Total Jitter
HSST_DJ $_{2.5G}$	-	-	0.08	UI		Deterministic Jitter
HSST_TJ $_{3.125G}$	-	-	0.2	UI	3.125Gbps	Total Jitter
HSST_DJ $_{3.125G}$	-	-	0.08	UI		Deterministic Jitter
HSST_TJ $_{5.0G}$	-	-	0.3	UI	5.0Gbps	Total Jitter
HSST_DJ $_{5.0G}$	-	-	0.1	UI		Deterministic Jitter
HSST_TJ $_{6.6G}$	-	-	0.3	UI	6.6Gbps	Total Jitter
HSST_DJ $_{6.6G}$	-	-	0.1	UI		Deterministic Jitter

The switch characteristics of the receiving side of the HSST hard-core Receiver are shown in the following table

Table 7-9 Receiver side switch characteristics of HSSTLP hard core Receiver

Name	Minimum	Typical	Maximum	Unit	Description
HSST_T $_{RXIDLETIME}$	-		34	ns	RXELECIDLE state to LOS signal response time between
HSST_RX $_{VPPOOB}$	72	-	210	mV	OOB detection threshold peak-to-peak

HSST_RX TRACK	-5000	-	5000	ppm	Receiver spread spectrum follow, modulation frequency 33kHz
HSST_RX LENGTH	-	-	512	UI	Support RX continuous long 0 or long 1 length
HSST_RX TOLERANCE	-1250	-	1250	ppm	Frequency offset tolerance of data / reference clock
Sinusoidal Jitter Tolerance					
HSST_SJ_0.6	TBD	-	-	UI	Sinusoidal Jitter (1), 0.6Gbps
HSST_SJ_1.25	0.42	-	-	UI	Sinusoidal Jitter (1), 1.25Gbps
HSST_SJ_2.5	0.42	-	-	UI	Sinusoidal Jitter (1), 2.5Gbps
HSST_SJ_3.125	0.4	-	-	UI	Sinusoidal Jitter (1), 3.125Gbps
HSST_SJ_5.0	0.4	-	-	UI	Sinusoidal Jitter (1), 5.0Gbps
HSST_SJ_6.6	0.4	-	-	UI	Sinusoidal Jitter (1), 6.6Gbps

Note: 1. The frequency of the injected sinusoidal jitter is 10MHz

8. PCIe Hard Core Features

Table 8-1 PCIe performance parameters

Name	Numerical value	Unit	Description
Fpclk	250	MHz	PCIe Core maximum clock frequency
Fpclk_div2	125	MHz	User interface maximum clock frequency