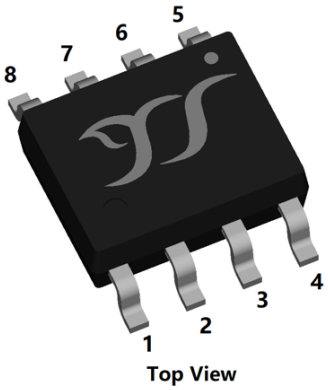
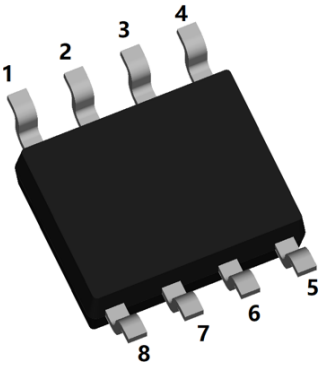
N-Channel and P-Channel Complementary Power MOSFET

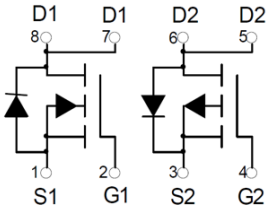


Top View



Bottom View

SOP-8



Product Summary

NMOS

- V_{DS} 30V
- I_D 7A
- $R_{DS(ON)}$(at VGS=10V) ＜18mohm
- $R_{DS(ON)}$(at VGS=4.5V) ＜30mohm

PMOS

- V_{DS} -30V
- I_D -7A
- $R_{DS(ON)}$(at VGS=-10V) ＜23mohm
- $R_{DS(ON)}$(at VGS=-4.5V) ＜34mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Wireless charger
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	±20	±20	V
Drain Current	T_A=25℃	I_D	7	-7	A
	T_A=70℃		5.6	-5.6	
Pulsed Drain Current [A]		I_{DM}	30	-42	A
Total Power Dissipation	T_A=25℃	P_D	1.9	1.9	W
	T_A=70℃		1.2	1.2	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	65.6	65.6	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS07NP03A	F2	Q07NP03	4000	8000	64000	13“ reel

■ N-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A		14	18	mΩ
		V_{GS}=4.5V, I_D=5A		23	30	
Diode Forward Voltage	V_{SD}	I_S=6A,V_{GS}=0V			1.2	V
Gate resistance	R_G	f=1MHz, Open drain	-	1	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	7	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		526		pF
Output Capacitance	C_{oss}			78		
Reverse Transfer Capacitance	C_{rss}			69		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=5.6A		12.22		nC
Gate-Source Charge	Q_{gs}			2.37		
Gate-Drain Charge	Q_{gd}			2.31		
Reverse Recovery Chrage	Q_{rr}	I_F=5.6A, di/dt=100A/us		1.28		
Reverse Recovery Time	t_{rr}			16.5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=15V, I_D=5.6A R_{GEN}=3Ω		5		
Turn-on Rise Time	t_r			28.2		
Turn-off Delay Time	$t_{D(off)}$			12.8		
Turn-off fall Time	t_f			21.6		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ P-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.0	-1.5	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-6A		18	23	mΩ
		V_{GS}=-4.5V, I_D=-5A		25	34	
Diode Forward Voltage	V_{SD}	I_S=-6A,V_{GS}=0V			-1.2	V
Gate resistance	R_G	f=1MHz, Open drain	-	8	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-7	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		1497		pF
Output Capacitance	C_{oss}			176		
Reverse Transfer Capacitance	C_{rss}			145		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-9A		28.5		nC
Gate-Source Charge	Q_{gs}			5.6		
Gate-Drain Charge	Q_{gd}			5.4		
Reverse Recovery Chrage	Q_{rr}	I_F=-9A, di/dt=100A/us		6		
Reverse Recovery Time	t_{rr}			14.2		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V, R_L=2Ω R_{GEN}=2.5Ω		9.7		
Turn-on Rise Time	t_r			43.9		
Turn-off Delay Time	$t_{D(off)}$			54.7		
Turn-off fall Time	t_f			58.9		

C. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

D. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ N-MOS Typical Performance Characteristics

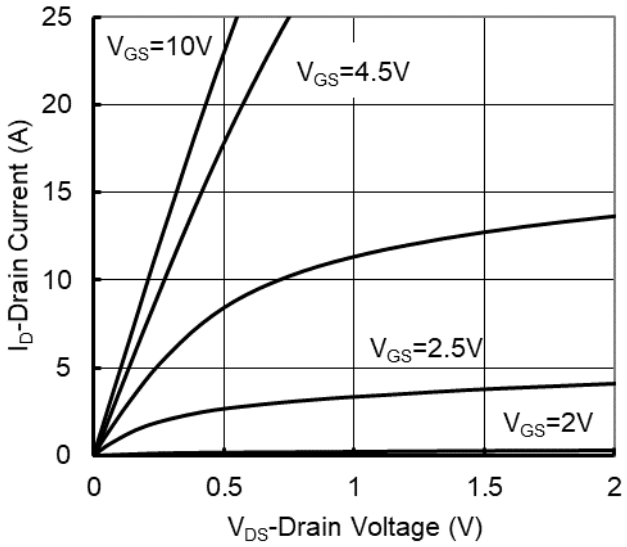


Figure1. Output Characteristics

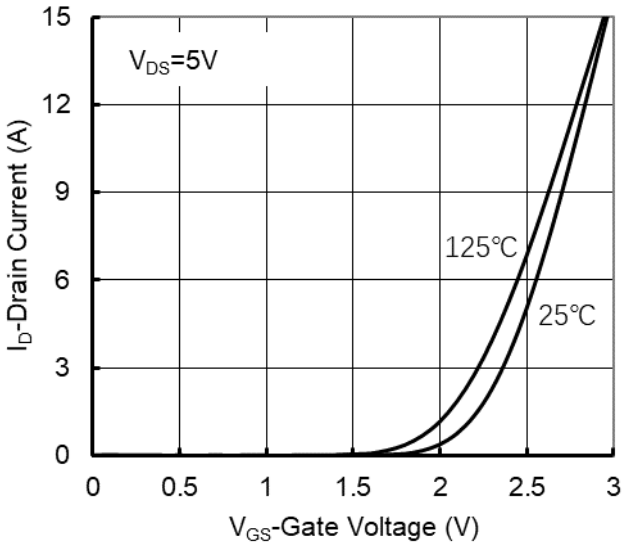


Figure2. Transfer Characteristics

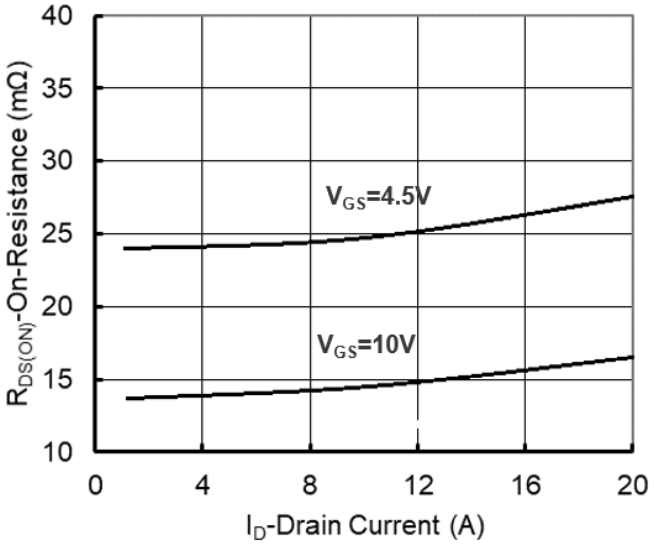


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

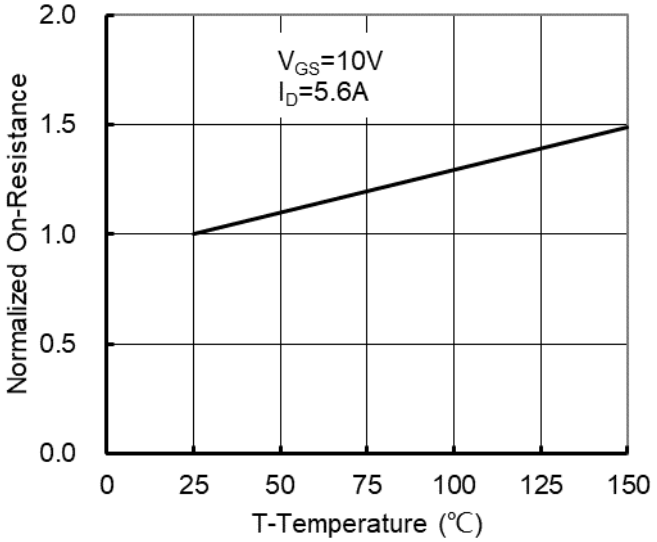


Figure 4: On-Resistance vs. Junction Temperature

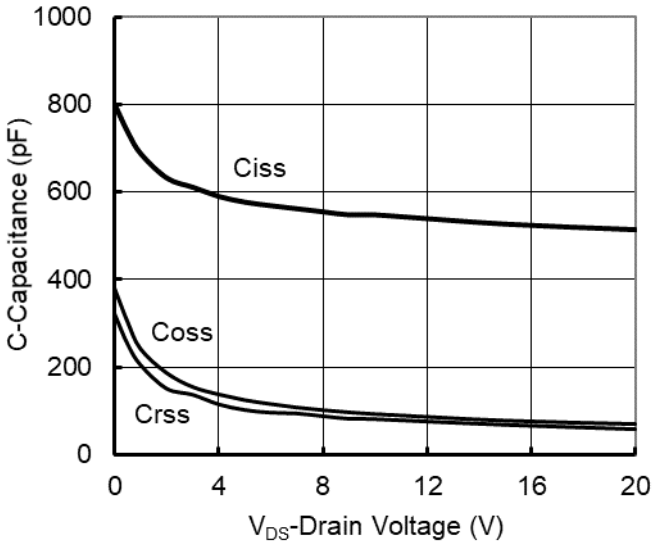


Figure5. Capacitance Characteristics

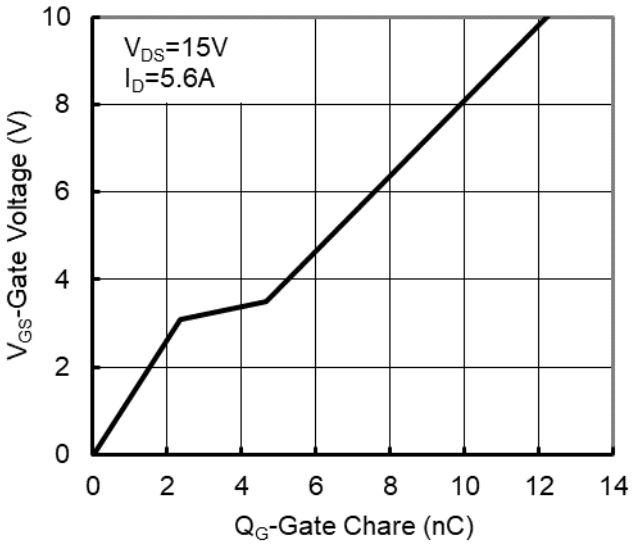


Figure6. Gate Charge

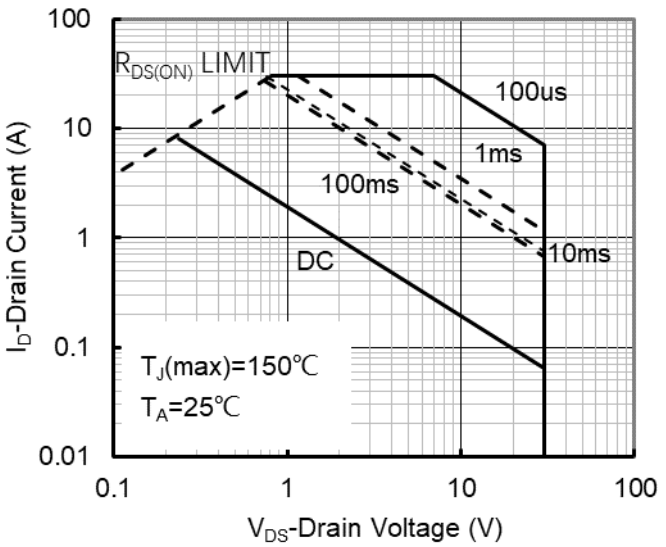


Figure7. Safe Operation Area

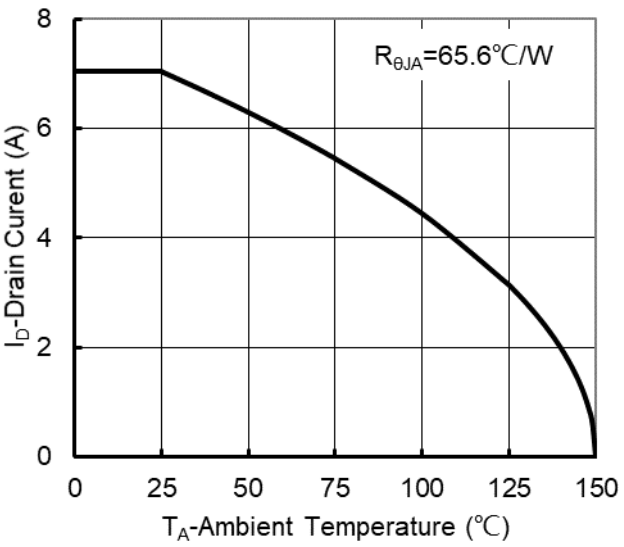


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

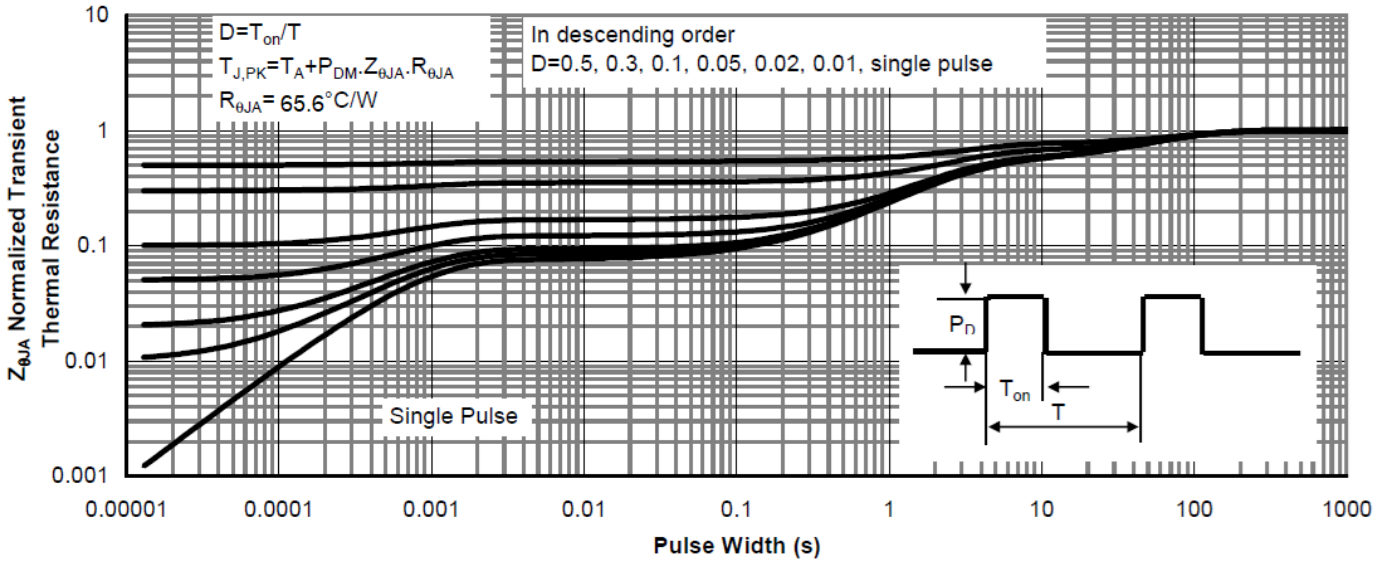


Figure9.Normalized Maximum Transient Thermal Impedance

■ P-MOS Typical Performance Characteristics

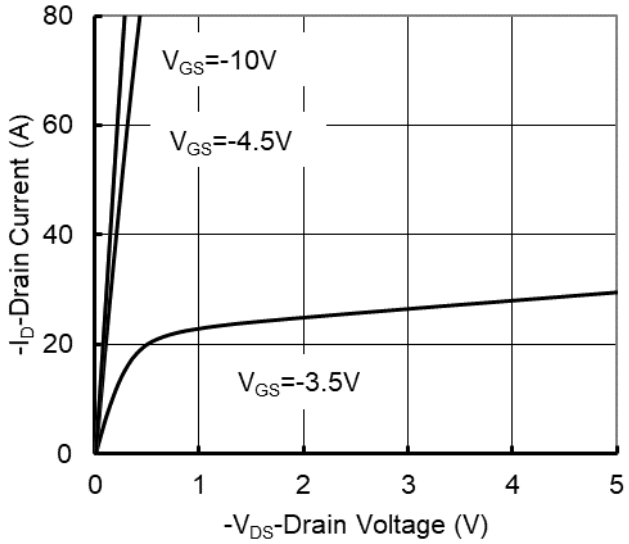


Figure1. Output Characteristics

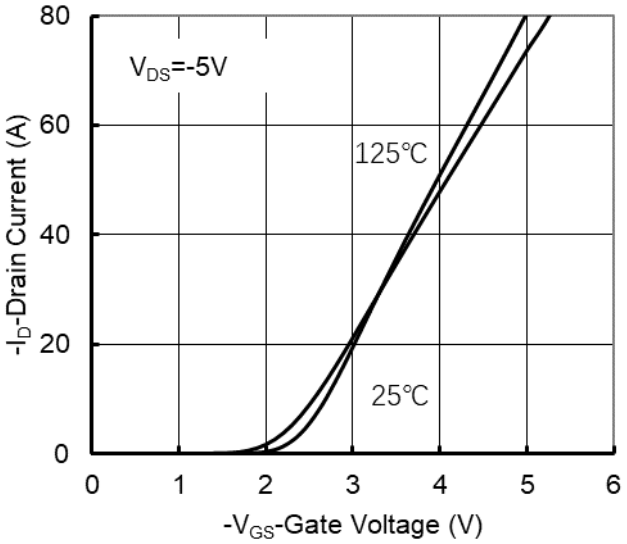


Figure2. Transfer Characteristics

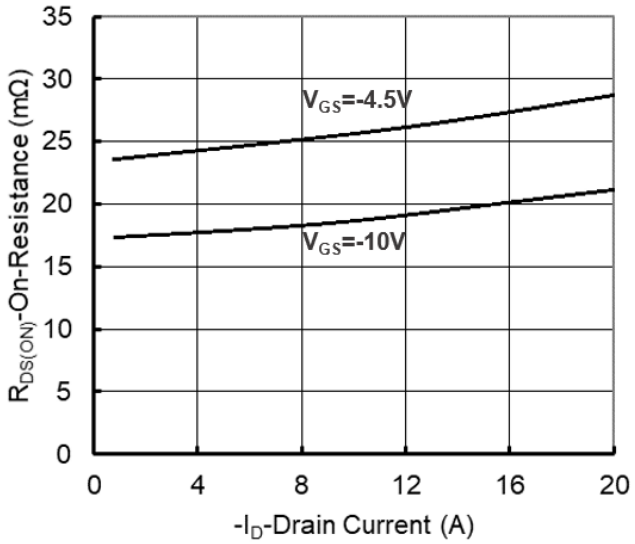


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

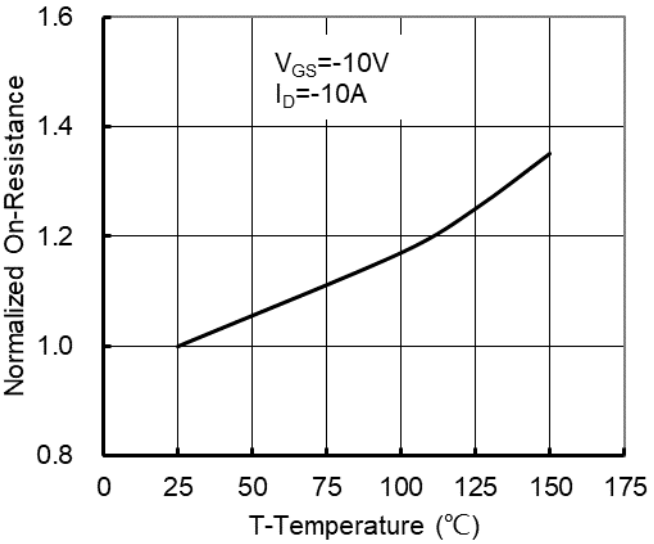


Figure 4: On-Resistance vs. Junction Temperature

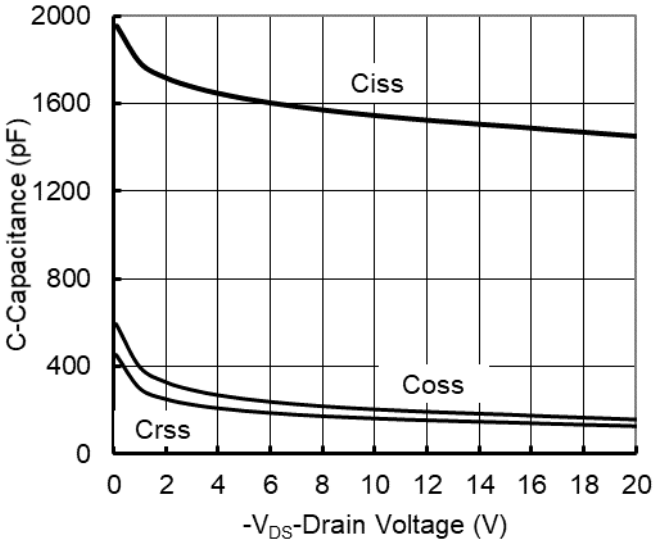


Figure5. Capacitance Characteristics

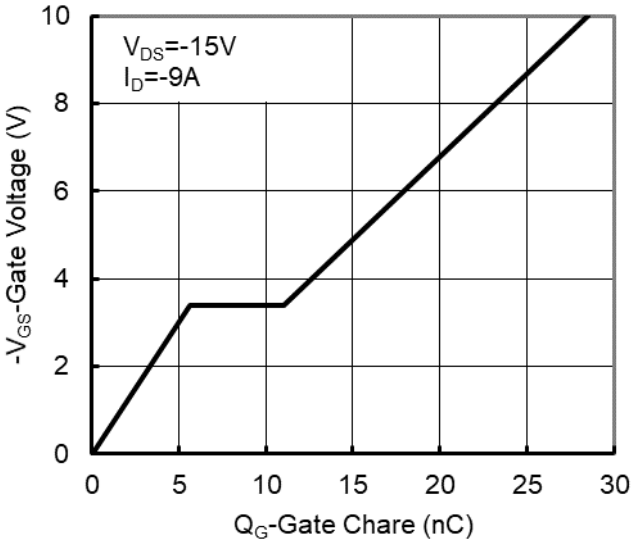


Figure6. Gate Charge

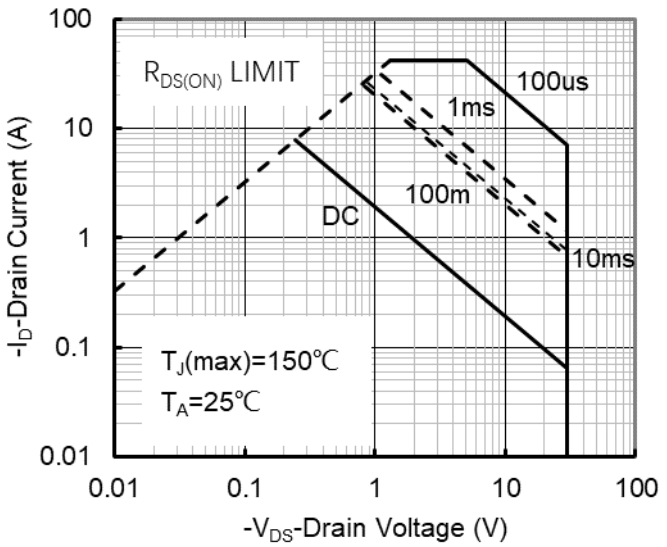


Figure7. Safe Operation Area

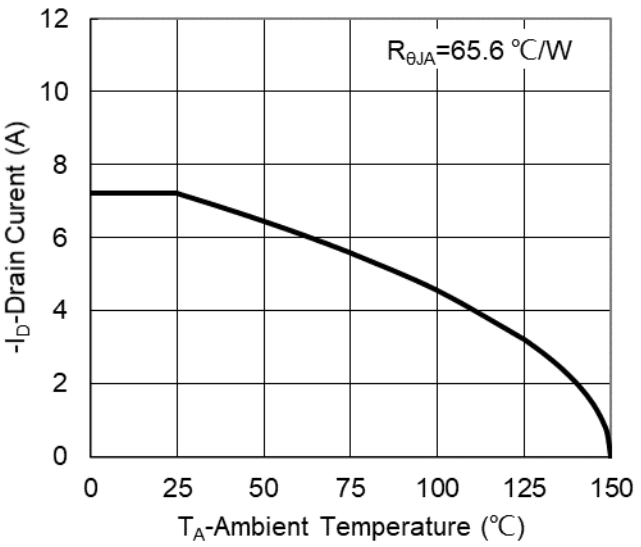


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

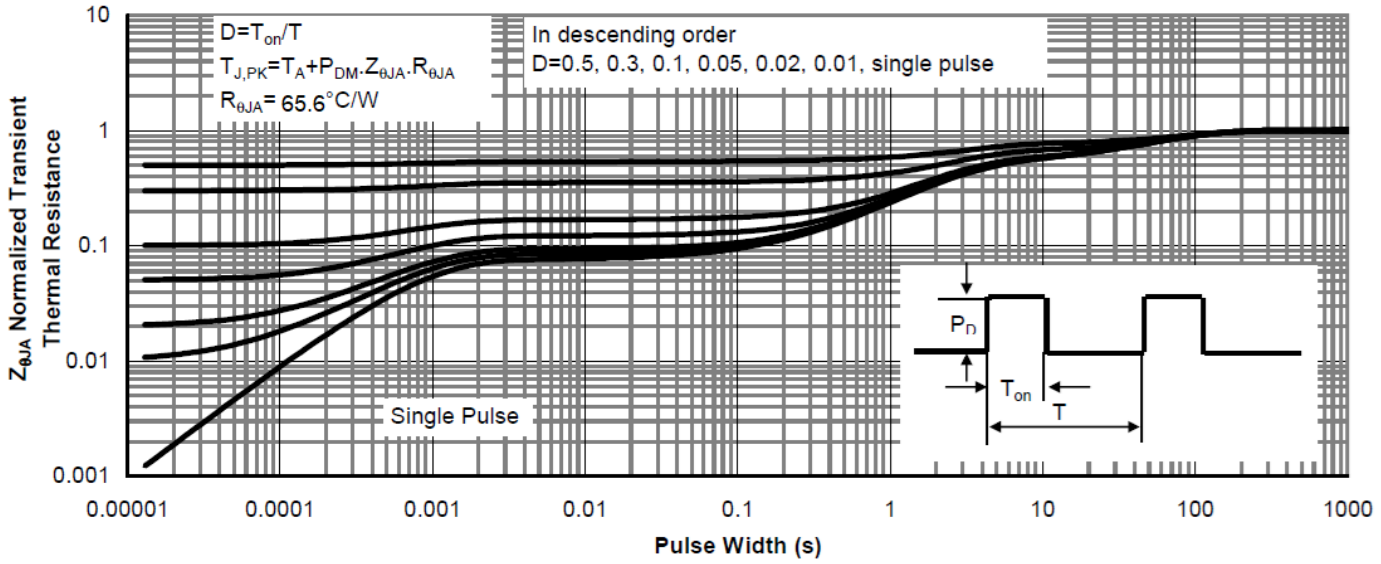
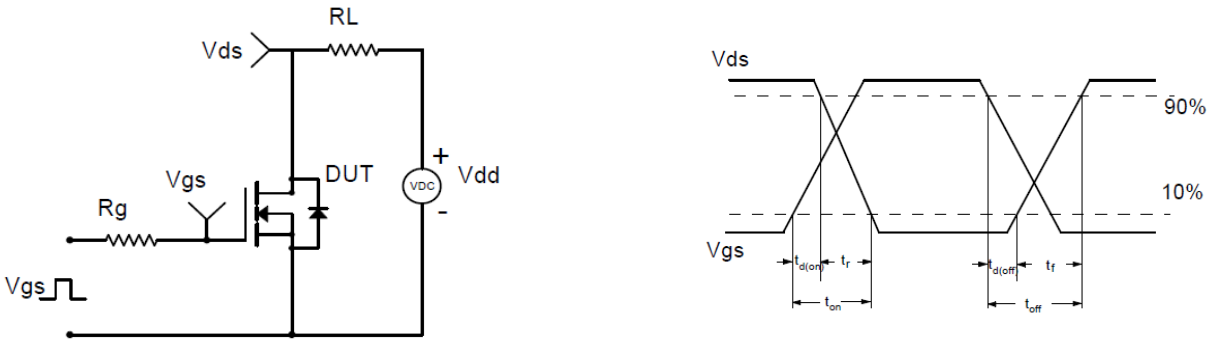
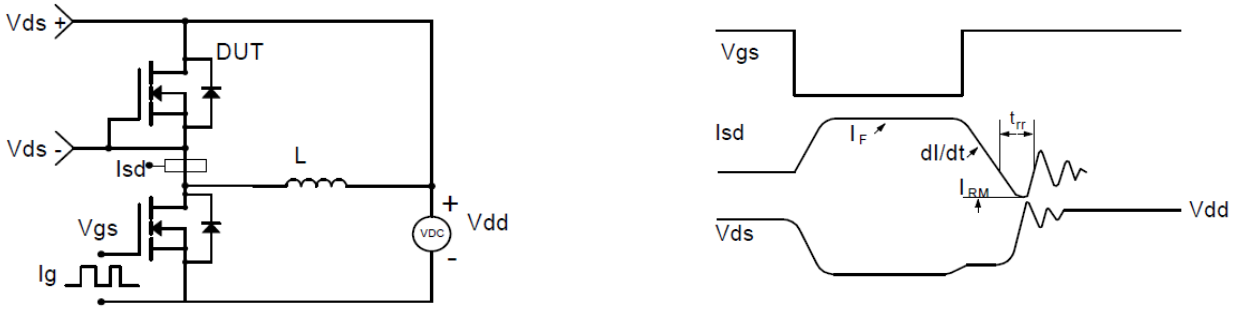


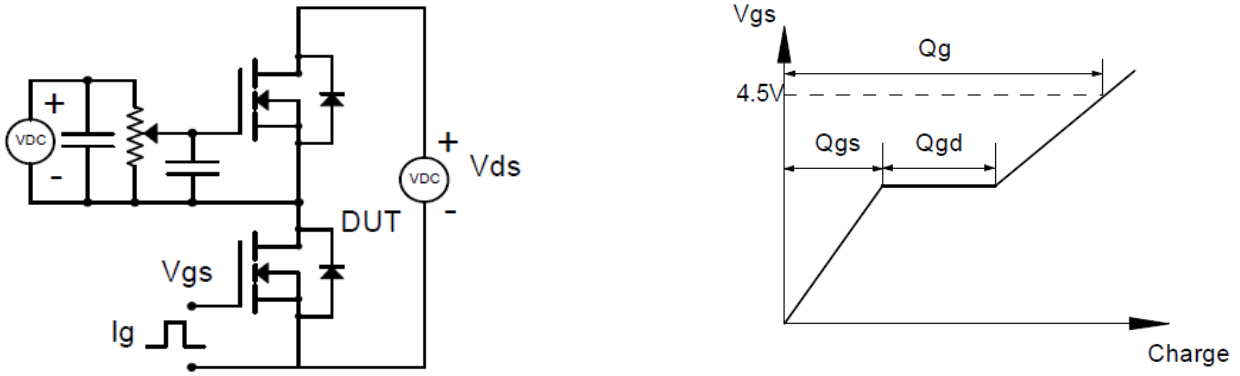
Figure9.Normalized Maximum Transient Thermal Impedance



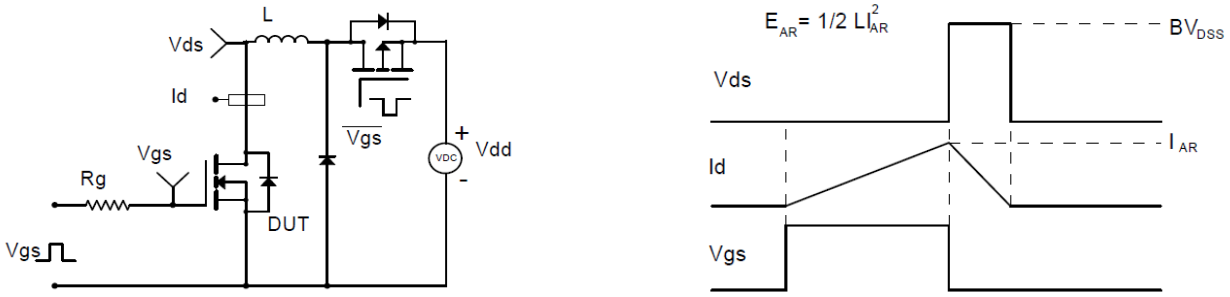
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

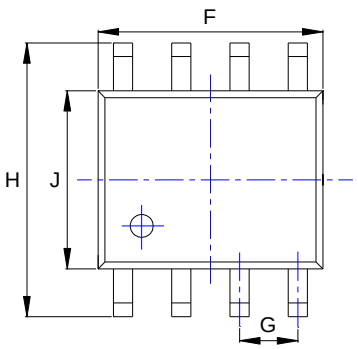


Gate Charge Test Circuit & Waveform

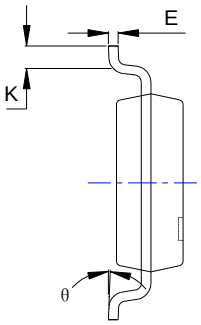


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

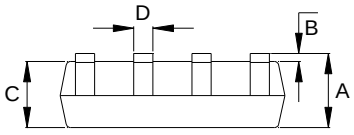
■ SOP-8 Package Information



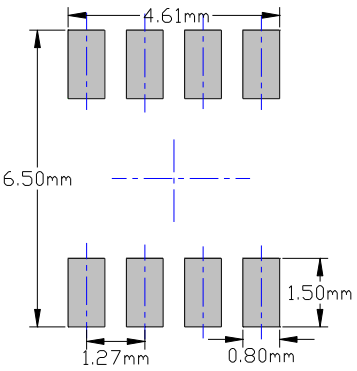
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

Disclaimer

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the specification of the products displayed herein to improve reliability, function or design or otherwise.

The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Yangjie or anyone on its behalf, assumes no responsibility or liability for any damages resulting from such improper use of sale.

This publication supersedes & replaces all information previously supplied. For additional information, please visit our website http:// www.21yangjie.com , or consult your nearest Yangjie's sales office for further assistance.