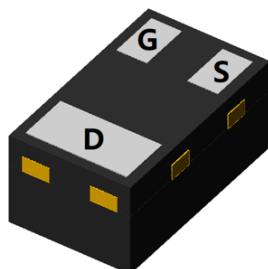


N-Channel Enhancement Mode Field Effect Transistor

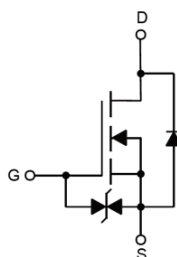


Top View



Bottom View

DFN1006-3L



Product Summary

- V_{DS} 60V
- I_D 260mA
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.5\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<3.0\Omega$
- ESD Protected Up to 2.0KV (HBM)

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface: TTL/CMOS

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$ @ Steady State	I_D	260	mA
	$T_A=70^\circ\text{C}$ @ Steady State		210	
Pulsed Drain Current ^A		I_{DM}	1.3	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$		P_D	200	mW
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JA}$	600	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
2N7002KCL3	F1	7 • 2	10000	100000	400000	7" reel



2N7002KCL3

■ Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}= \pm 20V, V_{DS}=0V$			± 10	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}= V_{GS}, I_D=250\mu A$	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}= 10V, I_D=260mA$		1.9	2.5	Ω
		$V_{GS}= 4.5V, I_D=200mA$		2.0	3.0	
Diode Forward Voltage	V_{SD}	$I_S=260mA, V_{GS}=0V$		0.9	1.2	V
Maximum Body-Diode Continuous Current	I_S				260	mA
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=0.26A$		0.13		S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V, f=1MHz$		21		pF
Output Capacitance	C_{oss}			9		
Reverse Transfer Capacitance	C_{rss}			4		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=30V, I_D=0.26A$		1.22		nC
Gate-Source Charge	Q_{gs}			0.5		
Gate-Drain Charge	Q_{gd}			0.18		
Reverse Recovery Charge	Q_{rr}	$V_{GS}=0V, I_S=260mA, V_R=25V, di/dt=100A/\mu s$		3.6		
Reverse Recovery Time	t_{rr}			16		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=50V, I_D=260mA, R_{GEN}=50\Omega$		7		ns
Turn-on Rise Time	t_r			19		
Turn-off Delay Time	$t_{D(off)}$			20		
Turn-off fall Time	t_f			84		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.



■ Typical Performance Characteristics

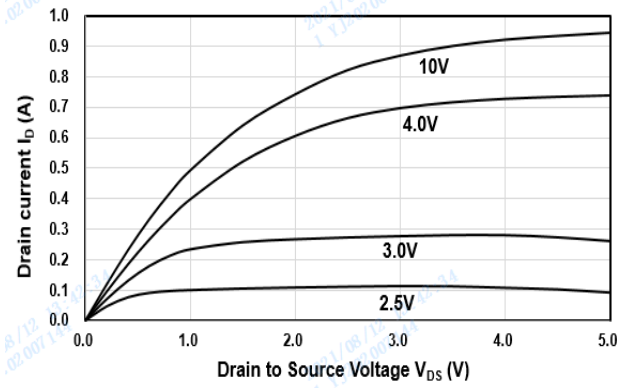


Figure1. Output Characteristics

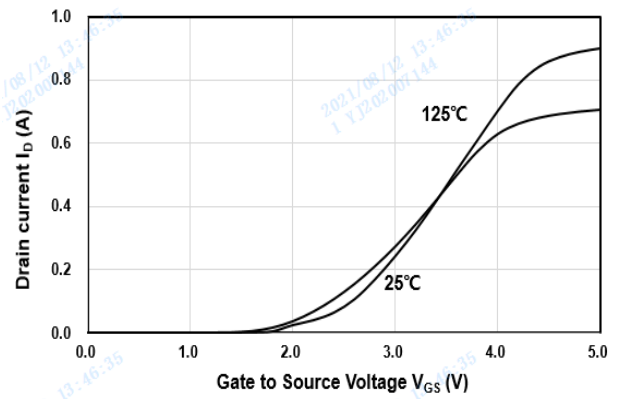


Figure2. Transfer Characteristics

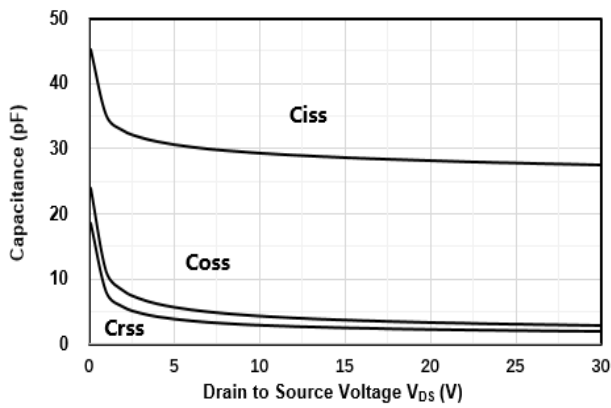


Figure3. Capacitance Characteristics

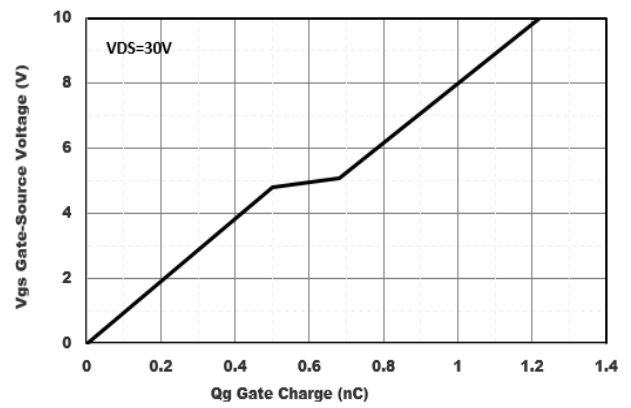


Figure4. Gate Charge

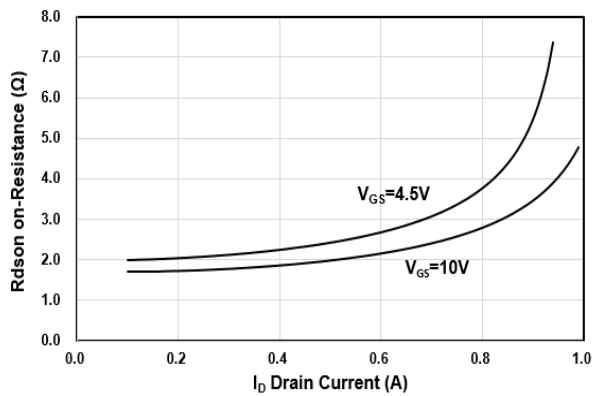


Figure5. Drain-Source on Resistance

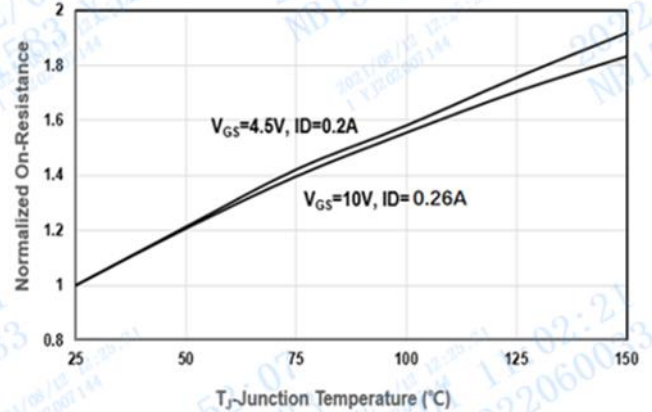


Figure6. Drain-Source on Resistance



2N7002KCL3

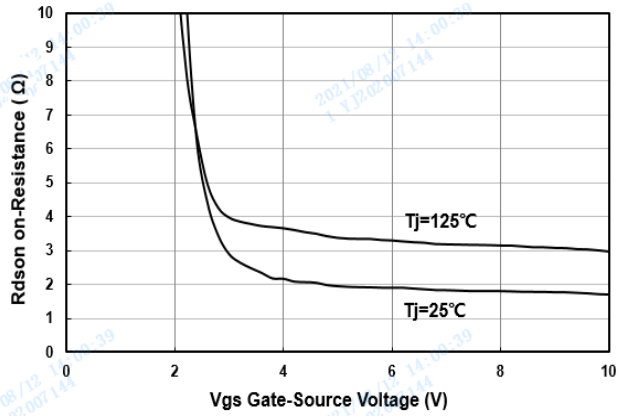


Figure7. On-Resistance vs V_{GS}

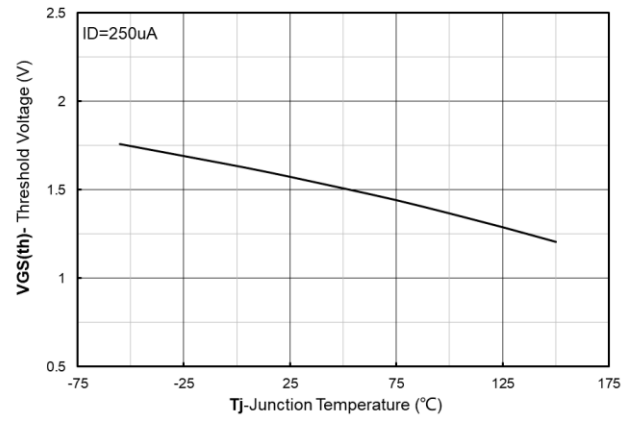


Figure8. Threshold Voltage vs Temperature

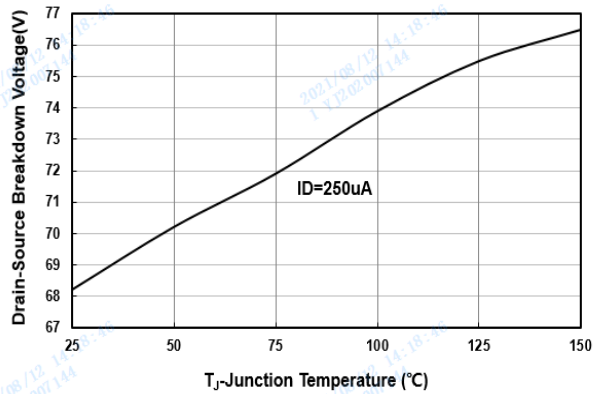


Figure9. Breakdown Voltage vs Temperature

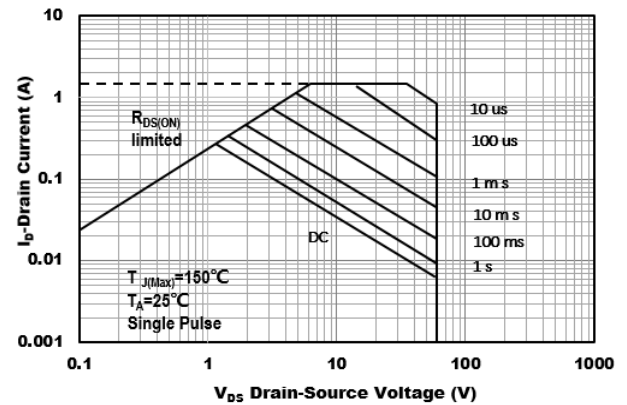


Figure10. Safe Operation Area

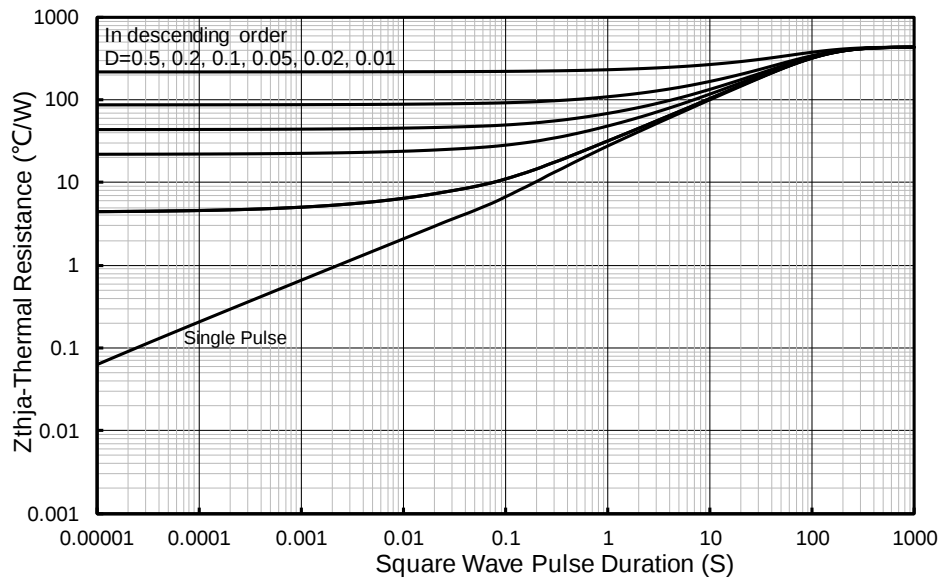
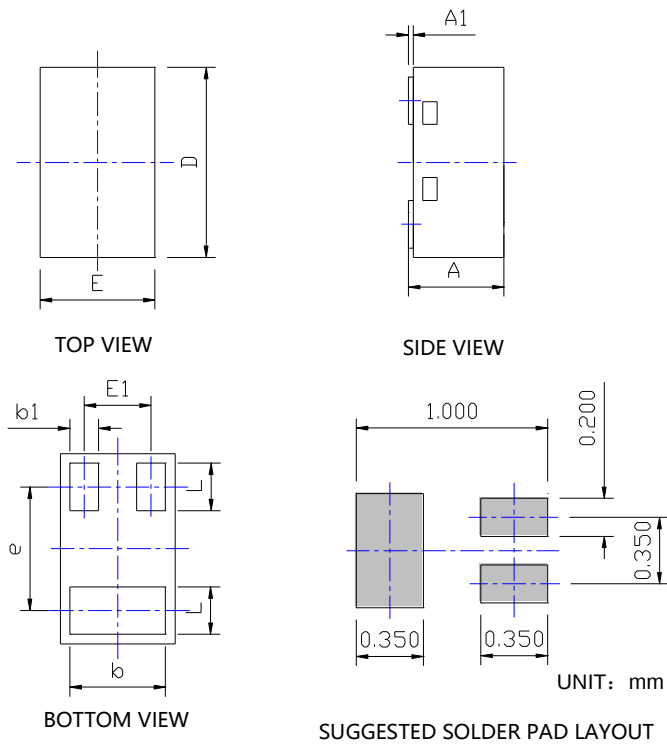


Figure11. Maximum Transient Thermal Impedance



2N7002KCL3

■ DFN1006-3L Package information



SYMBOL	DIMENSIONS		
	Millimeter		
	MIN.	NOM.	MAX.
A	0.42	---	0.55
A1	0.025REF		
b	0.45	0.50	0.55
b1	0.10	0.15	0.20
D	0.95	1.00	1.05
E	0.55	0.60	0.65
E1	0.35BSC		
e	0.65BSC		
L	0.20	0.25	0.30

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE LEAD BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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