

$V_{\text{DRM}} = 5200 \text{ V}$
 $I_{\text{T(AV)M}} = 5200 \text{ A}$
 $I_{\text{T(RMS)}} = 8170 \text{ A}$
 $I_{\text{TSM}} = 99.0 \cdot 10^3 \text{ A}$
 $V_{\text{T0}} = 1.04 \text{ V}$
 $r_{\text{T}} = 0.115 \text{ m}\Omega$

Phase Control Thyristor

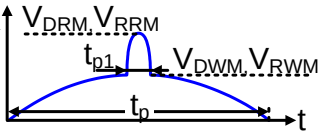
5STP 52U5200

Doc. No. 5SYA1042-07 Apr. 20

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

Blocking

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	5STP 52U5200	Unit
Max. surge peak forward and reverse blocking voltage	$V_{\text{DSM}}, V_{\text{RSM}}$	$t_p = 10 \text{ ms}, f = 5 \text{ Hz}$ $T_{\text{vj}} = 5 \dots 125 \text{ }^\circ\text{C}$, Note 1	5200	V
Max repetitive peak forward and reverse blocking voltage	$V_{\text{DRM}}, V_{\text{RRM}}$	$f = 50 \text{ Hz}, t_p = 10 \text{ ms}, t_{p1} = 250 \text{ }\mu\text{s}$, $T_{\text{vj}} = 5 \dots 125 \text{ }^\circ\text{C}$, Note 1, Note 2	5200	V
Max crest working forward and reverse voltages	$V_{\text{DWM}}, V_{\text{RWM}}$		3470	V
Critical rate of rise of commutating voltage	dv/dt_{crit}	Exp. to $0.67 \cdot V_{\text{DRM}}, T_{\text{vj}} = 125 \text{ }^\circ\text{C}$	2000	V/ μs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DRM}	$V_{\text{DRM}}, T_{\text{vj}} = 125 \text{ }^\circ\text{C}$			800	mA
Reverse leakage current	I_{RRM}	$V_{\text{RRM}}, T_{\text{vj}} = 125 \text{ }^\circ\text{C}$			800	mA

Note 1: Voltage de-rating factor of 0.11% per $^\circ\text{C}$ is applicable for T_{vj} below $+5 \text{ }^\circ\text{C}$.

Note 2: Recommended minimum ratio of $V_{\text{DRM}} / V_{\text{DWM}}$ or $V_{\text{RRM}} / V_{\text{RWM}} = 2$. See App. Note 5SYA 2051.

Mechanical data

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_{M}		120	135	160	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				3.6	kg
Housing thickness	H	$F_{\text{M}} = 135 \text{ kN}, T_{\text{a}} = 25 \text{ }^\circ\text{C}$	34.57		35.22	mm
Surface creepage distance	D_{S}		56			mm
Air strike distance	D_{a}		22			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

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On-state

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, $T_c = 70\text{ °C}$			5200	A
RMS on-state current	$I_{T(RMS)}$				8170	A
Peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_{vj} = 125\text{ °C}$, sine half wave, $V_D = V_R = 0\text{ V}$, after surge			$99.0 \cdot 10^3$	A
Limiting load integral	I^2t				$49.0 \cdot 10^6$	A ² s
Peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_{vj} = 125\text{ °C}$, sine half wave, $V_R = 0.6 \cdot V_{RRM}$, after surge			$78.0 \cdot 10^3$	A
Limiting load integral	I^2t				$30.4 \cdot 10^6$	A ² s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	$I_T = 3000\text{ A}$, $T_{vj} = 125\text{ °C}$		1.26	1.38	V
Threshold voltage	$V_{(TO)}$	$I_T = 2000\text{ A} - 6000\text{ A}$, $T_{vj} = 125\text{ °C}$			1.04	V
Slope resistance	r_T				0.115	mΩ
Holding current	I_H	$T_{vj} = 25\text{ °C}$			200	mA
		$T_{vj} = 125\text{ °C}$			100	mA
Latching current	I_L	$T_{vj} = 25\text{ °C}$			900	mA
		$T_{vj} = 125\text{ °C}$			700	mA

Switching

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	$T_{vj} = 125\text{ °C}$, $I_T = 3000\text{ A}$, $V_D \leq 0.67 \cdot V_{DRM}$, $I_{GM} = 2\text{ A}$, $t_r = 0.5\text{ μs}$	Cont. $f = 50\text{ Hz}$		250	A/μs
			Cont. $f = 1\text{ Hz}$		1000	A/μs
Circuit-commutated turn-off time	t_q	$T_{vj} = 125\text{ °C}$, $I_T = 2000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1.5\text{ A/μs}$, $V_D \leq 0.67 \cdot V_{DRM}$, $dv_D/dt = 20\text{ V/μs}$			940	μs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery charge	Q_{rr}	$T_{vj} = 125\text{ °C}$, $I_T = 2000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1.5\text{ A/μs}$	3000	5720	8000	μAs
Reverse recovery current	I_{RM}		55	86	95	A
Gate turn-on delay time	t_{gd}	$T_{vj} = 25\text{ °C}$, $V_D = 0.4 \cdot V_{RM}$, $I_{GM} = 2\text{ A}$, $t_r = 0.5\text{ μs}$			3	μs

Triggering

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$		see Fig. 7			W

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	$T_{vj} = 25\text{ °C}$			2.6	V
Gate-trigger current	I_{GT}	$T_{vj} = 25\text{ °C}$			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \cdot V_{DRM}$, $T_{vjmax} = 125\text{ °C}$			0.3	V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \cdot V_{DRM}$, $T_{vjmax} = 125\text{ °C}$			10	mA

Thermal

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				125	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled $F_m = 120... 160\text{ kN}$			4	K/kW
	$R_{th(j-c)A}$	Anode-side cooled $F_m = 120... 160\text{ kN}$			8	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled $F_m = 120... 160\text{ kN}$			8	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled $F_m = 120... 160\text{ kN}$			0.8	K/kW
	$R_{th(c-h)}$	Single-side cooled $F_m = 120... 160\text{ kN}$			1.6	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^n R_i (1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/kW)	2.698	0.817	0.356	0.129
τ_i (s)	0.9526	0.1217	0.0127	0.0028

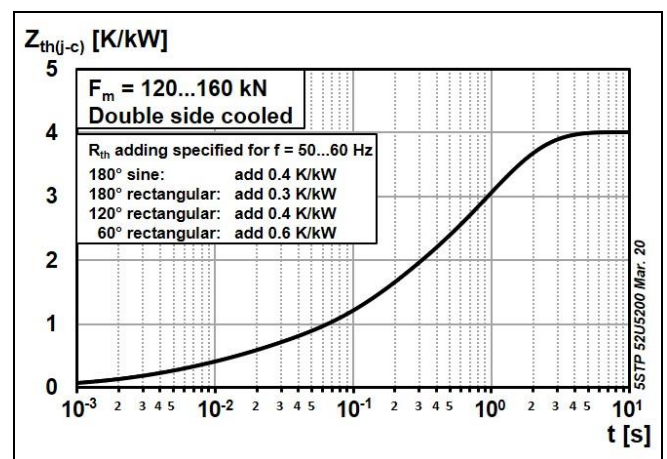
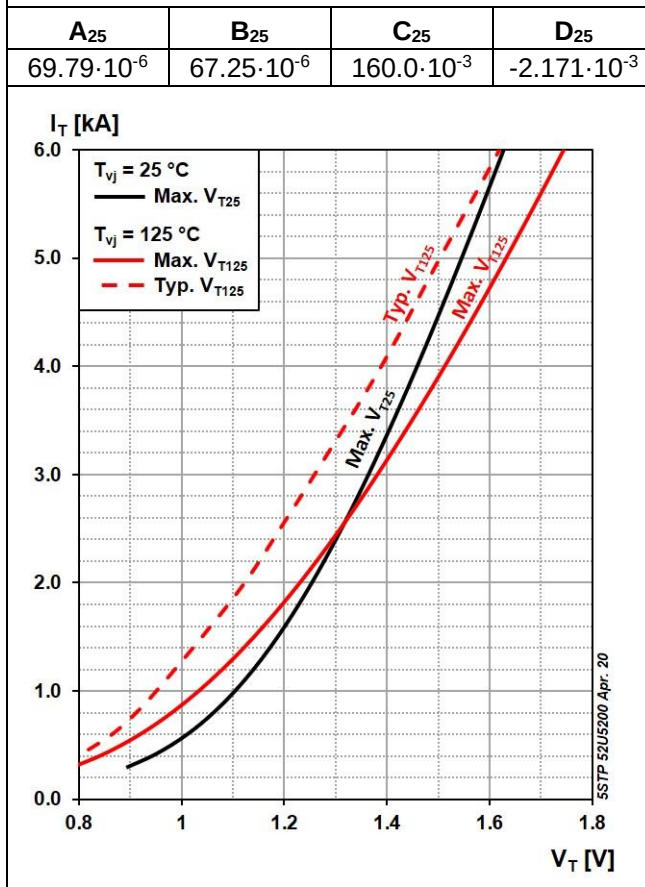


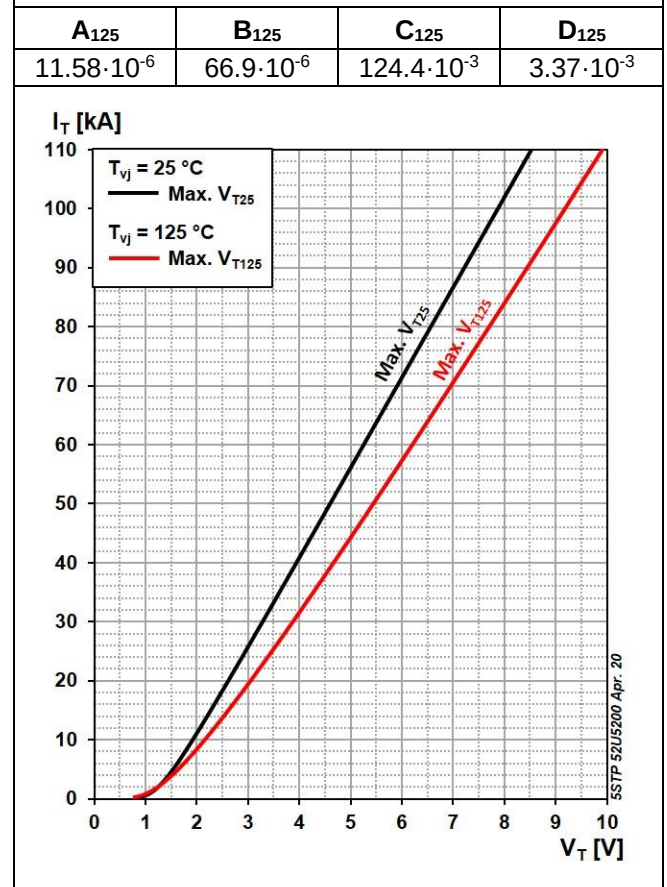
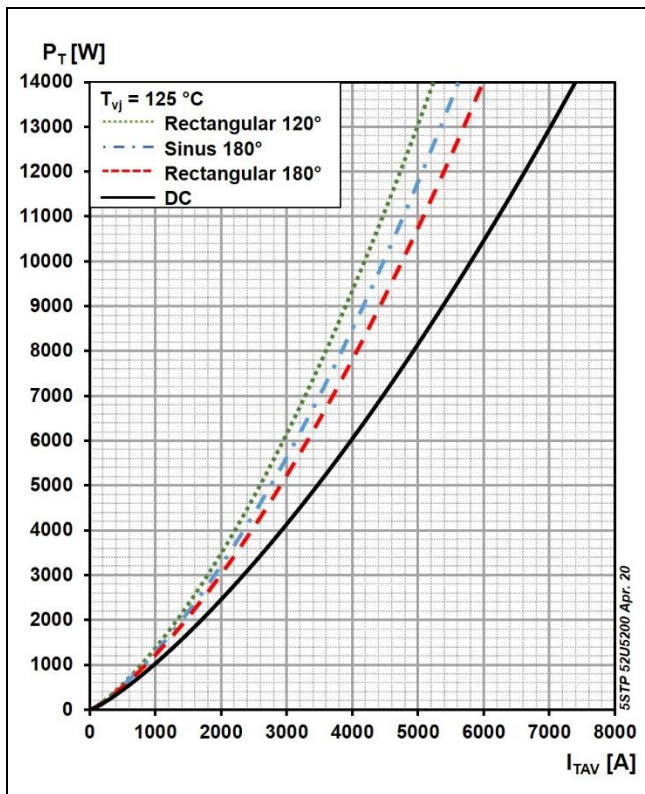
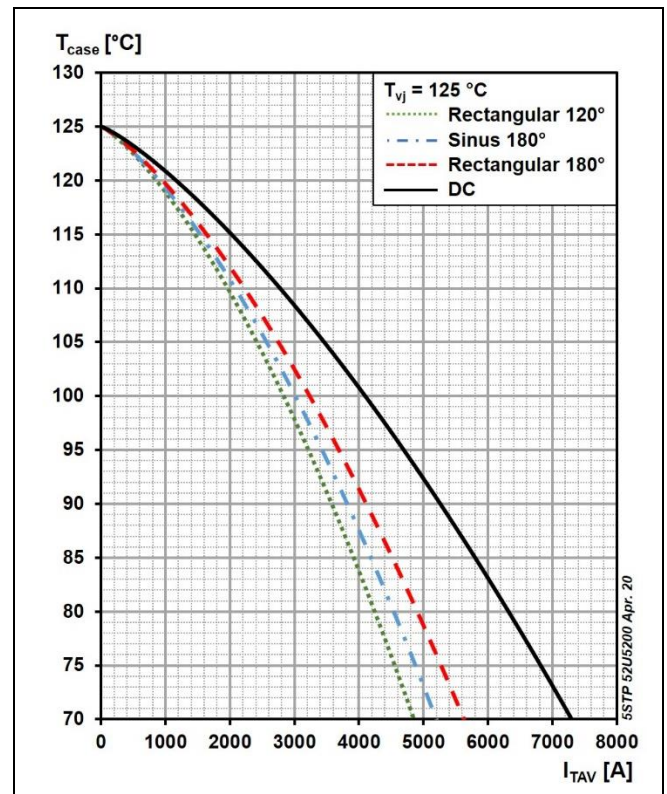
Fig. 1 Transient thermal impedance (junction-to-case) vs. time

Max. on-state characteristic model:

$$V_{T25} = A_{TVj} + B_{TVj} \cdot I_T + C_{TVj} \cdot \ln(I_T + 1) + D_{TVj} \cdot \sqrt{I_T}$$

Valid for $I_T = 300 - 110000$ A**Fig. 2** On-state voltage characteristics**Max. on-state characteristic model:**

$$V_{T125} = A_{TVj} + B_{TVj} \cdot I_T + C_{TVj} \cdot \ln(I_T + 1) + D_{TVj} \cdot \sqrt{I_T}$$

Valid for $I_T = 300 - 110000$ A**Fig. 3** On-state voltage characteristics**Fig. 4** On-state power dissipation vs. mean on-state current, turn-on losses excluded**Fig. 5** Max. permissible case temperature vs. mean on-state current, switching losses ignored

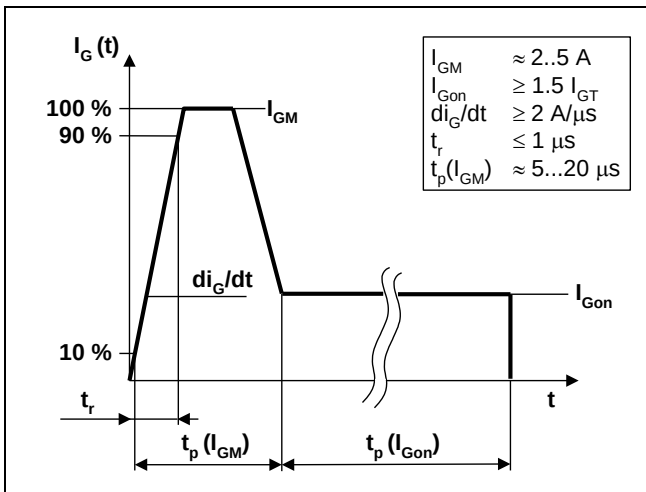


Fig. 6 Recommended gate current waveform

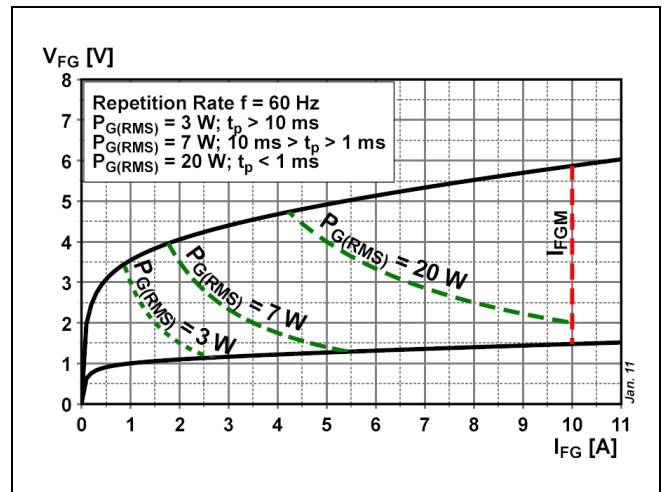


Fig. 7 Max. peak gate power loss

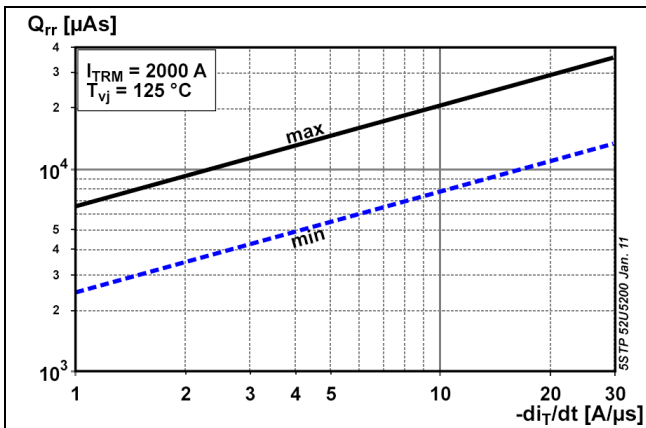


Fig. 8 Reverse recovery charge vs. decay rate of on-state current

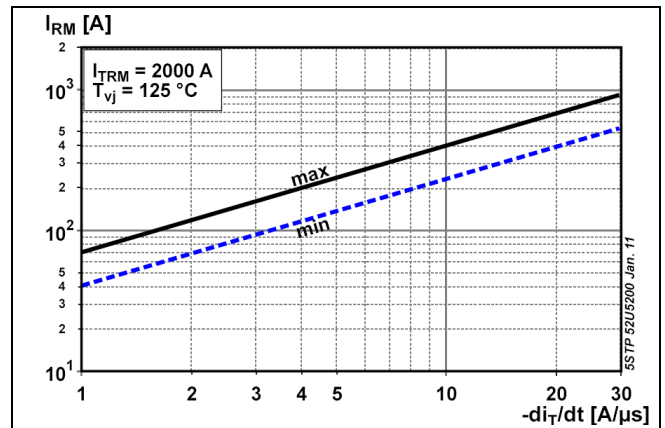


Fig. 9 Peak reverse recovery current vs. decay rate of on-state current

Turn-on and Turn-off losses

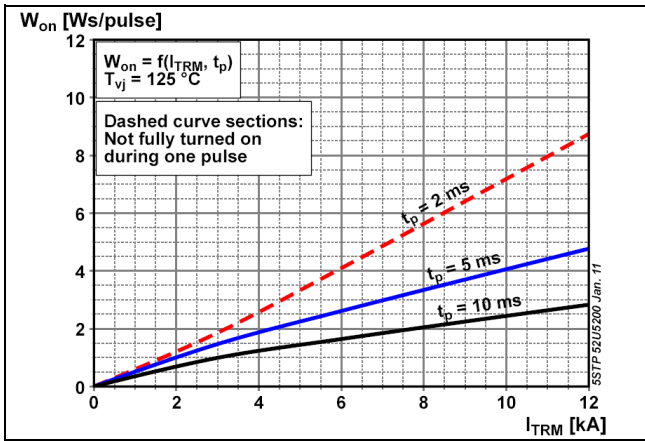


Fig. 10 Turn-on energy, half sinusoidal waves

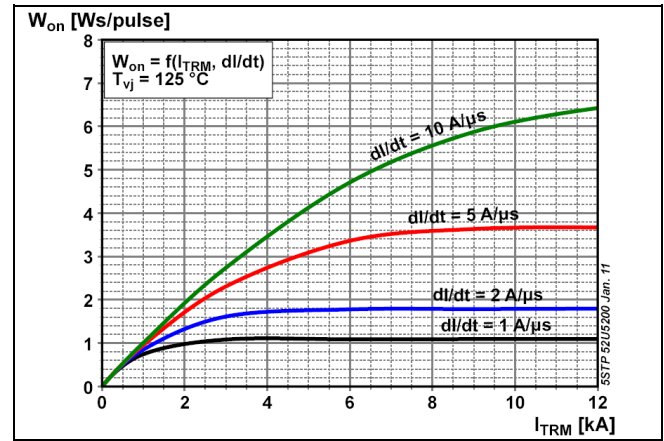


Fig. 11 Turn-on energy, rectangular waves

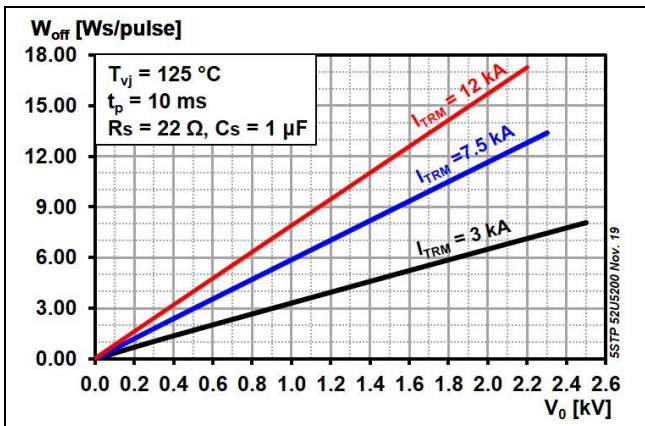


Fig. 12 Typical turn-off energy, half sinusoidal waves

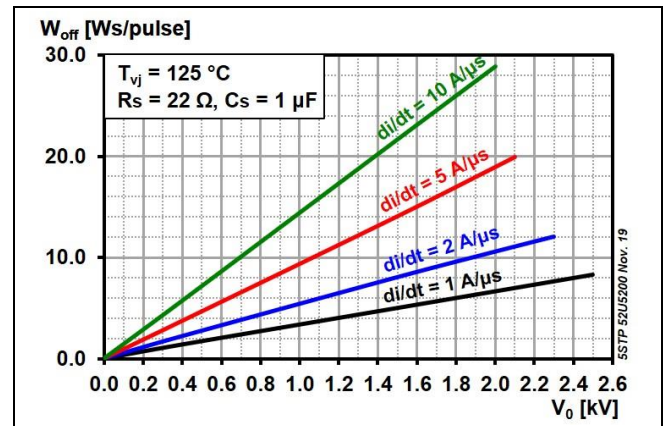


Fig. 13 Typical turn-off energy, rectangular waves

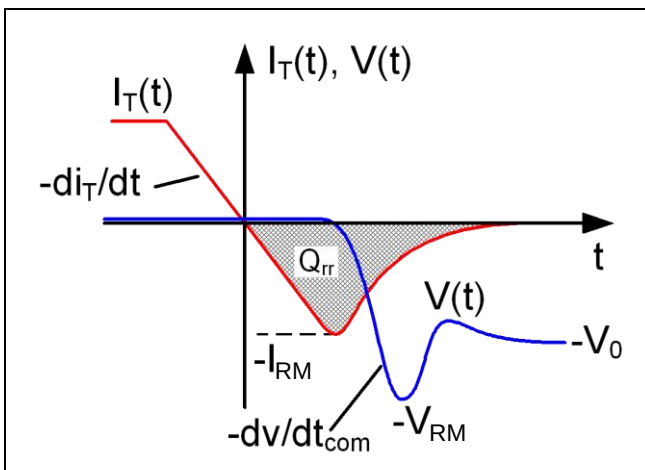


Fig. 14 Current and voltage waveforms at turn-off

Total power loss for repetitive waveforms:

$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

where

$$P_T = \frac{1}{T} \int_0^T I_T \cdot V_T(I_T) dt$$

Fig. 15 Relationships for power loss

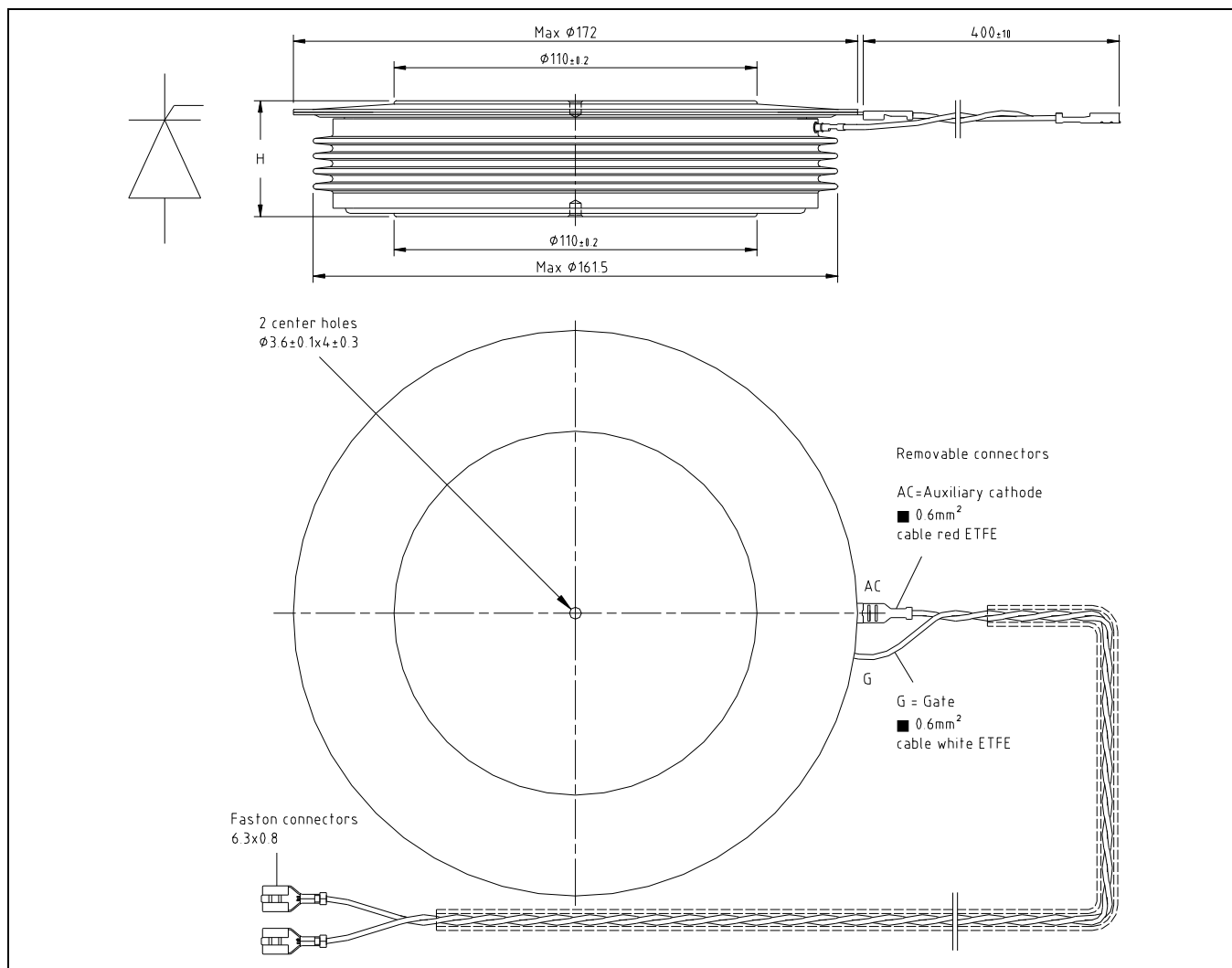


Fig. 16 Device Outline Drawing

Related documents:

5SYA 2020	Design of RC-Snubbers for Phase Control Applications
5SYA 2049	Voltage definitions for phase control and bi-directionally controlled thyristors
5SYA 2051	Voltage ratings of high power semiconductors
5SYA 2034	Gate-drive recommendations for phase control and bi-directionally controlled thyristors
5SYA 2036	Recommendations regarding mechanical clamping of Press-Pack High Power Semiconductors
5SYA 2102	Surge currents for Phase Control Thyristors
5SZK 9118	General Environmental Conditions for High Power Semiconductors

Please refer to <http://www.abb.com/semiconductors> for current version of documents.

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