

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

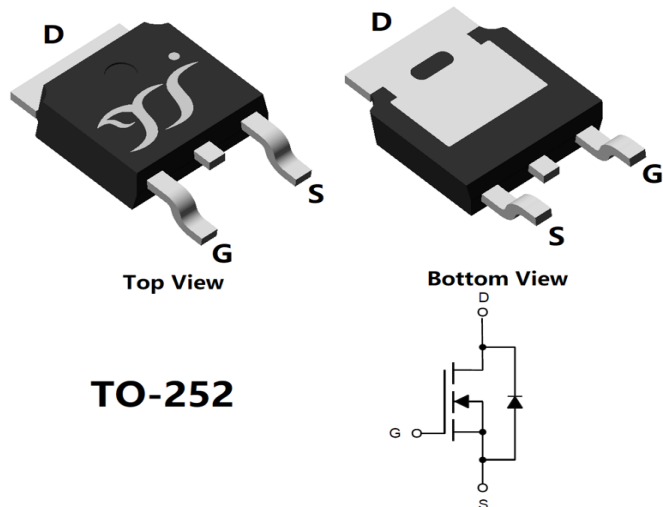
- V_{DS} 100V
- I_D 45A
- $R_{DS(on)}$ (at $V_{GS}=10V$) <17 mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-252

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	7.5	A
	$T_A=100^\circ\text{C}$		4.5	
	$T_C=25^\circ\text{C}$		45	
	$T_C=100^\circ\text{C}$		28.5	
Pulsed Drain Current ^A		I_{DM}	180	A
Avalanche energy ^B		EAS	81	mJ
Total Power Dissipation ^C	$T_A=25^\circ\text{C}$	P_D	2.5	W
	$T_A=100^\circ\text{C}$		1	
	$T_C=25^\circ\text{C}$		72	
	$T_C=100^\circ\text{C}$		28.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10S$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.35	1.7	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD45G10B	F1/F2	YJD45G10B	2500	/	25000	13"Reel



YJD45G10B

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2	2.8	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		14	17	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A,V _{GS} =0V			1.3	V
Maximum Body-Diode Continuous Current	I _S				45	A
Gate resistance	R _G	f= 1 MHz, Open drain		1		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V,V _{GS} =0V,f=1MHZ		1135		pF
Output Capacitance	C _{oss}			399		
Reverse Transfer Capacitance	C _{rss}			18		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V,V _{DS} =50V,I _D =25A		16		nC
Gate-Source Charge	Q _{gs}			5.6		
Gate-Drain Charge	Q _{gd}			2.4		
Reverse Recovery Chrage	Q _{rr}	I _F =20A, di/dt=100A/us		42		
Reverse Recovery Time	t _{rr}			39.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V,I _D =25A R _{GEN} =2.2Ω		39.2		ns
Turn-on Rise Time	t _r			11		
Turn-off Delay Time	t _{D(off)}			53.2		
Turn-off fall Time	t _f			15.8		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=0.5mH, I_{AS}=18A,.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation PDSM is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



■ Typical Performance Characteristics

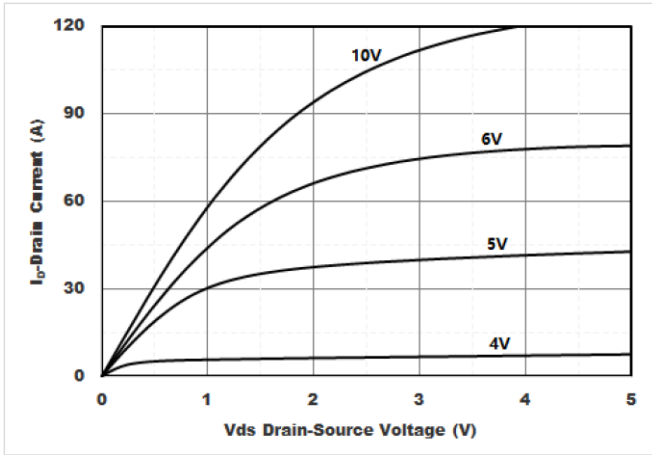


Figure1. Output Characteristics

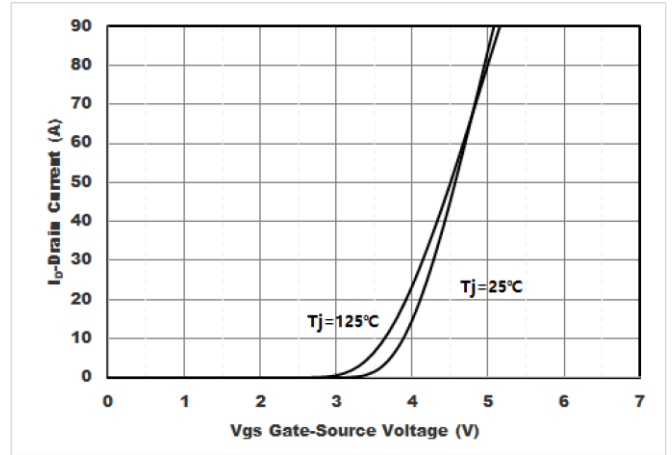


Figure2. Transfer Characteristics

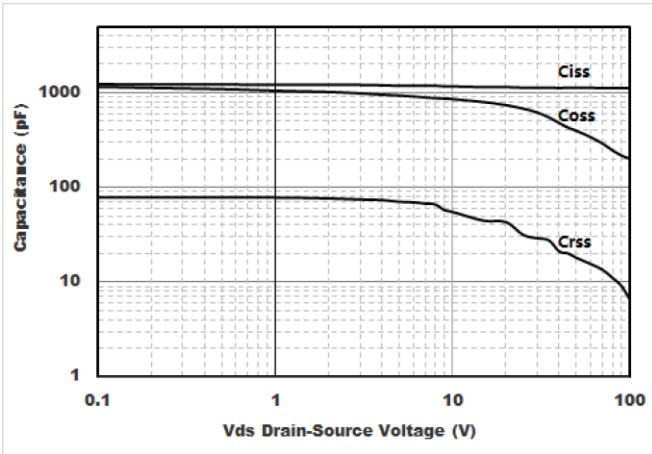


Figure3. Capacitance Characteristics

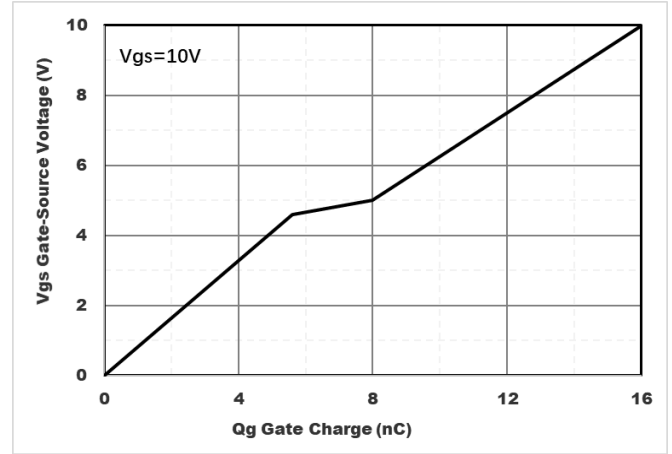


Figure4. Gate Charge

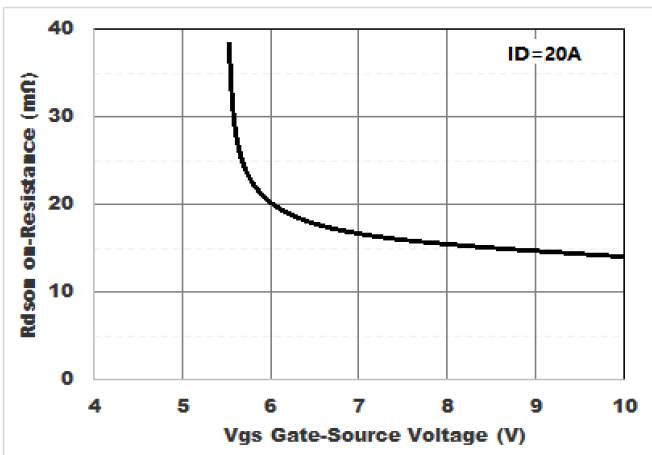


Figure5. On-Resistance vs. Drain Current and Gate Voltage

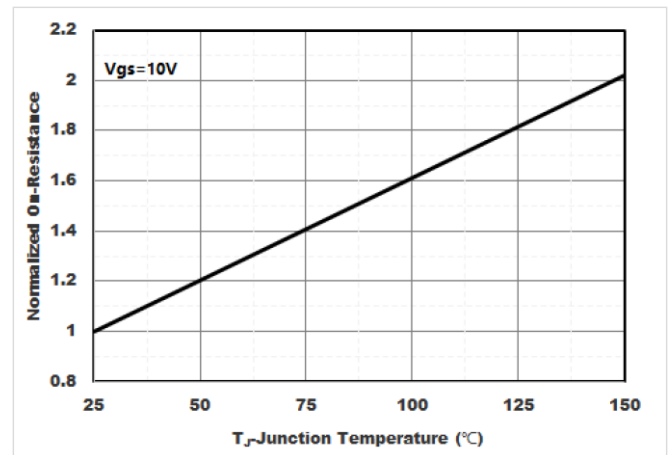


Figure6. Normalized On-Resistance



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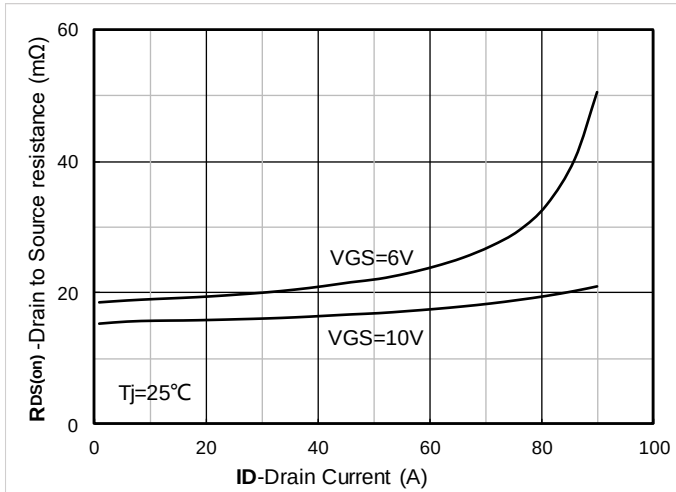


Figure 7. RDS(on) VS Drain Current

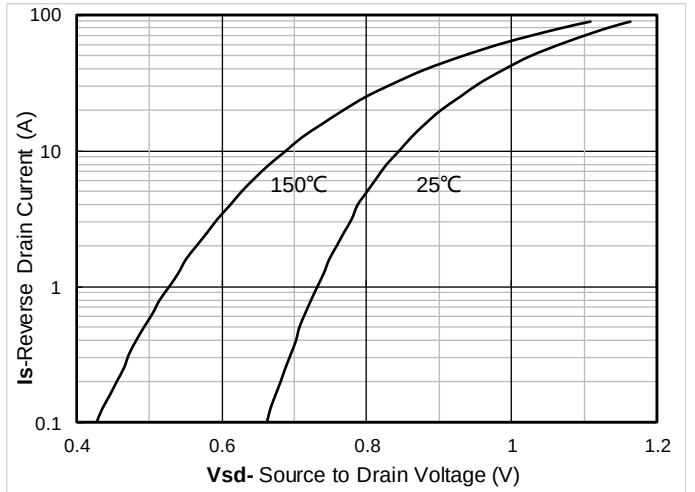


Figure 8. Forward characteristics of reverse diode

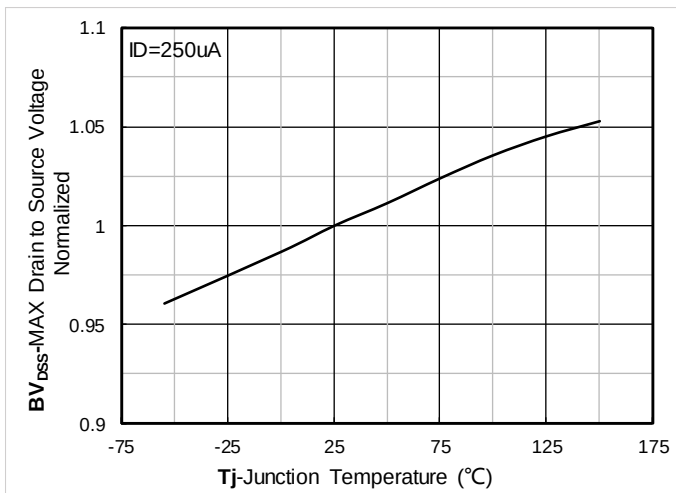


Figure 9. Normalized breakdown voltage

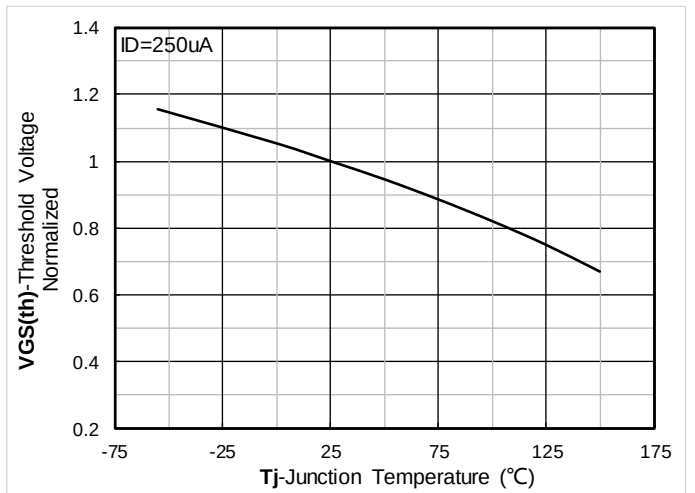


Figure 10. Normalized Threshold voltage

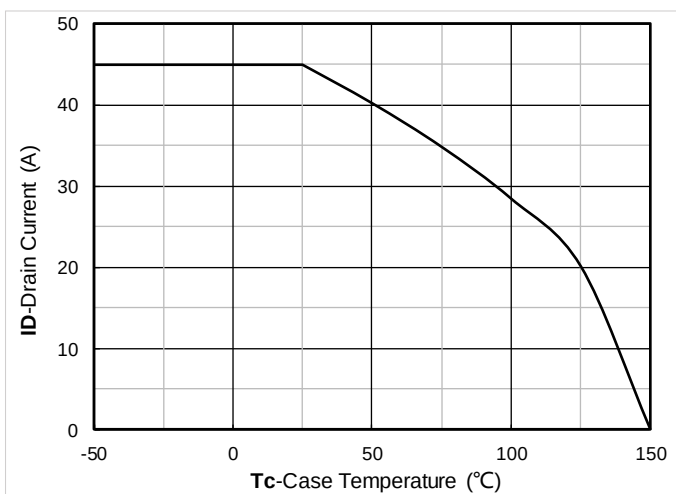


Figure 11. Current dissipation

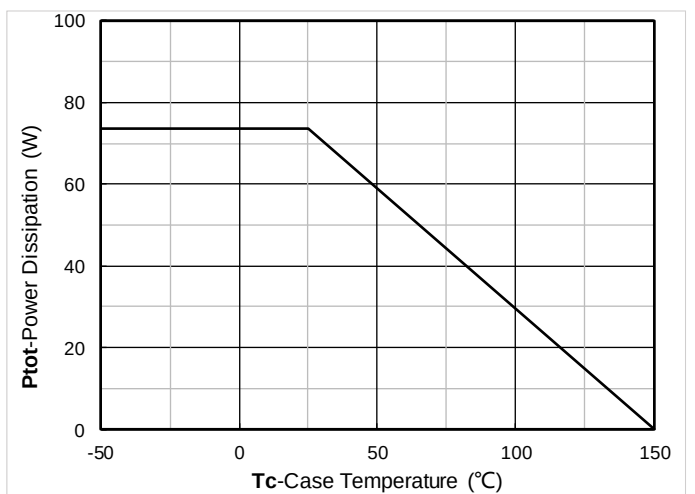


Figure 12. Power dissipation

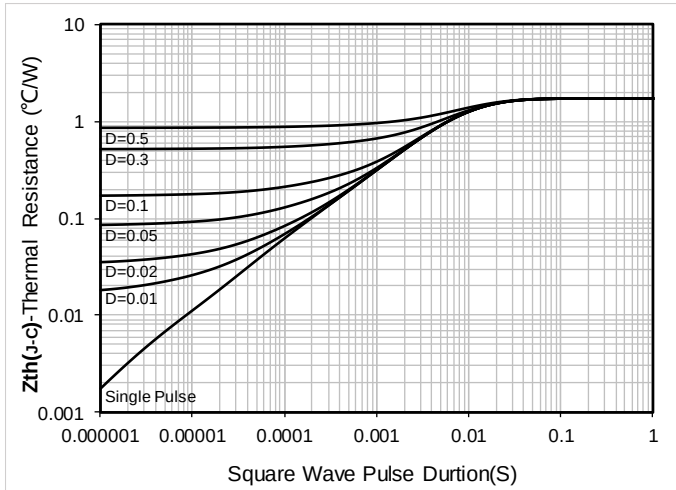


Figure 13. Maximum Transient Thermal Impedance

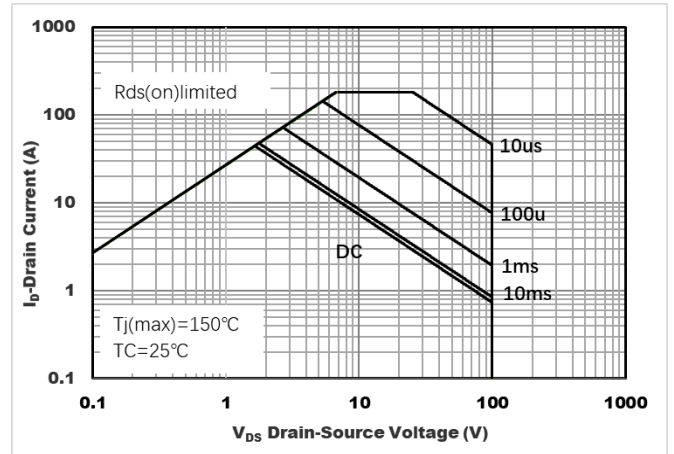
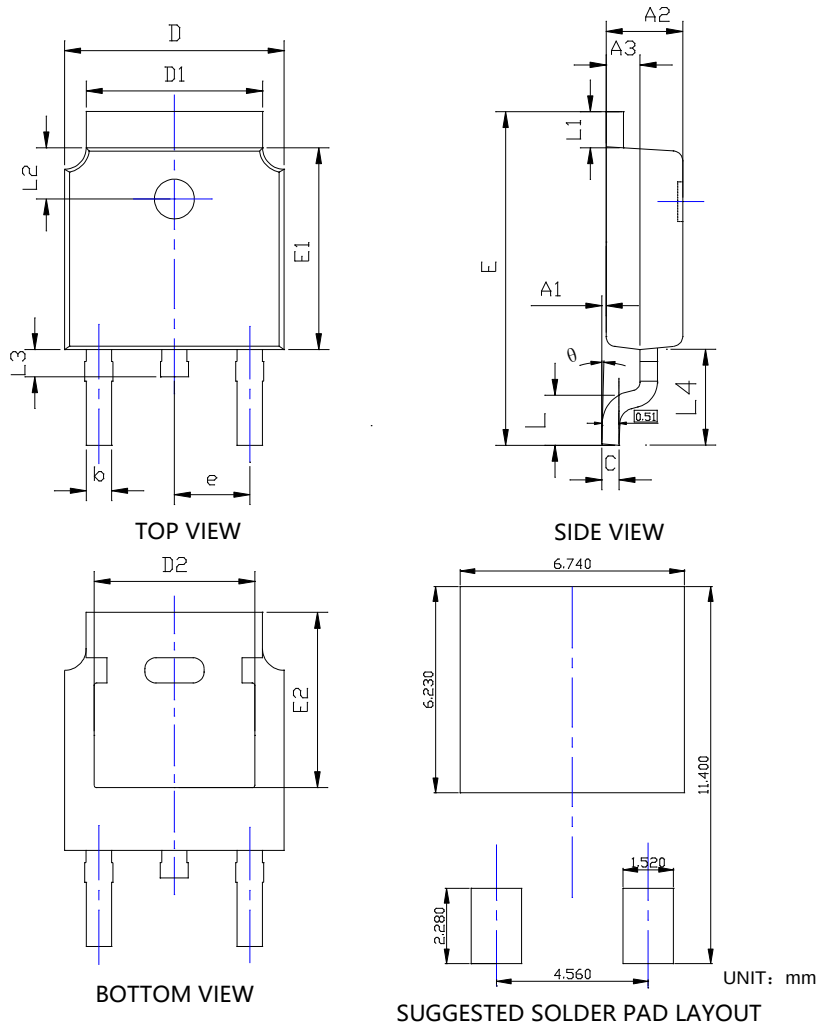


Figure 14. Safe Operation Area



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■ TO-252-B Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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