Series SDR

CR-P201P/CR-P203P

User Manual

Version Records:

Data	Version	Description
2023.05.25	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

Content

Part 1: Product Overview

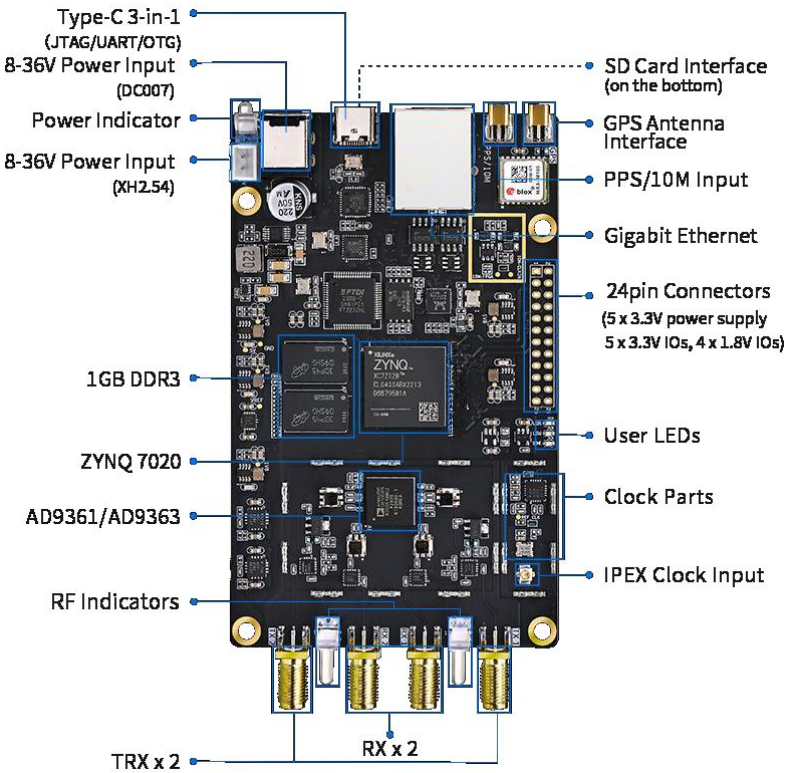
Part 1.1: Product Overview

This article introduces the CR-P201P/CR-P203P, these two hardware is fully compatible, direct software replacement can be used. The CR-P201P/CR-P203P used XILINX's XC7Z020-2CLG400I as the main controller, equipped with ADI's AD9361/AD9363 RF chip constitutes the main structure of the product. CR-P201P is ZYNQ7020 with AD9361, P203P is ZYNQ7020 with AD9363, the main difference between the two is that the bandwidth of the RF chip is different, users can choose the corresponding products according to the actual requirements.

The CR-P201P/CR-P203P integrated a variety of RF and other hardware interfaces, rich resources, easy to use, the following Product Function Block Diagram is an overview of the internal resource structure.

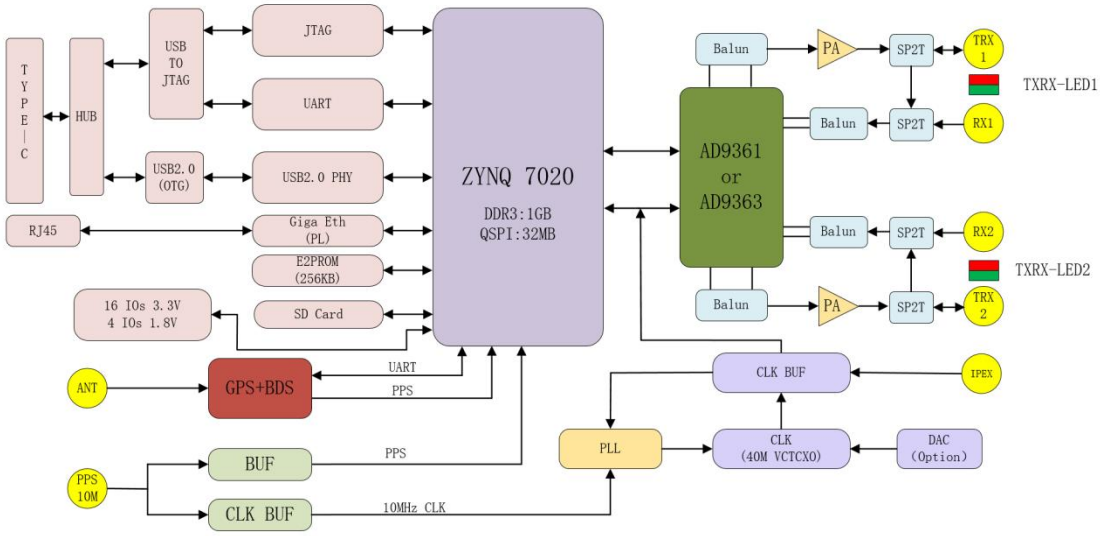
The PCBA Board Form Factors is 115mm * 70mm (4.53 inch * 2.76 inch), the thickness of PCB is 2.2mm, and the customized shell form factor is 125mm * 75mm (4.92 inch * 2.95 inch), the whole shell also plays a role in heat dissipation, to ensure the stable operation of the product.

The product is designed in accordance with industrial-grade standards, operating temperature -40℃-85 ℃, using a 0.1ppm high-precision clock, all interfaces are made of static electricity protection.



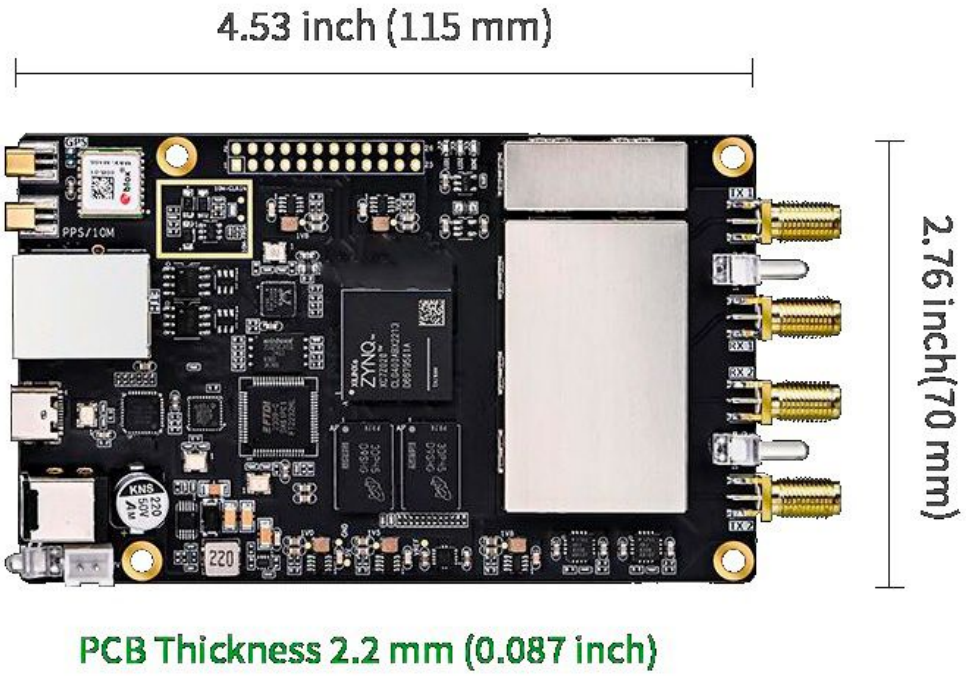
Part 1.2: Product Function Block Diagram

In this section, we will show the configuration details of the product in detail through the product block diagram and product specifications, as shown below.



Part 1.3: Form Factors

PCBA Board form factors is 115mm * 70mm (4.53 inch * 2.76 inch), and the customized shell form factor is 125mm * 75mm (4.92 inch * 2.95 inch).




4.92 inch (125 mm)
SDR
CR-P201P | CR-P203P
2.95 inch(75 mm)
TRX2
RX2
RX1
TRX1
0.91 inch
(23mm)

Part 2: Hardware Overview

Part 2.1: CR-P201P vs CR-P203P

The following table lists the parameter indicators of CR-P201P and CR-P203P. The difference between the two products is the selection of different RF chips, so the difference between CR-P201P and CR-P203P is the different frequency ranges of RF ports and different signal bandwidths. Users can compare the following table to choose the corresponding product.

PZSDR Main Parameters

SDR Module	CR-P201P	CR-P203P
RF Chip	**AD9361**	**AD9363**
Frequency range	70M-6Ghz	325M-3.8Ghz
Signal Bandwidths	200K-56Mhz	200K-20Mhz
Power Amplifier	2 Channel of TX	
FPGA Chip	XC7Z020-2CLG400I	
Processor Core	Dual Cortex-A9, 766Mhz	
Logic Cells	85K	
DDR3	1GB	
QSPI FLASH	256Mb	
E2PROM	256Kb	
RF Clock	40M VCTCXO(0.5PPM) / ipex Input/ External (Default is 40M VCTCXO)	
Gigabit Ethernet	1	
USB OTG	1	
UART	1	
JTAG	1	
SD Card Interface	1	
GPS	1	
PPS/ 10M Input	1	
Expansion Port IOs	16 x 3.3V IO, 4 x 1.8V IO	
Form Factors	Board: 4.53 inch x 2.76 inch x **0.09** inch	
Protection Class	Static Electricity Protection, Clock/RF are Shielded	
Power Supply	8-36V Ultra-wide Voltage Supply (Limit 50V)	
Working Tem.	-40°C~+85°C	

Part 2.2: About Power Supply

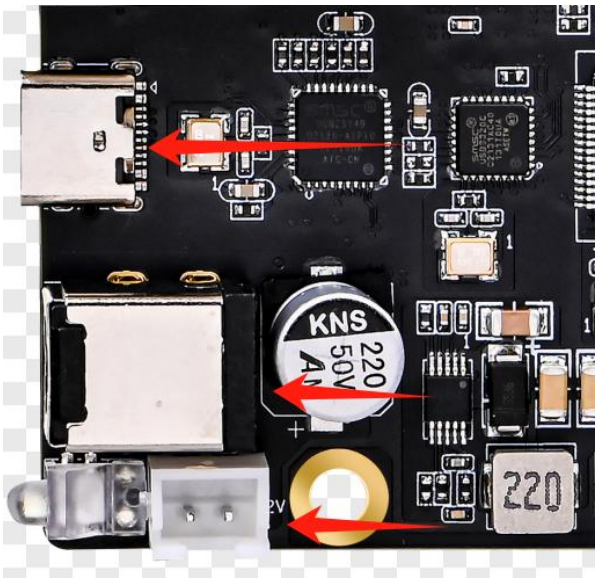
The product provides three kinds of power supply mode: XH2.54 interface, TypeC

interface, DC-007B interface, three kinds of power supply mode for customers to choose to use in different use mode.

XH2.54: If the product is integrated into the device, it can be powered through the XH2.54 interface, the power supply voltage range is 8-36V/1A.

TypeC: Here the TypeC interface provides multiple functions, both on the board power supply, directly connected to the computer USB interface, you can provide 5V power for the board. At the same time is also a communication interface, provides a JTAG, UART communication function, convenient for users to download and debug the board.

DC-007B and XH2.54 is connected, only one of the two can be connected. But with TypeC is to do the power compatible design, the two power supply can be connected at the same time, there is no conflict.



Part 2.3: System Clock

The CR-P201P/CR-P203P provides a 33.33Mhz clock input for the PS side, the input pin location is PS_CLK_500; provides a 40M clock for the PL side, the input pin location is IO_L11P_SRCC_35, pin number is J16.

Part 2.4: Global Reset

The CR-P201P/CR-P203P provides the nGST reset key near the board edge location for a system reset key, active low. This pin is connected to the PS_POR_500 on the PS side and the IO_12N_MRCC_34 (pin location U19) pin on the PL side, respectively.

Part 2.5: Boot Mode Selection

The P201P/P203P supports three boot modes, namely JTAG, QSPI Flash, and SD

card. Startup mode switching can provide the board side of the toggle switch to choose, when the switch toggle to the JTAG side, that is, JTAG startup mode, you can download the debugging single board through the JTAG interface; when the switch toggle to the side of the QSPI/SD, the startup mode switches to QSPI Flash and SD card mode, in this mode, we have done a special design, when not SD card, the default for QSPI In this mode, we have made a special design, when SD card is not connected, the default is QSPI Flash startup, when SD card is connected, the startup mode is automatically switched to SD mode.

Part 2.6: DDR3 Introduction

The PS side is equipped with two industrial-grade DDR3 chips, a single capacity of 512MB, two total capacity of 1GB, model MT41K256M16TW-107IT:P, DDR3L pin allocation can directly call the system allocation. You can also refer to the Demos provided by our company.

Part 2.7: QSPI FLASH Introduction

The CR-P201P/CR-P203P has a 32MB QSPI FLASH onboard, which can be used to store startup files and user files.

QSPI FLASH Pin	Pin Name	Pin Position
DATA0	MIO2	B8
DATA1	MIO3	D6
DATA2	MIO4	B7
DATA3	MIO5	A6
QSPI_CS	MIO1	A7
QSPI_CLK	MIO6	A5

Part 2.8: E2PROM Introduction

An E2PROM is reserved on the CR-P201P/CR-P203P with a capacity of 256Kb and the pin definitions are listed in the table below.

E2PROM PIN	PIN Name	PIN Position
I2C_SCL	MIO10	E9
I2C_SDA	MIO11	C6

Part 2.9: PL side Gigabit Ethernet

The Gigabit Ethernet chip is placed on the carrier board, and the Ethernet chip is

interconnected with the ZYNQ chip through the PL side, connecting the corresponding pins as shown in the following table Chip address PHY_AD[2:0]=010.

RMGII Signal	Pin Name	Pin Position
GPHY_GTX_CLK	IO_L3P_35	E17
GPHY_TXD0	IO_L3N_35	D18
GPHY_TXD1	IO_L4P_35	D19
GPHY_TXD2	IO_L4N_35	D20
GPHY_TXD3	IO_L5P_35	E18
GPHY_TX_EN	IO_L5N_35	E19
GPHY_RX_CLK	IO_L13P_MRCC_35	H16
GPHY_RXD0	IO_L6P_35	F16
GPHY_RXD1	IO_L6N_35	F17
GPHY_RXD2	IO_L7P_35	M19
GPHY_RXD3	IO_L7N_35	M20
GPHY_RX_DV	IO_L8P_35	M17
GPHY_MDC	IO_L2P_35	B19
GPHY_MDIO	IO_L2N_35	A20

Part 2.10: SD Card Slot Interface

The SD card holder is placed on the carrier board, which is connected to the BANK501 on the PS side of ZYNQ, because the level of BANK501 is 1.8V, but the data level of SD is 3.3V, We use the TXS02612RTWR for level shifting. The following is the pin assignment and schematic diagram of SD card interface, details refer to the schematic.

SD Card Slot Interface	Pin Name	Pin Position
SD_CLK	MIO40	D14
SD_CMD	MIO41	C17
SD_DATA0	MIO42	E12
SD_DATA1	MIO43	A9
SD_DATA2	MIO44	F13
SD_DATA3	MIO45	B15

Part 2.11: USB to JTAG and UART

The CR-P201P/CR-P203P is designed with a USB to JTAG/UART interface, the JTAG is connected to the JTAG interface of the host controller, and the UART is connected to the UART1 pin of the host controller. The following is the UART pin assignment, more detailed circuit can refer to the schematic.

UART	Pin Name	Pin Position
UART1_TX	MIO12	D9

UART1_RX	MIO13	E8

Part 2.12: USB 2.0

The USB2.0 chip is integrated on the CR-P201P/CR-P203P. The following table lists the correspondence between the USB PHY and the main chip. For detailed information, please refer to the schematic.

USB2.0 Signal	Pin Name	Pin Position
USBPHY_DATA0	MIO32	A14
USBPHY_DATA1	MIO33	D15
USBPHY_DATA2	MIO34	A12
USBPHY_DATA3	MIO35	F12
USBPHY_DATA4	MIO28	C16
USBPHY_DATA5	MIO37	A10
USBPHY_DATA6	MIO38	E13
USBPHY_DATA7	MIO39	C18
USBPHY_STP	MIO30	C15
USBPHY_NXT	MIO31	E16
USBPHY_DIR	MIO29	C13
USBPHY_CLKOUT	MIO36	A11
USB_nRSET	MIO48	B12

Part 2.13: AD9361 Introduction

The RF part of the product uses ADI's AD9361, and in this subsection will introduce in details, from the RF link, data channel, and clock part.

Part 2.13.1: RF Front-end Circuits

The RF front-end circuit involves three parts: balun, amplifier, and RF switch. The bandwidth of the balun is 10M-6Ghz, which covers the communication bandwidth of the AD9361.

The bandwidth of the amplifier is 50M-6Ghz, which also covers the communication bandwidth of AD9361, but the gain flatness of the amplifier in the whole communication bandwidth is slightly different. The following table can see the amplifier's indicators for each frequency point in detail.

FREQ	Gain	Isolation	Input Return Loss	Output Return Loss	Stability		IP-3 Output	1dB Comp. Output	Noise Figure
(MHz)	(dB)	(dB)	(dB)	(dB)	K	Measure	(dBm)	(dBm)	(dB)
50.00	17.73	23.19	14.21	18.51	1.14	0.76	31.53	17.82	2.10
80.00	17.14	22.43	16.76	18.87	1.14	0.73	32.21	17.91	1.97
100.00	16.93	22.26	18.14	19.00	1.15	0.72	32.46	17.83	2.00
200.00	16.55	22.00	21.40	19.27	1.18	0.72	32.09	17.88	1.96
400.00	16.32	21.92	22.06	19.17	1.19	0.72	32.80	17.69	2.18
500.00	16.22	21.95	21.60	19.08	1.20	0.73	32.65	17.75	2.22
600.00	16.12	21.91	20.87	18.92	1.21	0.73	32.75	17.73	2.18
800.00	15.90	21.94	19.22	18.59	1.23	0.75	32.97	17.68	2.22
1000.00	15.63	21.95	17.75	18.27	1.24	0.77	32.35	17.74	2.14
1200.00	15.34	21.94	16.45	17.96	1.26	0.79	33.10	17.70	2.27
1400.00	15.03	21.96	15.29	17.73	1.29	0.81	33.34	17.71	2.28
1500.00	14.88	21.96	14.70	17.47	1.29	0.82	32.76	17.78	2.31
1600.00	14.70	21.96	14.37	17.59	1.31	0.83	33.06	17.69	2.35
1800.00	14.38	21.98	13.49	17.43	1.33	0.85	33.66	17.56	2.36
2000.00	14.04	21.97	12.88	17.64	1.36	0.87	33.23	17.81	2.39
2200.00	13.72	21.93	12.29	17.75	1.38	0.89	33.13	17.99	2.45
2400.00	13.42	21.90	11.83	17.77	1.40	0.91	33.38	17.82	2.44
2500.00	13.27	21.94	11.64	17.87	1.41	0.92	33.32	17.96	2.50
2600.00	13.13	21.94	11.46	17.91	1.43	0.93	33.58	17.80	2.61
2800.00	12.85	21.83	11.14	17.97	1.44	0.95	33.46	17.78	2.65
3000.00	12.57	21.81	10.87	17.73	1.46	0.96	33.43	17.84	2.57
3200.00	12.35	21.77	10.64	17.84	1.47	0.97	32.91	17.81	2.70
3400.00	12.09	21.84	10.61	18.20	1.52	0.98	33.34	17.88	2.73
3500.00	12.00	21.75	10.43	17.93	1.51	0.98	33.57	17.63	2.89
3600.00	11.89	21.62	10.24	17.62	1.50	0.99	33.63	17.80	2.78
3800.00	11.68	21.57	10.12	17.40	1.52	0.99	33.53	17.82	2.91
4000.00	11.51	21.44	9.87	17.10	1.51	1.00	33.78	17.77	3.01
4200.00	11.36	21.39	9.75	16.86	1.52	1.00	33.67	17.67	2.96
4400.00	11.24	21.35	9.57	16.39	1.51	1.01	33.48	17.50	3.04
4500.00	11.08	21.33	9.53	16.36	1.54	1.01	33.53	17.62	3.12
4600.00	11.06	21.42	9.49	16.15	1.55	1.01	33.33	17.68	3.19
4800.00	10.90	21.23	9.20	15.40	1.52	1.02	33.45	17.59	3.25
5000.00	10.75	21.21	9.09	15.04	1.53	1.02	33.46	17.18	3.27
5200.00	10.64	21.03	8.71	14.21	1.49	1.02	33.61	17.24	3.34
5400.00	10.55	20.98	8.50	13.69	1.48	1.02	33.92	16.79	3.45
5500.00	10.50	20.92	8.35	13.36	1.47	1.02	33.27	17.75	3.44
5600.00	10.67	21.34	8.50	13.68	1.51	1.03	33.63	17.27	3.51
5700.00	10.57	21.11	8.18	13.01	1.46	1.03	33.71	17.19	3.51
5800.00	10.48	20.92	7.96	12.52	1.43	1.03	33.58	17.27	3.59
5900.00	10.40	20.86	7.76	12.12	1.41	1.03	33.69	17.15	3.70
6000.00	10.37	20.82	7.64	12.03	1.40	1.03	34.30	16.80	3.72
6500.00	10.12	20.52	6.68	10.59	1.30	1.04	33.96	16.82	4.00
7000.00	9.73	20.58	5.74	9.16	1.23	1.05	33.55	16.34	4.12
7500.00	8.78	20.45	5.07	7.72	1.19	1.04	32.63	15.47	4.72
8000.00	7.49	21.63	4.30	6.09	1.27	1.01	30.33	15.48	5.32

The RF switch adopts SPDT one-in-two-out, with a bandwidth of 9K-8G, and the RF switch has an internal integrated electrostatic protection circuit, which effectively protects the RF port. The switching logic of the corresponding RF switch can be referred to the following table, for the TX/RX switching of AD9361, you can refer to the schematic for the actual connection relationship to correspond to the adjustment.

LS	CTRL	RFC-RFC1	RFC-RFC1
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

In addition, for the RF front-end we have involved 4-way LED indication, port setting 1 corresponds to LED on and port setting 0 corresponds to LED off. The following table lists the LED pin correspondences.

LED	Pin Name	Pin Position
LED_RF_TX1	IO_21P_35	N15
LED_RF_RX1	IO_21N_35	N16
LED_RF_TX2	IO_22P_35	L14
LED_RF_RX2	IO_22N_35	L15

Part 2.13.2: AD9361 Control and Data Ports

The AD9361 digital port is divided into data port and control port, the data port can be defined as LVCMOS, can also be defined as LVDS, LVCMOS communication rate is not high, so the project provided by Puzhi, default LVDS interface to define the data port, the following table lists the pin correspondence, you can also refer to the schematic.

AD9361 Interface	Pin Name	Pin Position
AD9631_TX_P0	IO_8P_34	W14
AD9631_TX_N0	IO_8N_34	Y14
AD9631_TX_P1	IO_5P_34	T14
AD9631_TX_N1	IO_5N_34	T15
AD9631_TX_P2	IO_4P_34	V12
AD9631_TX_N2	IO_4N_34	W13
AD9631_TX_P3	IO_10P_34	V15
AD9631_TX_N3	IO_10N_34	W15
AD9631_TX_P4	IO_6P_34	P14
AD9631_TX_N4	IO_6N_34	R14
AD9631_TX_P5	IO_9P_34	T16
AD9631_TX_N5	IO_9N_34	U17
AD9631_TX_FRAME_P	IO_7P_34	Y16
AD9631_TX_FRAME_N	IO_7N_34	Y17
AD9631_FB_CLK_P	IO_11P_SRCC_34	U14
AD9631_FB_CLK_N	IO_11N_SRCC_34	U15
AD9631_RX_P0	IO_21P_34	V17
AD9631_RX_N0	IO_21N_34	V18
AD9631_RX_P1	IO_17P_34	Y18
AD9631_RX_N1	IO_17N_34	Y19

AD9631_RX_P2	IO_16P_34	V20
AD9631_RX_N2	IO_16N_34	W20
AD9631_RX_P3	IO_18P_34	V16
AD9631_RX_N3	IO_18N_34	W16
AD9631_RX_P4	IO_15P_34	T20
AD9631_RX_N4	IO_15N_34	U20
AD9631_RX_P5	IO_20P_34	T17
AD9631_RX_N5	IO_20N_34	R18
AD9631_RX_FRAME_P	IO_19P_34	R16
AD9631_RX_FRAME_N	IO_19N_34	R17
AD9631_DATA_CLK_P	IO_13P_MRCC_34	N18
AD9631_DATA_CLK_N	IO_13N_MRCC_34	P19
AD9631_CLK_OUT	IO_14P_SRCC_34	N20
AD9631_SPI_CLK	IO_1P_34	T11
AD9631_SPI_nCS	IO_1N_34	T10
AD9631_SPI_DI	IO_2P_34	T12
AD9631_SPI_DO	IO_2N_34	U12
AD9631_nRST	IO_22N_34	W19
AD9631_ENABLE	IO_23P_34	N17
AD9631_EN_AGC	IO_23N_34	P18
AD9631_SYNC_IN	IO_24P_34	P15
AD9631_TXNRX	IO_24N_34	P16
AD9631_CTRL_OUT0	IO_14P_SRCC_13	Y9
AD9631_CTRL_OUT1	IO_16P_13	W10
AD9631_CTRL_OUT2	IO_14N_SRCC_13	Y8
AD9631_CTRL_OUT3	IO_15P_13	V8
AD9631_CTRL_OUT4	IO_15N_13	W8
AD9631_CTRL_OUT5	IO_16N_13	W9
AD9631_CTRL_OUT6	IO_12N_MRCC_13	U10
AD9631_CTRL_OUT7	IO_12P_MRCC_13	T9
AD9631_CTRL_IN0	IO_11P_SRCC_13	U7
AD9631_CTRL_IN1	IO_13N_MRCC_13	Y6
AD9631_CTRL_IN2	IO_13P_MRCC_13	Y7
AD9631_CTRL_IN3	IO_11N_SRCC_13	V7

Part 2.13.3: AD9361 Clock Circuit

The input clock of AD9361 adopts 40M VCTCXO with an accuracy of up to 0.5ppm. In addition, the board has reserved ADF4002BRUZ chip, so if there is a higher requirement for the clock accuracy, it can be adjusted by inputting it to ADF4002BRUZ through RF header. For detailed use of the clock you can refer to the schematic.

Part 2.14: PPS and Clock Inputs

The CR-P201P/CR-P203P designed a PPS input and 10M clock input circuit, this circuit from the same mmcx interface input, RC circuit with the FPGA's IO control to select the PPS and the clock circuit on and off, in addition to the 10M clock signal is also connected to the ADF4002, to do the clock correction.PPS and the clock were connected to the FPGA's:

Signal Name	Pin Name	Pin Position
PPS-IN	IO_14P_SRCC_35	J18
10M_FPGA	IO_12P_MRCC_34	U18
EN_10M_FPGA	IO_25_34	T19
EN_10M_CLKIN	IO_22P_34	W18

Part 2.15: GPS Module

The GPS module is integrated on the board, which can implement GPS and BeiDou positioning function. We can provide UART to configure and read the GPS module data, in addition the module provides PPS signal. The following table lists the pin correspondences of the GPS module, details refer to the schematic.

GPS Modue	Pin Name	Pin Position
GPS_UART_TXD	IO_16N_35	G18
GPS_UART_RXD	IO_17P_35	J20
GPS_nRESET	IO_16P_35	G17
GPS_PPS	IO_14N_35	H18

Part 2.16: IO Expansion Ports

The 40P 2.54mm pitch row of pins is designed on the board for the connection of the expansion signals, the following table marks the location of the chip where the signals are located, refer to the schematic section for detailed connections.

IO Interface	Pin Name	Pin Position	Level Standards	IO Interface	Pin Name	Pin Position	Level Standards
5	IO_1P_35	C20	3.3V	6	IO_15P_35	F19	3.3V
7	IO_1N_35	B20		8	IO_15N_35	F20	
9	IO_19P_35	H15		10	IO_20P_35	K14	
11	IO_19N_35	G15		12	IO_20N_35	J14	
13	IO_23P_35	M14		14	IO_9P_35	L19	
15	IO_23N_35	M15		16	IO_9N_35	L20	
17	IO_12N_35	K18		18	IO_18N_35	G20	

19	IO_13N_35	H17		20	IO_25_35	J15	
21	IO_20P_13	Y12	1.8V	22	IO_21P_13	V11	1.8V
23	IO_20N_13	Y13		24	IO_21N_13	V10	

Part 2.17: User LED

The CR-P201P/CR-P203P has two LEDs reserved for user-defined use, LED high level on,LED low level off. The following table lists the pin correspondences of the LEDs, for a more detailed description you can refer to the schematic.

LED Pin	Pin Name	Pin Position
LED1	IO_0_35	G14
LED2	IO_8N_35	M18