Shenzhen Leadtek Electronics Co.,Ltd

PRODUCT SPECIFICATION

TFT-LCD   MODULE

Module No：LTK080WXBLM15-V0

☑ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
jona	*Jerry*	*lan*

Final Approval by Customer

Approved by	Comment

※The specification of "TBD" should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

1.Document Revision History

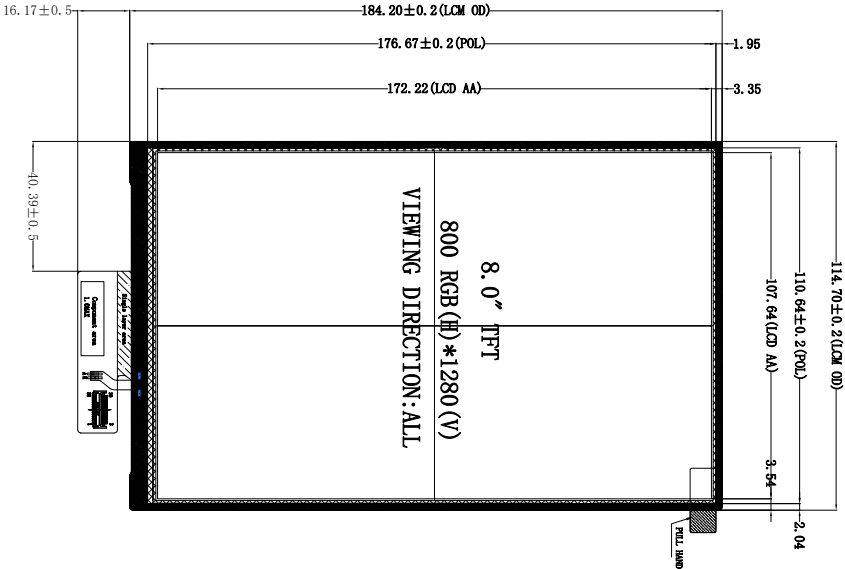| Version	Contents	Date	Note
V0	Initial version	2024.04 20	

2.General Specifications

N0	Item	Specification	Unit	Remark
1	LCD Size	TFT"8.0	inch	-
2	Panel Type	IPS	-	-
3	Display Resolution	800 x RGB x 1280	pixel	-
4	Display mode	Normally Black	-	-
5	Display colors	16.7M	-	-
6	Viewing Direction	ALL	-	-
7	LCM Module size	114.70(H)x184.20（V)x2.51(T)	mm	Note
8	Active Area	107.64(H)x172.22(V)	mm	Note
9	Pixel Pitch	0.1345(W)×0.1345(H)	mm	-
10	Weight	TBD	g	-
11	Driver IC	ILI9881C	bit	-
12	Light Source	White LED	-	-
13	Interface	MIPI 4 lane	-	-

3.EXTERNAL DIMENSIONS

Front View

8.0" TFT
800 RGB(H)*1280(V)
VIEWING DIRECTION:ALL

184.20±0.2(LCM OD)
176.67±0.2(POL)
172.22(LCD AA)
16.17±0.5
1.95
3.35
114.70±0.2(LCM OD)
110.64±0.2(POL)
107.64(LCD AA)
40.39±0.5
3.54
2.04
PULL HAND

Side View

2.51±0.2(LCM OD)

Back View

Connector:
FH26-31S-0.3SHW(10)

Iron frame hole digging

82.00
1.00MAX
23.65
61.04
16.34

Model label
LTK080WXBLM15-V0
YYYY-MM-DD

21 CHIP WHITE LEDs
VF=9.6V(TYP),IF=140mA

A
K
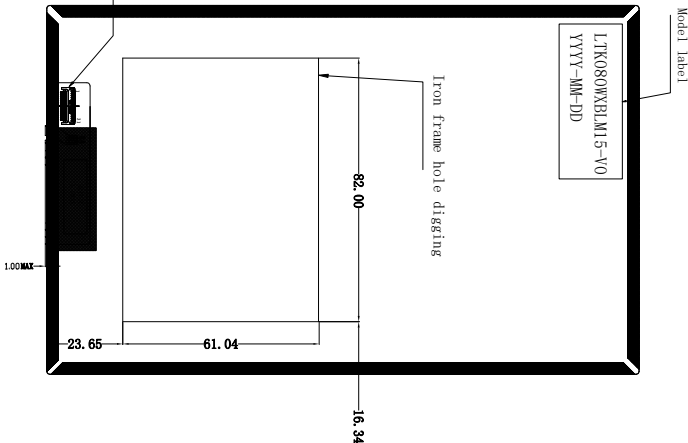
PIN	SYMBOL
1	LEDA
2	LEDA
3	LEDA
4	NC
5	LEDK
6	LEDK
7	LEDK
8	LEDK
9	GND
10	GND
11	MIPI_D2+
12	MIPI_D2-
13	GND
14	MIPI_D1+
15	MIPI_D1-
16	GND
17	MIPI_CLK+
18	MIPI_CLK-
19	GND
20	MIPI_D0+
21	MIPI_D0-
22	GND
23	MIPI_D3+
24	MIPI_D3-
25	GND
26	TE
27	RESET
28	NC
29	VDDIO/1.8V
30	VDD/3.3V
31	VDD/3.3V

Notes:

1. Display: 8.0", TFT
2. Resolution: 800*RGB*1280
3. LCD Viewing Direction: ALL
4. LCD Driver:ILI9881C
5. LCM Brightness:420 cd/m² (TYP) ,Uniformity≥80%
6. *:Critical dimension:( )Reference dimension
7. Operating Temperature:-20℃~+60℃
8. Storage Temperature:-30℃~+70℃
9. Requirements on Environmental Protection: ROHS
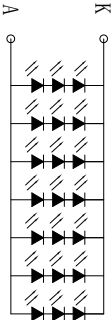
REV		DESCRIPTION	DATE	NAME
3				
2				
1				
0		NEW	2024.04.19	IAN

Shenzhen Leadtek Electronics Co.,Ltd

LEADTEK DISPLAY

SCALE:1/1	UNIT:mm	PAGE:1/1	VER:V0	Approve	Check	Drawn
Part No:	LTK080WXBLM15			Kevin	JONA	IAN
Customer No:						

4.0 Interface Pin Connection

4.1 TFT LCD Module

PIN NO	SYMBOL	DESCRIPTION
1	LEDA	Power for LED backlight (Anode)
2	LEDA	Power for LED backlight (Anode)
3	LEDA	Power for LED backlight (Anode)
4	NC	No connect.
5	LEDK	Power for LED backlight (Cathode)
6	LEDK	Power for LED backlight (Cathode)
7	LEDK	Power for LED backlight (Cathode)
8	LEDK	Power for LED backlight (Cathode)
9	GND	Ground
10	GND	Ground
11	MIPI_D2+	HSSI_D2_Pare differential small amplitude signals.
12	MIPI_D2-	HSSI_D2_Nare differential small amplitude signals.
13	GND	Ground
14	MIPI_D1+	HSSI_D1_Pare differential small amplitude signals.
15	MIPI_D1-	HSSI_D1_Nare differential small amplitude signals.
16	GND	Ground.
17	MIPI_CLK+	HSSI_CLK_P are differential small amplitude signals
18	MIPI_CLK-	HSSI_CLK_N are differential small amplitude signals
19	GND	Ground.
20	MIPI_D0+	HSSI_D0_P are differential small amplitude signals.
21	MIPI_D0-	HSSI_D0_N are differential small amplitude signals.
22	GND	Ground.
23	MIPI_D3+	HSSI_D3_P are differential small amplitude signals.
24	MIPI_D3-	HSSI_D3_N are differential small amplitude signals.
25	GND	Ground.
26	NC	No connect.
27	RESET	Global reset pin.1.8V
28	NC	No connect.
29	IOVCC	Power supper 1.8V
30	VCI	Power supper 3.3 V
31	VCI	Power supper 3.3 V

5.0 Absolute Maximum Ratings

5.1 Electrical Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VCI	-0.3	3.6	V	GND=0
	IOVCC	-0.3	3.6	V	GND=0

Note (1) Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at indicated in the operational sections(6.1) of this specification.

5.2 Back-light Unit:

PARAMETER	Sympol	Min.	Typ.	Max.	Unit	Test Condition	Note
LED Current	IF	–	140	–	mA	–	–
LED Voltage	VF	8.4	9.6	9.9	V	IF=140mA	–
LCM Luminance (on the modulesurface ,BM-7)	LV	–	420	–	cd/m2	IF=140mA	–
Color temperature（@CA210）		8000	9000	10000	K	IF=140mA	–
Life Time		–	30000	–	Hr.	IF=140mA	–
Color	White						

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2)Ta=25±2℃

(3)Test condition: LED Current 140mA
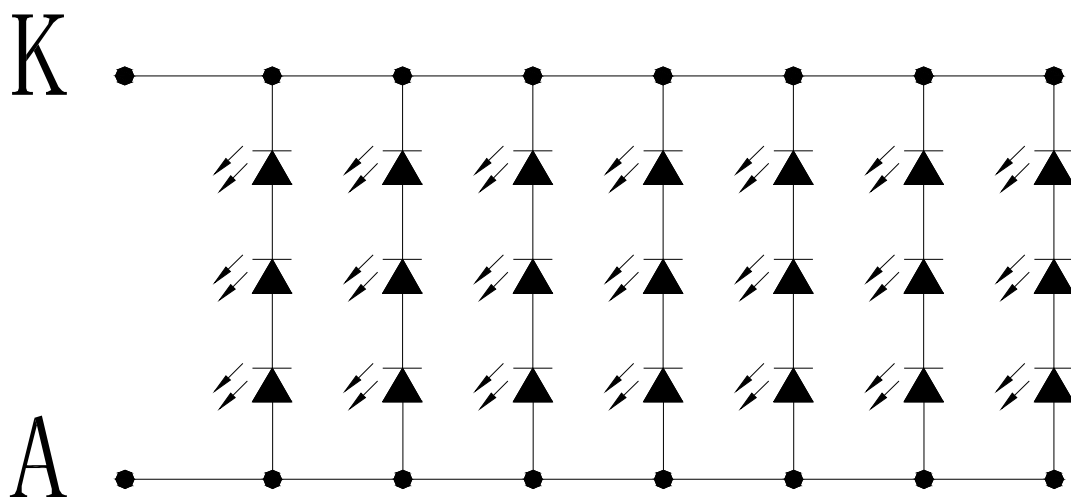
CURRENT IF=140mA

3C*7B=21LED

5.3 Electrical Specifications(Typical Operation Conditions, At Ta = 25 °C)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Power Supply Voltage	VCI	2.8	3.3	3.3	V	-
	IOVCC	1.75	1.8	3.3	V	-

5.4 Power On/Off Sequence.

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWON	0	-	-	ms	
tON1	0	-	-	ms	
tMIPI-ON	0	-	tRPWIRES	ms	
tRPWIRES	5	-	-	ms	
tRESETL	10	-	-	us	
tRESETH	5	-	-	ms	
tSLPOUT	120	-	-	ms	
tBLON	0	-	-	ms	

BOOSTM[1:0]=01/11 (External AVDD/AVEE Power)
VCCD=IOVCC=VCCH=1.65V ~ 3.6V, AVDD=VCI=VCIP=4.5V ~ 6.0V, AVEE=-4.5V ~ -6.0V
Power on:

	Min	Typ	Max
Power up tRamp for AVDD/AVEE/IOVCC	-	no limit	-
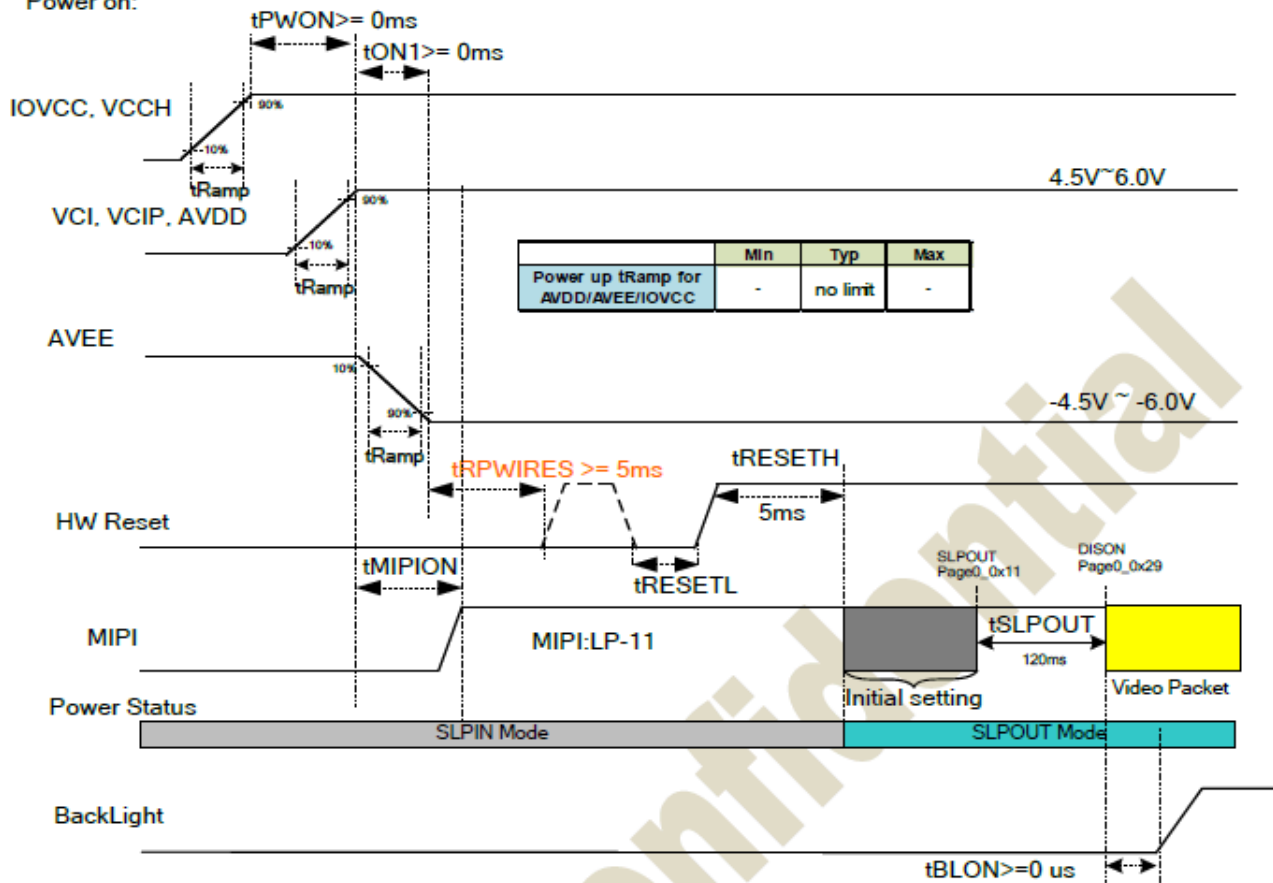
For the power off case2, DISOFF command and tDISOFF are optional. That means t_{CMD_OFF} could be followed by the SLPIN command and tSLPIN , without DISOFF command and tDISOFF.

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWOFF	0	-	-	ms	
tPWOFF1	0	-	-	ms	
tPWOFF2	0	-	-	ms	
tMIPIOFF1	0	-	-	ms	power off case 1
tRSTOFF1	120	-	-	ms	power off case 1
tMIPIOFF2	0	-	-	ms	power off case 2
tRSTOFF2	0	-	-	ms	power off case 2
tCMD_OFF	1	-	-	ms	power off case 2
tDISOFF	50	-	-	ms	power off case 2
tSLPIN	100	-	-	ms	power off case 2
tBLOFF	0	-	-	ms	

BOOSTM[1:0]=01/11 (External AVDD/AVEE Power)
VCCD=IOVCC=VCCH=1.65V ~ 3.6V, AVDD=VCI=VCIP=4.5V ~ 6.0V, AVEE=-4.5V ~ -6.0V

Power off: Case 1
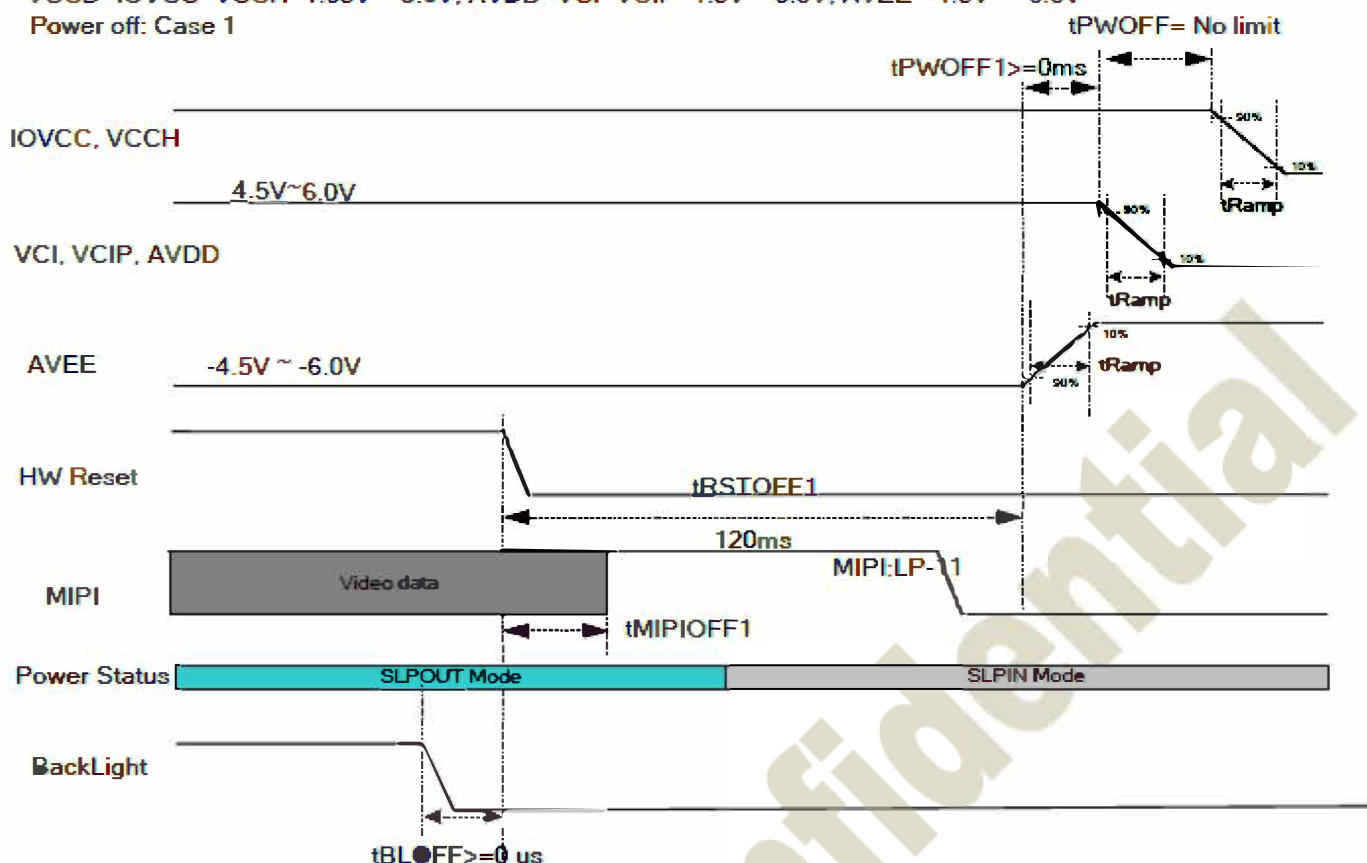
6.0 Optical Characteristics

6.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	Θ=0	900	1200	—		(1)(2)(4)
Response time		Tr+ Tf	Normal viewing angle	—		35	msec	(1)(3)
Color chromaticity (CIE1931)	White	W_x		-0.040	0.300	+0.040		(1)(4) CF Glass C light
		W_y			0.310			
	Red	Rx			-			
		Ry			-			
	Green	Gx			-			
		Gy			-			
	Blue	Bx			-			
		By			-			
Viewing angle	Hor.	Θ_L	CR>10	-	**80**	—		
		Θ_R		-	**80**	—		
	Ver.	Θ_U		-	**80**	—		
		Θ_D		-	**80**	—		
NTSC					60%	—	%	
Luminance Uniformity		YU		70	—		%	

6.2 Measuring Condition

■ Measuring surrounding : dark room

■ Ambient temperature : 25±2℃

■ 30min. warm-up time.

6.3 Measuring Equipment

■ TOPCON BM-7

■ Measuring spot size : field 2°

Note (1) Definition of Vsat and Vth (at 20℃)
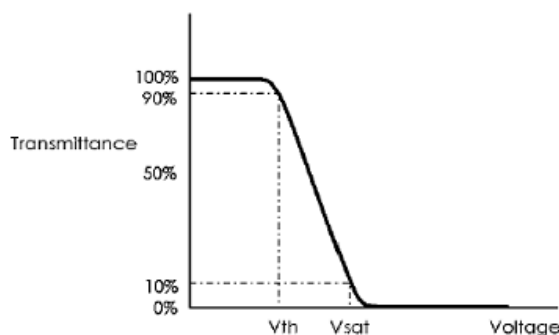
Note (2) Definition of Viewing Angle :
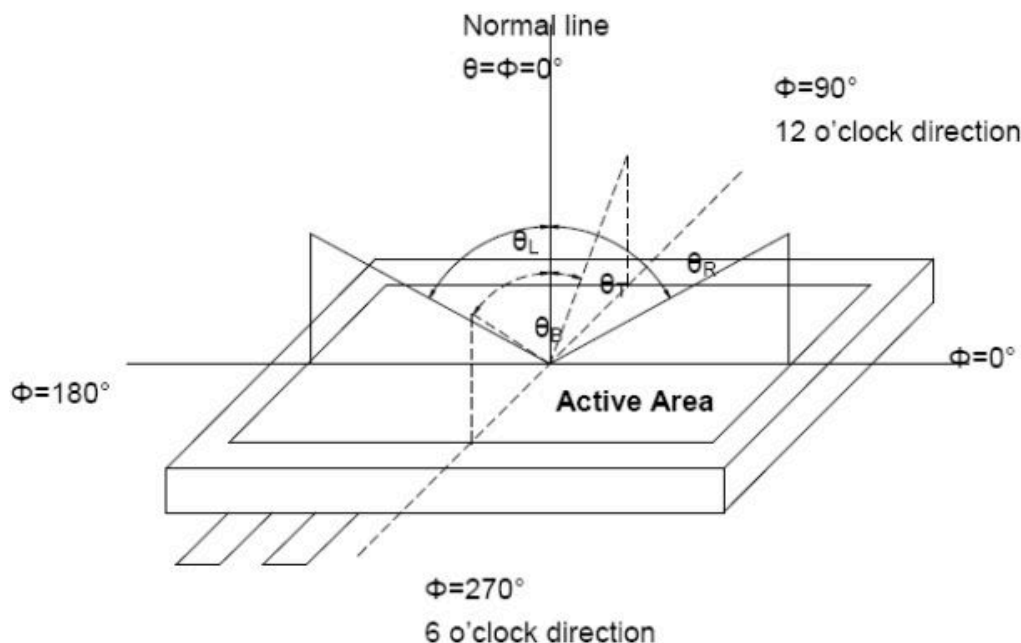
Note 3: Definition of response time:
The response time is defined as the LCD optical switching time interval between
"White" state and "Black" state. Rise time (TON) is the time between photo detector
output intensity changed from 90% to 10%. And fall time (TOFF) is the time
between photo detector output intensity changed from 10% to 90%.
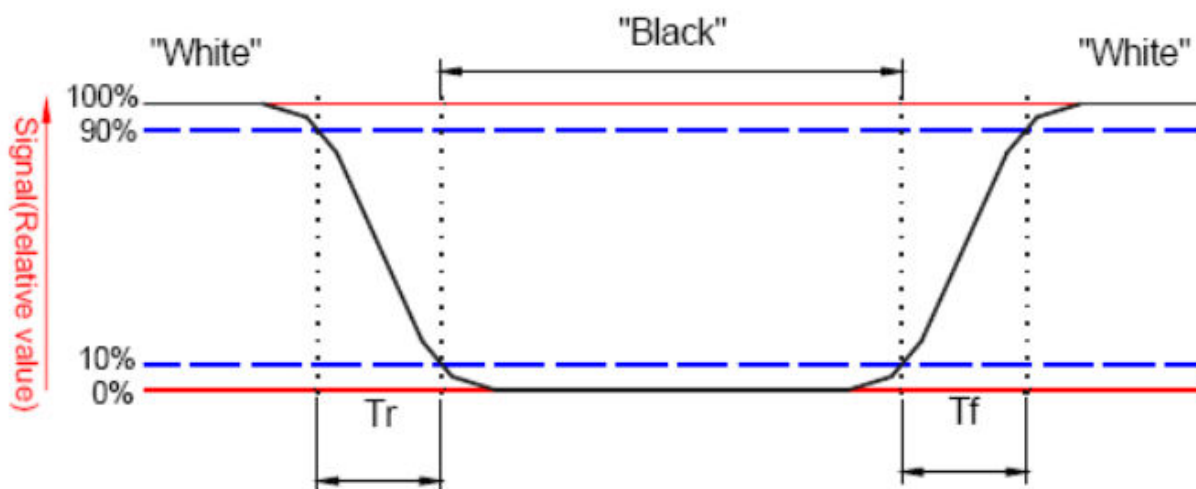
Note 4: Definition of contrast ratio:

Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

Note 5: Definition of color chromaticity (CIE 1931)

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel

7.0 Block Diagram

7.1 TFT-LCD Module
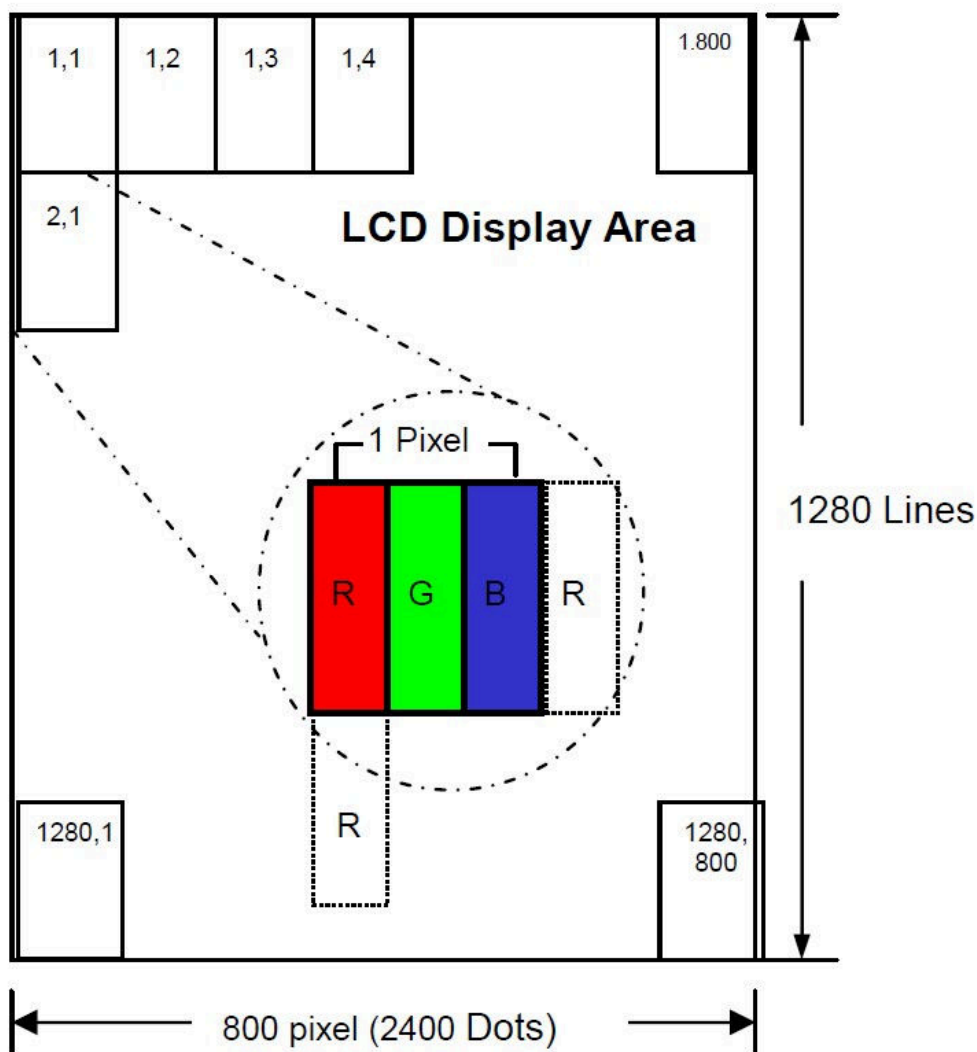
8.0 MIPI Interface(Mobile Industry Processing Interface)

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure 7.1 shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.
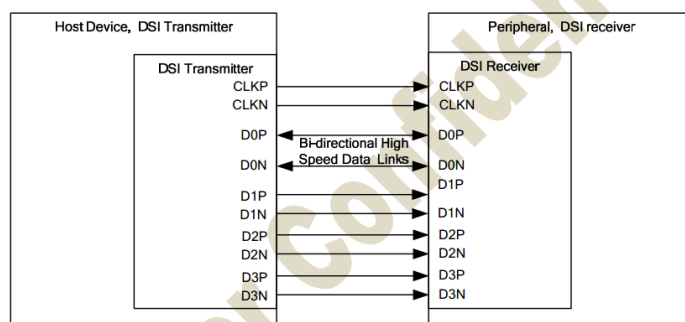
8.1 MIPI Signal Timing Characteristics

8.1.1 AC Electrical Characteristics

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the

differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times.
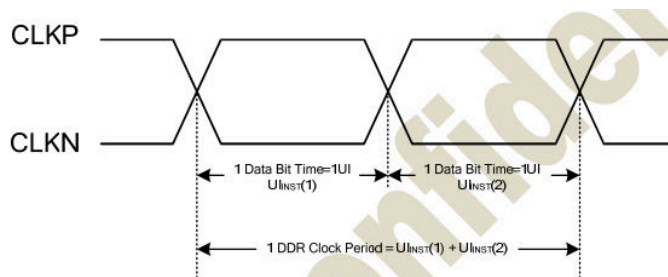
Figure 11.5: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI. The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5), (6)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 850bps of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.
(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(6) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data. The transmitter shall ensure that a rising edge of the DDR

clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.
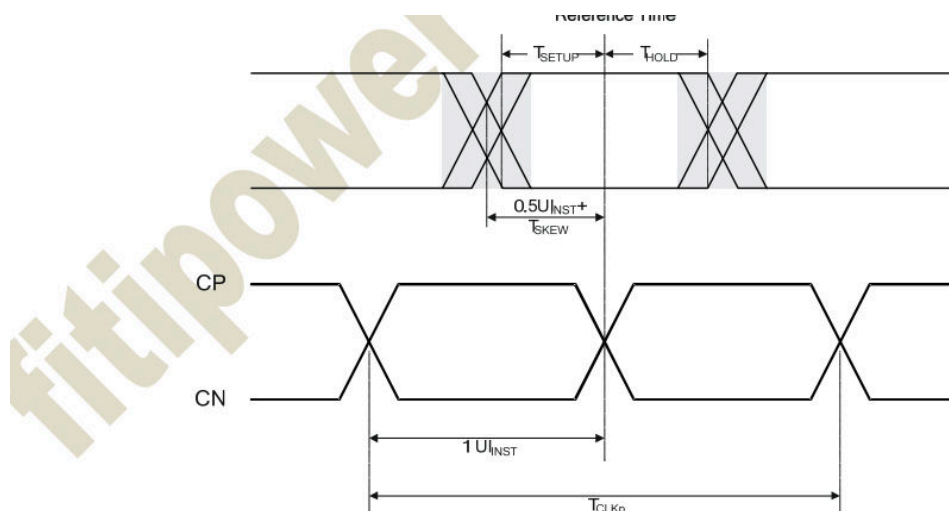

Figure 11.6: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

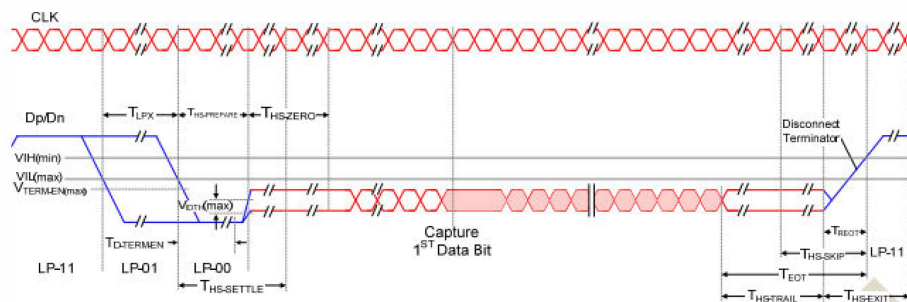**Table 11.12: Data to Clock Timing Specifications**

Burst Mode Data Transmission

Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40 + 4*UI$	-	$85 + 6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145 + 10*UI$	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	$35 + 4*UI$	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	$85 + 6*UI$	-	$145 + 10*UI$	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$max(n*8*UI, 60 + n*4*UI)$	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns
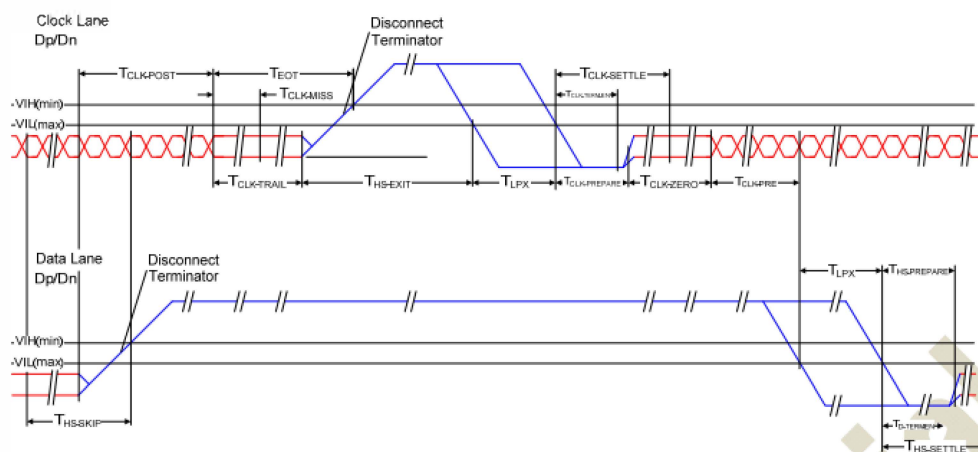
**Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode**

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

8.1.2Timing for MIPI Characteristics.

Iten	Symbol	Valaues	Unit
Frame Rate	Fr	60	Hz
Clock Frequency	1/Tc	60	MHz
Hor. Display Period	tHD	800	clk (pixel)
HS Period	tH	960	clk (pixel)
HSYNC Width	tHW	20	clk (pixel)
HSYNC BP	tHBP	70	clk (pixel)
HSYNC FP	tHFP	70	clk (pixel)
Vertical Display Period	tvd	1280	line
VS Period	tv	1324	line
VSYNC Width	tVW	6	line
VSYNC BP	tVBP	22	line
VSYNC FP	tVFP	16	line

Note: One frame length = 16.67ms, One line length = 12.78us.
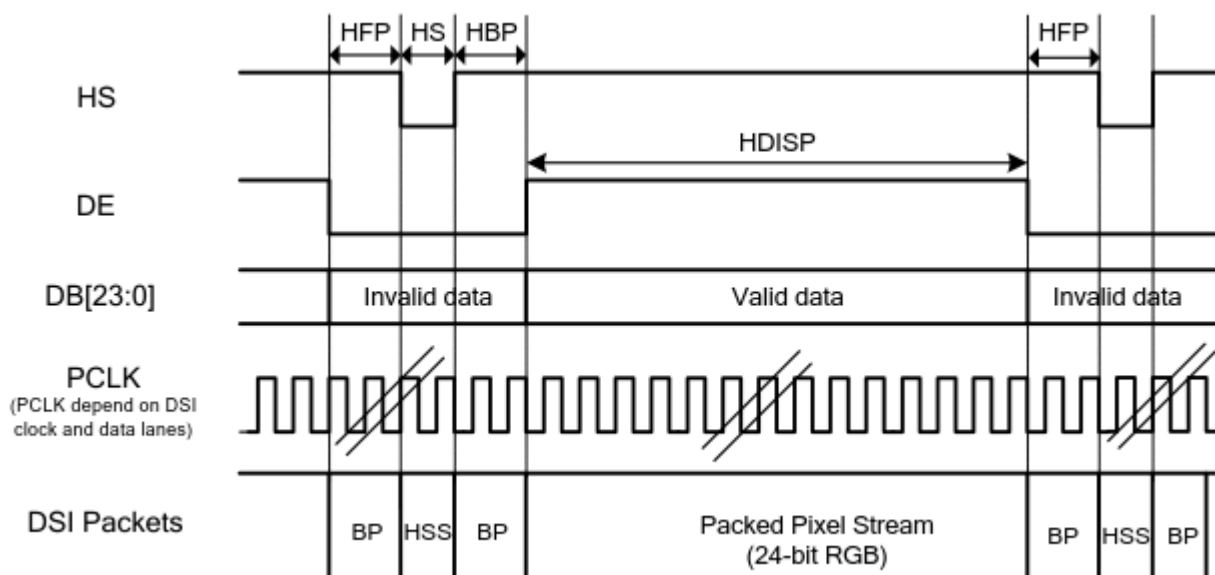
9.0 Reliability Test Items

9.1 Temperature and Humidity

Test Item 测	Test Condition	Remark
High Temperature Storage	+70℃±3℃,48hrs	
Low Temperature Storage	-30℃±3℃,48hrs	
High Temperature Operation	+60℃±3℃,48hrs	
Low Temperature Operation	-20℃±3℃,48hrs	
High Temperature and High Humidity Operation	+50℃±3℃, 90%±3%RH,48hrs	
Thermal Shock	-20℃/0.5h~+60℃/1h for a total 10 cycles	
Image Sticking	25℃,4hrs	Note1

Note: (1) All tests above are practiced at module type.
 (2) There is no display function NG issue occurred, All the cosmetic specification is judged before the
reliability stress.

10.0 Packing form

TBD

11.0 General Precaution

11.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

11.2 Asembly Precaytton

10.2.1 Please use the mounting hole on the module side in installing and do not bending or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.

10.2.2 Please design display housing in accordance with the following guide lines.

10.2.2.1 Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.

10.2.2.2 Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. The clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.

10.2.3 Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)

10.2.4 Please do not press any parts on the rear side such as source IC, gate IC, and FPC during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.

10.2.5 Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.

10.2.6 Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.

10.2.7 Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

11.3 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

11.4 Breakage of LCD Panel

10.4.1 If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

10.4.2 If liquid crystal contacts mouth or eyes, rinse out with water immediately.

10.4.3 If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

10.4.4 Handle carefully with chips of glass that may cause injury, when the glass is broken.

11.5 Absolute Maximum Ratings and Power Protection Circuit

10.5.1 Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

10.5.2 Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

10.5.3 It's recommended employing protection circuit for power supply.

11.6 Operation

10.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

10.6.2 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

10.6.3 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

10.6.4 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

11.7 Static Electricity

10.7.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

10.7.2 Because LCD module uses CMOS-IC on TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge.

10.7.3 Persons who handle the module should be grounded through adequate methods.

11.8 Disposal

When disposing LCD module, obey the local environmental regulations.

11.9 OTHERS

10.9.1 A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight land strong UV rays.

10.9.2 Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.

10.9.3 For the packaging box, please pay attention to the followings:

10.9.3.1 Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.

10.9.3.2 Please do not pile them up more than 6 boxes. (They are not designed so.) And please do not turn over.

10.9.3.3 Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.

10.9.3.4 Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

深圳市丽台电子有限公司

Shenzhen Leadtek Electronics Co.,Ltd

Quality Inspection Standards

品质允收标准

Model No. / 产品型号： **Applies 5.5~10.0 Inch Touch Display Screen**

Updated Date /生效日期： **2022-05-20**

Version / 版 本： **A0**

Customer confirmation ： _____

Record of Revision /修订履历

Version /版本	Revision Record /修订内容	Reviser /修订人	Revision Date /修订日期
V0	首发 / Starting	Green	2022.05.20

1.Scope of application /适用范围.

This document shall be applied to 5.5~10.0 inch touch display screen.

本文件适用于5.5~10.0 寸触摸显示屏.

2.Inspection conditions and environment /检验条件与环境.

2. 1 Inspection Conditions /检验条件:
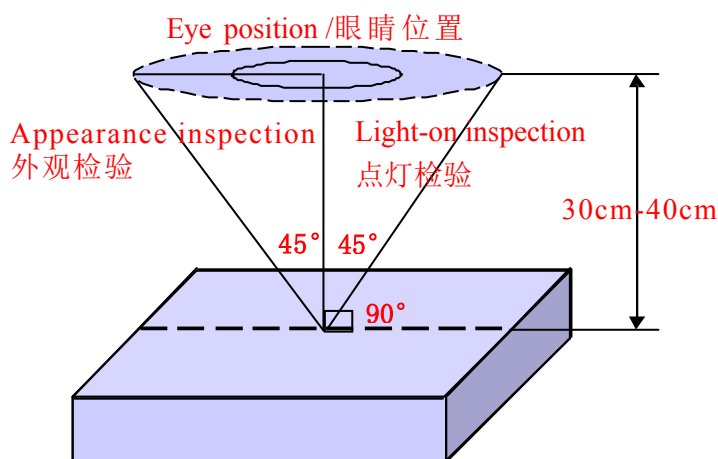
(1) Inspection Distance /检测距离: 35cm ±5cm.

（2）Check time /检验时间：

Displays performance test /功能测试：2~3S /Image，Cosmetic Inspection /外观检验:10~12S.

(3) Check the viewing angle /检验视角:

Light-on Inspection Angle /点灯检验角度：±45°.

Cosmetic Inspection Angle /外观检验角度：±45°.

(Perpendicular to LCD panel surface /垂直于LCD表面)

2.2 Inspection environment /检验环境:

Ambient Temperature 温度		25℃±5℃
Ambient Humidity 湿度		55±5%RH
Ambient Illumination 亮度	Cosmetic Inspection 外观检验	800-1000 Lux
	Functional Inspection 点灯检验	200~300Lux

2.3 Sampling Conditions /抽样条件:

（1）Quantity to be inspected /批量：Quantity of shipment lot per model /单次运送单一型号数量.

（2）Sampling method /抽样方法：

	GB/T 2828.1- 2003
Sampling Plan /抽样计划	Normal Inspection ， Single Sampling 正常检验、单次抽样
	General inspection level： Ⅱ 一般检验水平：二级
AQL	Major Defect /主要缺陷	0.65
	Minor Defect /次要缺陷	1.0

（3）The classification of Major(MA) and Minor(MI) defects is shown as "3.1 Classification of defects".

主缺(MA)及次缺(MI)定义于"3.1缺陷分类".

3.Terms And Definitions /术语和定义

3.1 Classification of defects / 缺陷分类：

（1）Major defects /主要缺陷:

A major defect is a defect that is likely to result in failure, or to reduce materially the usability of the product for its intended purpose .

可导致产品功能失效或减少产品可用性的缺陷.

（2）Minor defects /次要缺陷:

It will not cause the product to fail and reduce the defects in the effective use and operation of the product.

不会导致产品功能失效和减少产品的有效使用与操作的缺陷.

3.2 Point defects /点状缺陷：

The size of the point defect is defined by the diameter D, and the average diameter of the defect is
D=1/2（W+L）.

点状缺陷的大小是由直径 D 定义的，缺陷的平均直径 D=1/2(W+L).

3.3 Linear defects /线状缺陷：

When defect size L≥2W,the defect count as liner type defect.Size of linear defect is defined by length (L) and the maximum width (W).

当缺陷尺寸 L≥2W 时，被视为线状缺陷，线状缺陷是由长度 (L) 和最大宽度 (W) 定义的.

3
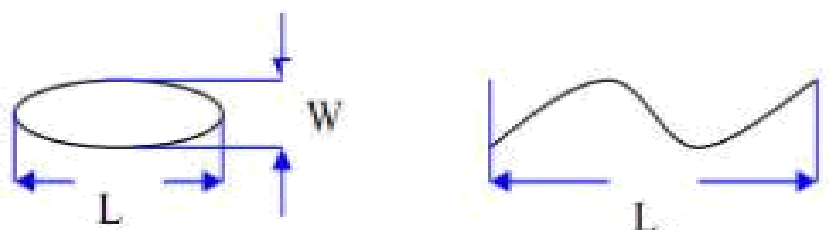
3.4 LCD sub-pixel dot /LCD子像素点

（1）Definition /定义 ：The point defect area is greater than 50% of the LCD sub-pixel area, and is visible through ND5% filter masking .

子像素点缺陷面积大于 50% LCD子像素面积, 且透过 ND5%遮盖是可见的.

（2）The drawing of 1/2 area sub-pixel definition / 1/2 面积的子像素定义绘图:

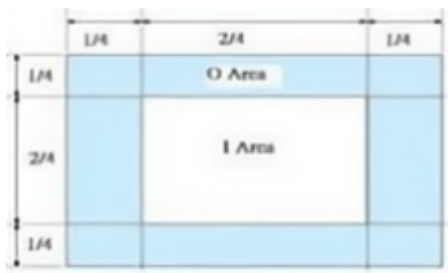The 1/2 area sub-pixel can be defined as below one or more of specific shapes

1/2 面积的子像素可以定义为如下一个或多个特定形状图：

3.5 Small bright dot /细碎亮点：

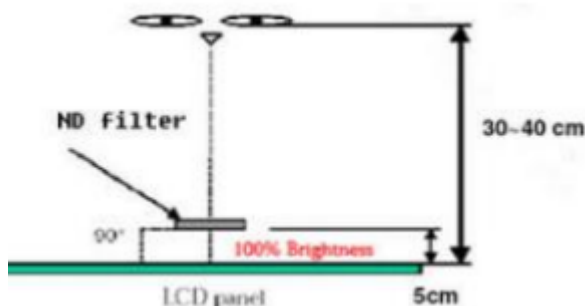Point defects smaller than "LCD sub-pixels" /小于"LCD子像素点"的点缺陷.

（Ratio of Zone I to Zone O /I 区与 O 区比例：1：2：1）

3.6 ND filter inspection method /ND卡的检验方法：

Hold the ND filter about 5cm above the display area, with your eyes 30-40cm away from the panel, and observe for 2~3 seconds.

在显示区域上方大约 5cm 处握住 ND 卡，眼睛距离面板 30-40cm，观察2~3 秒.

3.7 Any FPC surface problems that do not leak copper on the surface and do not cause functional failure are acceptable.
任何 FPC 表面问题，表面未露铜和不造成功能失效是可以接受.

3.8 Extraneous substances that can be wiped out ，like Finger point,Particles are not considered as a defect .
可以被擦拭干净的表面物质不视为缺陷 (如手指印，尘粒) .

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3.9 Defects that can be covered by the material and are not visible in appearance are not considered defects.

能被物料覆盖，外观不可见的缺陷不视为缺陷.

3.10 Panel damage /面板损伤：

Glass damage outside the AA display area that does not affect the effective wiring is acceptable.

AA 显示区域以外的玻璃损伤，不影响有效线路是可以接受的.

3.11 Issues not specified or defined in this acceptance standard shall be handled through friendly negotiation between the two parties.

本允收标准中未规定或定义的问题，双方友好协商处理.

4. Inspection standards /检验标准

4.1 Structural Dimensions /结构尺寸规格

Serial Number 序号	Measurement items /测量项目		Specification /规格	Remark /备注
	名称 /Name	Unit /单位	Tolerance /公差	
1	Outside dimension：Length 尺寸：长	mm /毫米	0.15mm~0.30mm	Please refer to the product specification for detailed dimensions and tolerances 详细的尺寸规格和公差请参考产品规格书
2	Outside dimension：Width 尺寸：宽	mm /毫米	0.15mm~0.30mm	
3	Outside dimension：Thickness 尺寸：高	mm /毫米	0.20mm~0.50mm	

4.2 Appearance Inspection Specification /外观检验规格
（D：diameter，　W：width，　L：length，　N：quantity，　DS：spacing）

Inspection area 检验区域	Inspection items 检验项目	Inspection specifications 检验规格	Defect category 缺陷类别	
Glass 玻璃	Wire(on Array) 线路	Can't be damaged 不能损伤	MA	
	Chipping/corner breaking 崩边/破角	Can't affect the effective lines and functions 不能影响有效线路和功能	MA	
	Edge 边缘	There must be no extensional cracks 不可有延伸性裂纹	MA	
Silicone 硅胶	Silicone coating 硅胶涂布	The height must not exceed the LCD CF surface 高度不能超过LCD CF面		MI
	Glue overflow 溢胶	Can't cover FPC, POL, etc 不能覆盖到FPC、POL等		MI

Inspection area 检验区域	Inspection items 检验项目	Inspection specifications 检验规格	Defect category 缺陷类别	
PCBA FPC Connector 连接器	Appearance 外观	Scratches or injuries are not allowed to cause copper exposure 划伤或损伤不允许表面出现露铜		MI
	Component 元器件	Can't be damaged and lack 不能损伤和缺少	MA	
	Goldfinger oxidation 金手指氧化	Not allowed 不允许		MI
	Connection status 连接状况	The connection must be accurate and stable 必须准确稳定连接	MA	
	Break 破裂	Not allowed 不允许	MA	
	Soldering,：false soldering/tinning/tin beads 假焊/连锡/锡珠	Not allowed 不允许	MA	
POL 偏光片	Scratches 划伤	1. W≤0.07mm；L≤5mm，Ignore（忽略） 2. 0.07mm＜W≤0.12mm；L≤5mm；N≤4；DS≥10mm 3. 0.12mm＜W；5mm＜L，Not allowable（不允许）		MI
	Dent 凹凸印	1. D≤0.20mm，Ignore（忽略） 2. 0.20mm＜D≤0.40mm；N≤4；DS≥10mm 3. 0.40mm＜D，Not allowable（不允许）		MI
	Bubbles 气泡	1. D≤0.20mm，Ignore（忽略） 2. 0.20mm＜D≤0.40mm；N≤4；DS≥10mm 3. 0.40mm＜D，Not allowable（不允许）		MI
	Point defects 点状不良	1. D≤0.20mm，Ignore（忽略） 2. 0.20mm＜D≤0.40mm；N≤4；DS≥10mm 3. 0.40mm＜D，Not allowable（不允许）		MI
	Edge bubbles 边缘气泡	1. Within 1/2BM of the display area, it is not allowed 显示区往外 1/2BM 区域内，不允许 2. The display area is 1/2 outside the BM area, and it is not controlled 显示区往外1/2BM区域以外，不管控		MI
	Dirty/watermarked 脏污/水印	No dirt/water lines/finger marks are allowed, and must be wiped clean 不允许有脏污/水纹/手指印，须擦拭干净方可		MI
	Warping 起翘	Not allowed 不允许		MI
	Attaching offset 贴偏	It is necessary to completely cover the display area outward, within the 1/2BM area, or without leaking POL edges after TP is attached 需完整覆盖显示区往外、1/2BM区以内或贴合TP后不会出现漏偏光片边缘		MI
	Mixture 混料	Mixing different types of POL or not using POL as required by the BOM，not allowed 不允许混贴不同型号的POL或未按BOM要求使用POL	MA	

Inspection area 检验区域	Inspection items 检验项目	Inspection specifications 检验规格		Defect category 缺陷类别
TP&CG	Point defects 点状不良	1. D≤0.20mm，Ignore（忽略） 2. 0.20mm＜D≤0.40mm；N≤4；DS≥10mm 3. 0.40mm＜D，Not allowable（不允许）		MI
	Scratches 划伤	1. W≤0.07mm；L≤5mm，Ignore（忽略） 2. 0.07mm＜W≤0.12mm；L≤5mm；N≤4；DS≥10mm 3. 0.12mm＜W；5mm＜L，Not allowable（不允许） 4. There is a feeling scratch，Not allowable 有感划伤，不允许		MI
	Edges and corners cracked 崩角/崩边	1. Product front /产品正面：Edge and corner chipping is not allowed 崩角、崩边不允许 2. Product back /产品背面: X≤ 0.5，Y≤0.5，Z≤1/2T；N≤4；DS≥10mm		MI
	Silk screen 丝印	The silk screen is clear, complete and correct 丝印清晰、完整、内容正确		MI
	Dirty 脏污	Non-wipeable dirt, not allowed 不可擦拭的脏污，不允许		MI
	Broken 破损	Not allowable 不允许	MA	
	Ink color aberration 油墨色差	ΔE>1，Not allowable（不允许）		MI
	Cover pinholes 针孔	1. D≤0.15mm，N≤4，DS≥10mm，allowable 2. D＞0.15mm，intensive pinholes（密集型针孔），Not allowable（不允许）		MI
	IR holes IR孔	Dirt, deviation, color difference, etc. are not allowed 不允许脏污、偏位、色差等		MI
BL 背光	Backlight separation 背光分离	Not allowable 不允许		MI
	Deformation of rubber iron and rubber frame 胶铁、胶框变形	Use the plug gauge 0.3mm on the flat surface and can snap in and judge NG 在平面上使用塞规0.3mm卡翘曲位置，能卡进判定NG		MI
	The iron frame is oxidized and not tightened 铁框氧化、卡不紧	Not allowable 不允许		MI
	Backlight sticky solder beads, glue, etc 背面粘锡珠、残胶等	Not allowable 不允许		MI
	Lnkjet coding，Barcode，QR code 喷码/条码/二维码	The lnkjet coding is clear and complete, the barcode and QR code can be scanned normally, and the content and format match 喷码清晰完整、条码和二维码可正常扫描，内容和格式相符		MI
	Accessories(protective film, double-sided tape, insulating adhesive, etc.) 辅料（保护膜、双面胶、绝缘胶等）	Defects such as missing pastes, sticking deviations, defects, and fractures are not allowed 不允许有漏贴、贴偏、残缺、断裂等缺陷		MI

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4.3 Electrical test specifications /电性检查规格
（D：diameter,　W：width,　L：length,　N：quantity,　DS：spacing）

Inspection items 检验项目	Inspection specifications 检验规格	Defect category 缺陷类别	
Glass bright spots/dark spots 玻璃亮点/暗点	1. D≤0.20mm，Ignore（忽略） 2. 0.20mm＜D≤0.40mm；N≤4；DS≥10mm 3. 0.40mm＜D，Not allowable（不允许）		MI
Mura	Use ND5% filter masking, visual invisibility is OK, 200~300Lux 使用ND5%遮盖，目视不可见即为OK，200~300Lux		MI
Small bright dot 细碎亮点	Use ND5% filter masking, visual invisibility is OK 使用ND5%遮盖，目视不可见即为OK		MI
Light leakage 漏光	1. Use ND5% filter masking, visual invisibility is OK 使用ND5%遮盖，目视不可见即为OK 2. If necessary, sign off on the sample 必要时，签限定样		MI
Backlight black/white dots 背光黑点/白点	1. D≤0.20mm，Ignore（忽略） 2. 0.20mm＜D≤0.40mm；N≤4；DS≥10mm 3. 0.40mm＜D，Not allowable（不允许）		MI
Linear foreign bodies 线状异物（异物毛丝等）	1. W≤0.07mm；L≤5mm，Ignore（忽略） 2. 0.07mm＜W≤0.12mm；L≤5mm；N≤4；DS≥10mm 3. 0.12mm＜W；5mm＜L，Not allowable（不允许）		MI
Black/White Print 黑印/白印	Use ND5% filter masking, visual invisibility is OK 使用ND5%遮盖，目视不可见即为OK		MI
The display is uneven 显示不均匀	Use ND5% filter masking, visual invisibility is OK 使用ND5%遮盖，目视不可见即为OK		MI
The brightness is uneven 亮度不均匀	Brightness uniformity＜85.0%，Not allowable 亮度均匀性＜85.0%，不允许		MI
Displacement of the membrane 膜材移位	Not allowable 不允许		MI
Interference pattern/Newtonian pattern 干涉纹/牛顿纹	Not allowable 不允许		MI
Display abnormal 显示异常	Not allowable 不允许	MA	
No display 无显示	Not allowable 不允许	MA	
Line/Missing Drawing 线条/缺画	Not allowable 不允许	MA	
Splash screen 闪屏	Not allowable 不允许	MA	
LCD grid LCD网格	Not allowable 不允许	MA	
Afterimage 残影	Not allowable 不允许	MA	
Wrong viewing angle 视角错误	Not allowable 不允许	MA	
No touch 无触摸	Not allowable 不允许	MA	
Touch the jump point 触摸跳点	Not allowable 不允许	MA	
Not sensitive 触摸不灵敏	Not allowable 不允许	MA	