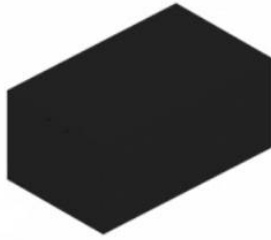


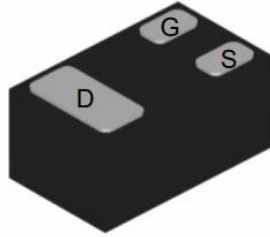


N-Channel Enhancement Mode Field Effect Transistor

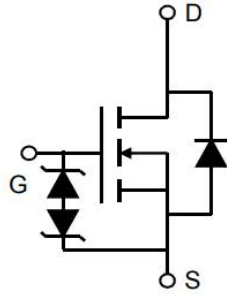
Top View



Bottom View



DFN1006-3L



Product Summary

- V_{DS} 20 V
- I_D 0.7 A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <300 mohm
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) <350 mohm
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) <700 mohm
- ESD Protected Up to 2.0KV (HBM)

General Description

- Trench Power LV MOSFET technology
- High Power and current handing capability

Applications

- PWM application
- Load switch

■ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	± 12	V
Drain Current	$T_A=25^{\circ}C$ @ Steady State	I_D	0.7	A
	$T_A=70^{\circ}C$ @ Steady State		0.56	
Pulsed Drain Current ^A		I_{DM}	2.8	A
Total Power Dissipation @ $T_A=25^{\circ}C$		P_D	0.9	W
Thermal Resistance Junction-to-Ambient @ Steady State		$R_{\theta JA}$	138	$^{\circ}C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^{\circ}C$

■ Ordering Information

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJA3134KA	F1	34	10000	100000	400000	7" reel



YJA3134KA

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ± 10V, V _{DS} =0V		2.0	± 10	μA
		V _{GS} = ± 8V, V _{DS} =0V		500	± 2000	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	0.35	0.75	1.1	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 4.5V, I _D =0.6A		180	300	mΩ
		V _{GS} = 2.5V, I _D =0.5A		260	350	
		V _{GS} = 1.8V, I _D =0.2A		415	700	
Diode Forward Voltage ^C	V _{SD}	I _S =0.7A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				0.7	A
Dynamic Parameters ^B						
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, f=1MHZ		56		pF
Output Capacitance	C _{oss}			20		
Reverse Transfer Capacitance	C _{rss}			2.5		
Gate Resistance	R _g	f=1 MHz, Open drain		50		Ω
Switching Parameters ^B						
Total Gate Charge	Q _g	V _{GS} =4.5V, V _{DS} =10V, I _D =0.5A		1		nC
Gate Source Charge	Q _{gs}			0.28		
Gate Drain Charge	Q _{gd}			0.22		
Reverse Recovery Chrage	Q _{rr}	I _F =0.5A, di/dt=20A/us		0.4		ns
Reverse Recovery Time	t _{rr}			14.4		
Turn-on Delay Time	t _{D(on)}	V _{GS} =4.5V, V _{DD} =10V, R _G =10Ω, I _D =500mA		2		
Turn-on Rise Time	t _r			18.8		
Turn-off Delay Time	t _{D(off)}			10		
Turn-off Fall Time	t _f			23		

A. Repetitive Rating: Pulse width limited by maximum junction temperature.

B. These parameters have no way to verify.

C. Pulse Test: Pulse Width≤300us, Duty Cycle≤0.5%.



■ Typical Performance Characteristics

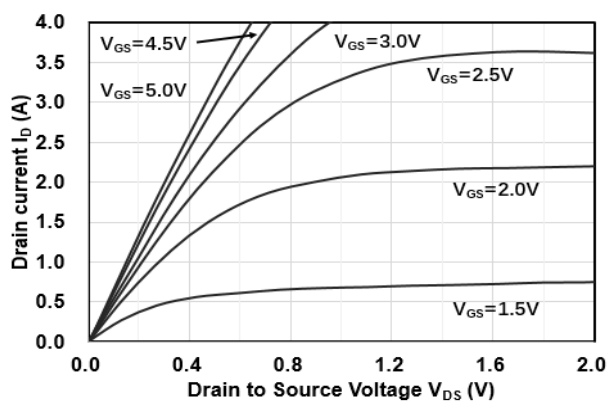


Figure1. Output Characteristics

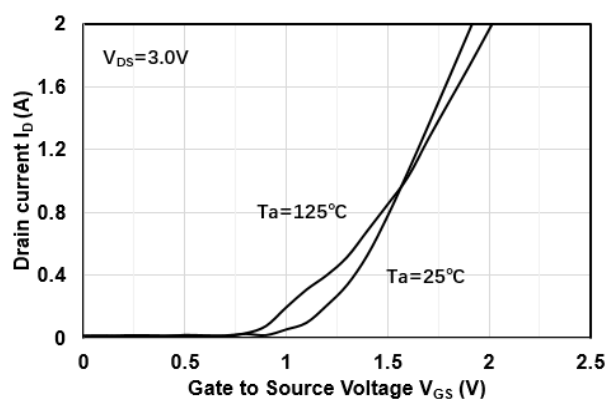


Figure2. Transfer Characteristics

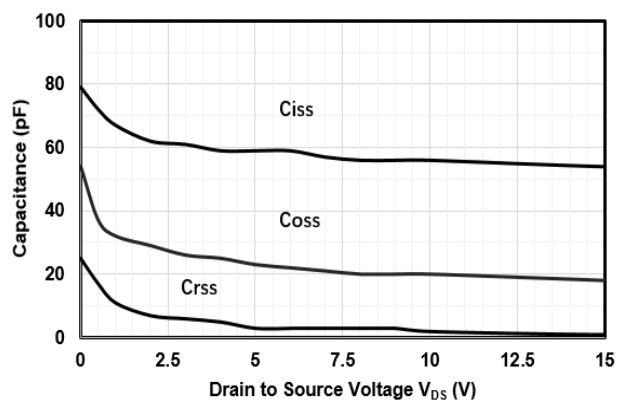


Figure3. Capacitance Characteristics

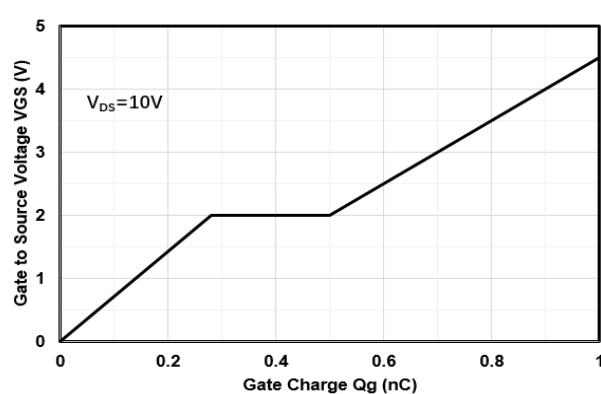


Figure4. Gate Charge

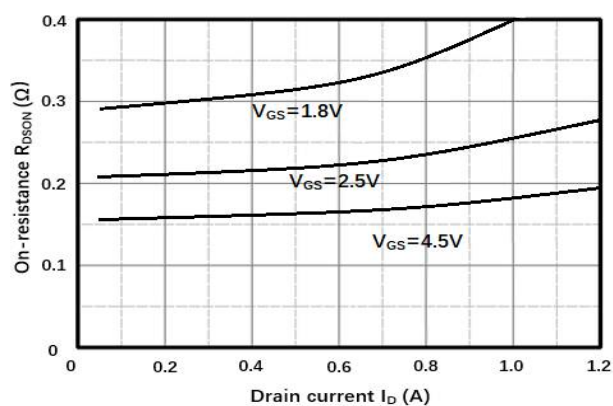


Figure5. Drain-Source on Resistance

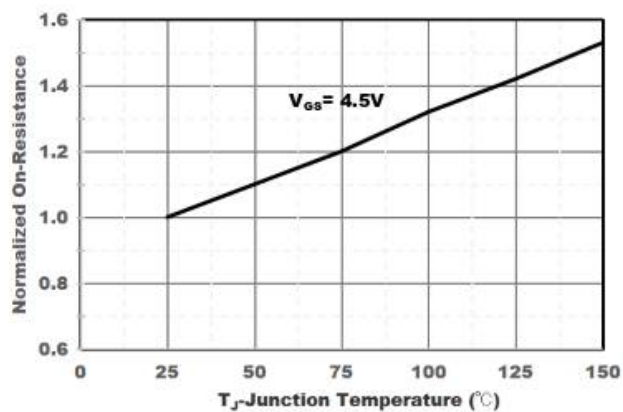


Figure6. Drain-Source on Resistance

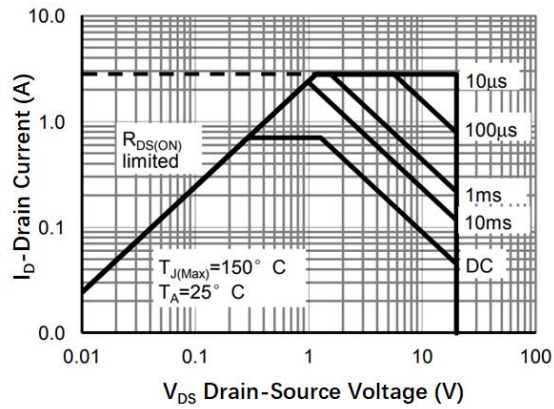


Figure7. Safe Operation Area

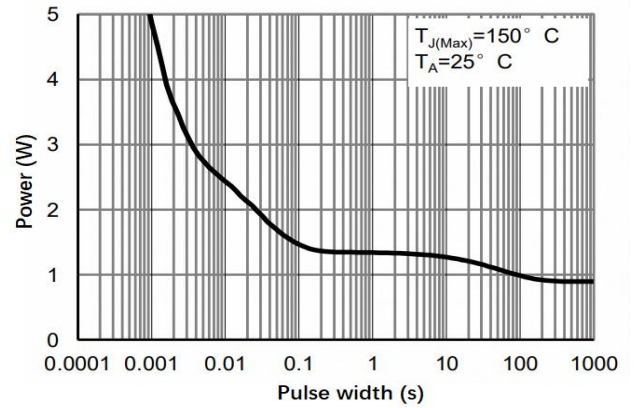


Figure8. Pulse Power Rating Junction-to Ambient

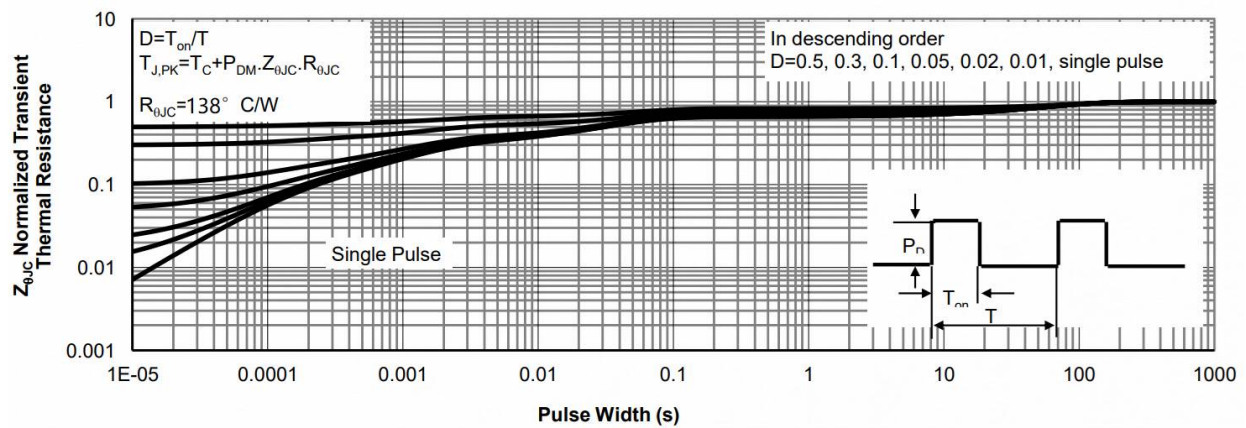
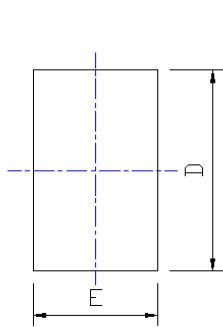


Figure9. Normalized Maximum Transient Thermal Impedance

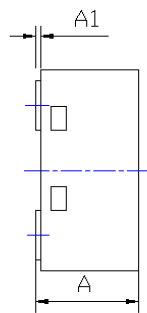


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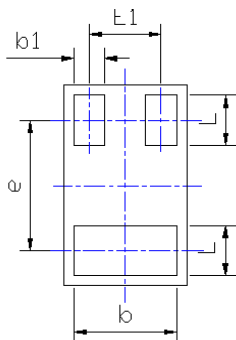
■DFN1006-3L Package information



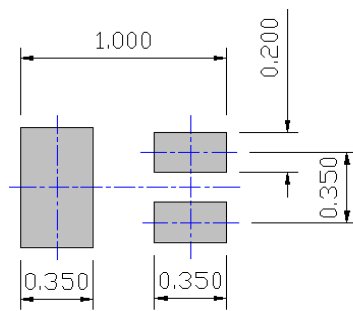
TOP VIEW



SIDE VIEW



BOTTOM VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS		
	Millimeter		
	MIN.	NOM.	MAX.
A	0.42	---	0.55
A1	0.025REF		
b	0.45	0.50	0.55
b1	0.10	0.15	0.20
D	0.95	1.00	1.05
E	0.55	0.60	0.65
E1	0.35BSC		
e	0.65BSC		
L	0.20	0.25	0.30

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE LEAD BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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