RoHS compliant
850 nm Multi-mode Transceiver (1000BASE-SX)
2×5, LC Duplex Connector, 3.3 V
1.0625Gbd Fiber Channel/1.25 Gigabit Ethernet

Features

- RoHS compliant
- Compliant with IEEE 802.3z Gigabit Ethernet standard
- Compliant with Fiber Channel standard
- Industry standard 2×5 footprint
- LC duplex connector
- Single power supply 3.3V
- Class 1 laser product complies with EN 60825-1

Ordering Information

PART NUMBER	INPUT/OUTPUT	SIGNAL DETECT	VOLTAGE	TEMPERATURE
LM24-C3S-TC-B	AC/AC	LVTTL	3.3V	0°C to 70 °C
LM24-C3S-TI-B	AC/AC	LVTTL	3.3V	-10°C to 85 °C

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	–40	85	°C	
Supply Voltage	*Vcc*	–0.5	4.0	V	
Input Voltage	V_{IN}	–0.5	*Vcc*	V	
Operating Current	I_{OP}	---	400	mA	
Soldering Temperature	T_{SOLD}	---	260	°C	10 seconds on leads

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Operating Environment

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Case Operating Temperature	T_C	0 -10	70 85	°C	
Supply Voltage	*Vcc*	3.1	3.5	V	
Supply Current	*Icc*	---	200	mA	

Transmitter Electro-optical Characteristics

***Vcc* = 3.1 V to 3.5 V, T_C = 0 °C to 70 °C (-10 °C to 85 °C)**

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Output Optical Power 62.5/125 μm, fiber	*Pout*	–9.5	---	-4	dBm	
Output Optical Power 50/125 μm, fiber	*Pout*	–9.5	---	-4	dBm	
Extinction Ratio	*ER*	9	---	---	dB	
Center Wavelength	λ_C	830	850	860	nm	
Spectral Width (RMS)	$\Delta\lambda$	---	---	0.85	nm	
Rise/Fall Time (20–80%)	$T_{r,\,f}$	---	---	260	ps	
Relative Intensity Noise	*RIN*	---	---	–117	dB/Hz	
Total Jitter	*TJ*	---	---	227	ps	
Output Eye			Compliant with IEEE802.3z			
Max. P_{out} TX-DISABLE Asserted	P_{OFF}	---	---	–45	dBm	
Disable input voltage- High	$T_{dis\text{-}H}$	2.2	---	---	V	
Disable input voltage- Low	$T_{dis\text{-}L}$	---	---	0.6	V	
Transmitter Data Input Differential Voltage	V_{DIFF}	0.4	---	2.0	V	

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Receiver electro-optical characteristics

Vcc = 3.1 V to 3.5 V, T_C = 0 °C to 70 °C (-10 °C to 85 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Optical Input Power-maximum	P_{IN}	0	---	---	dBm	BER < 10^{-12}
Optical Input Power-minimum (Sensitivity)	P_{IN}	---	---	–18	dBm	BER < 10^{-12}
Operating Center wavelength	λ_C	770	---	860	nm	
Optical Return Loss	ORL	12	---	---	dB	
Signal Detect-Asserted	P_A	---	---	–18	dBm	
Signal Detect-Deasserted	P_D	–35	---	---	dBm	
Signal Detect-Hysteresis	$P_A - P_D$	1.0	---	---	dB	
Signal Detect Voltage -High	V_{OH}	2.4	---	Vcc	V	
Signal Detect Voltage -Low	V_{OL}	0	---	0.5	V	
Data Output Rise, Fall Time (20–80%)	$T_{r,f}$	---	---	0.35	ns	
Data Output Differential Voltage	V_{DIFF}	0.5	---	1.8	V	

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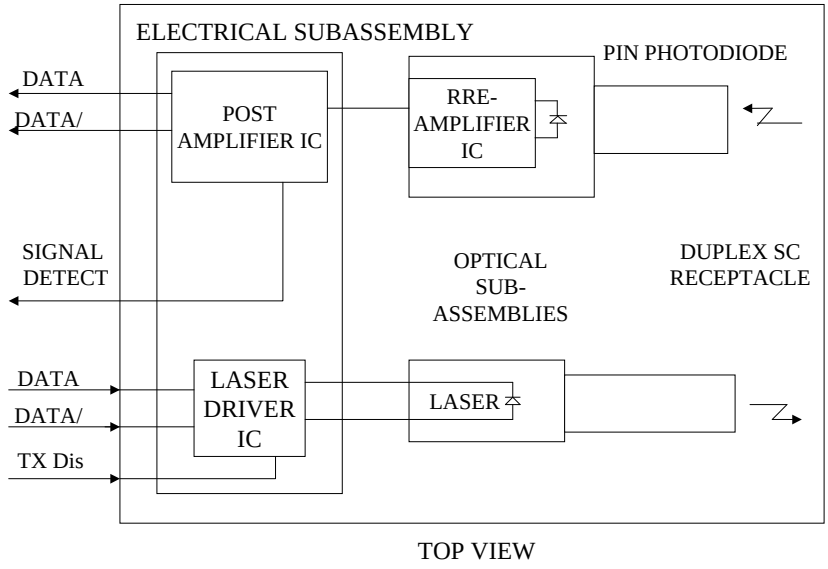
Block Diagram of Transceiver



Transmitter Section

The transmitter section consists of a 850 nm laser in an eye safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LD driver IC which converts differential input LVPECL logic signals into an analog laser driving current.

Receiver Section

The receiver utilizes a MSM detector integrated with a trans-impedance preamplifier in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

Receiver Signal Detect

Signal Detect is a basic fiber failure indicator. This is a single-ended LVTTL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 1.0 dB higher than the deassert level.

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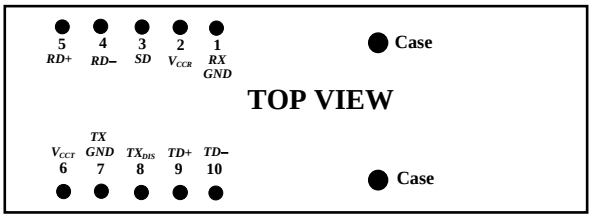
Connection Diagram

Pin-Out



PIN	SYMBOL	DESCRIPTION
1	*RX GND*	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	V_{CCR}	Receiver Power Supply Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
3	*SD*	Signal Detect. Normal optical input levels to the receiver result in a logic “1” output, V_{OH}, asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output V_{OL}, deasserted Signal Detect is a single-ended LVTTLoutput.
4	*RD–*	Receiver Data Output-Bar Internally ac coupled (100nF). Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
5	*RD+*	Receiver Data Output Internally ac coupled (100nF). Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
6	V_{CCT}	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	*TX GND*	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.
8	TX_{DIS}	Transmitter Disable. Connect this pin to +3.3V TTL logic high “1” to disable transmitter. To enable module connect to TTL logic low “0” or open.
9	*TD+*	Transmitter Data In. Requires an ac coupled input. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)
10	*TD–*	Transmitter Data In-Bar. Requires an ac coupled input. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)

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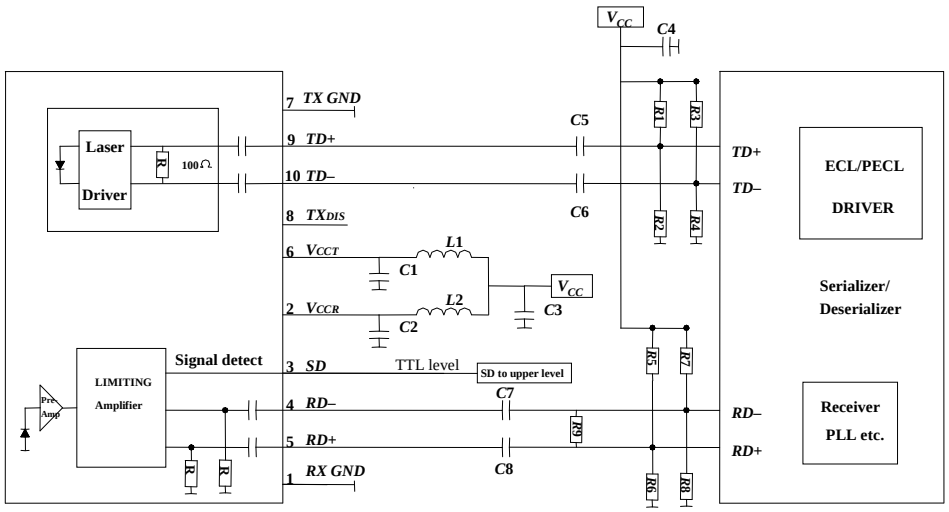
Recommended Circuit Schematic



$C1/C2/C4/C5/C6/C7/C8$ = 100 nF $C3$ = 4.7 μF $L1/L2$ = 1μH

$R1/R2/R3/R4/R5/R6/R7$/R8/R9 Depend on SerDes

In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

(1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.

(2) For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.

(3) Multi layer plane PCB is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.

(4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress *Vcc* noise over a broad frequency range, this prevents receiver sensitivity degradation due to V_{CC} noise.

(5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 μF capacitors and a surface-mount coil inductor for 1 μH inductor. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter.

(6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

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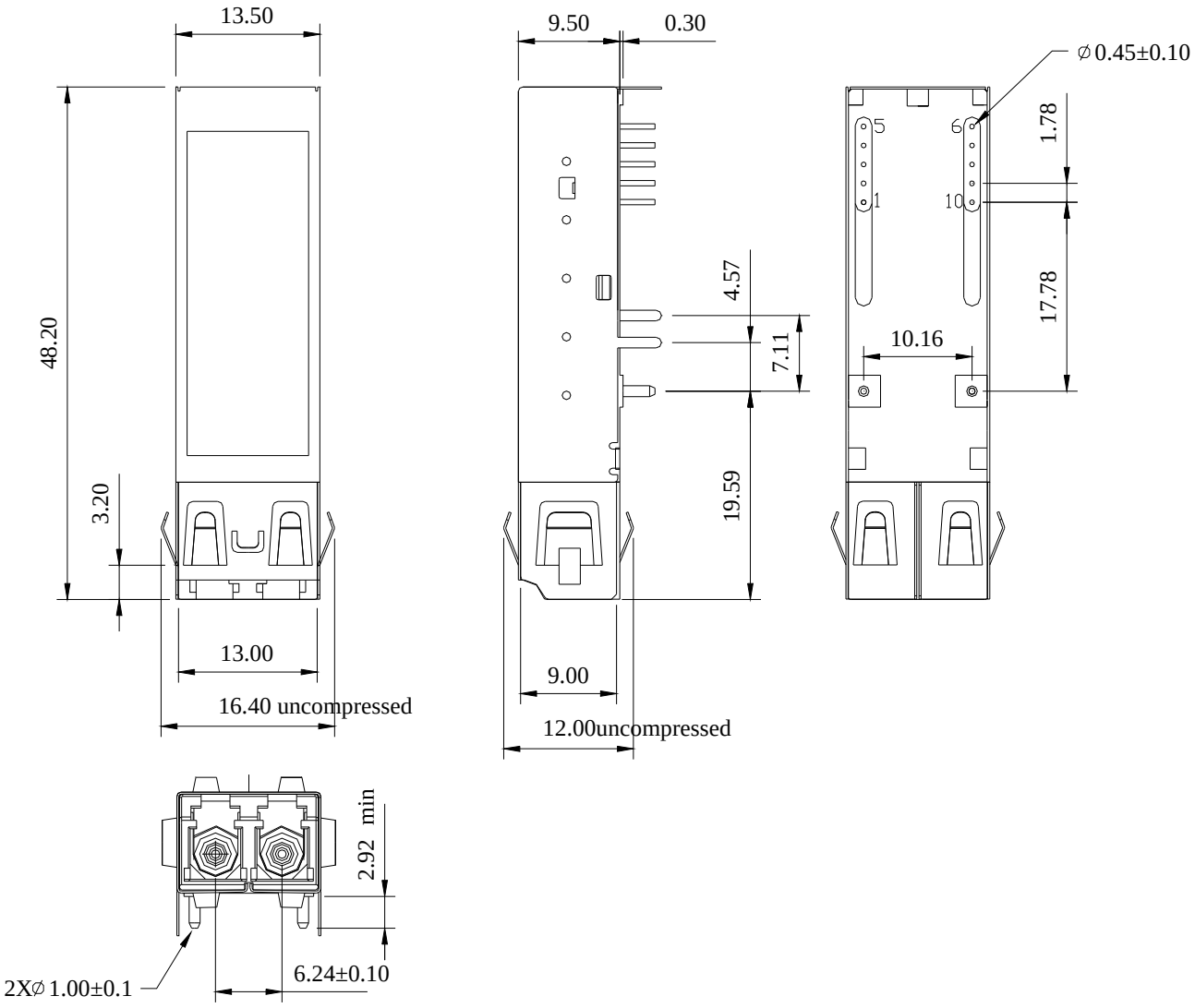
Drawing Dimensions



ALL DIMENSIONS ARE±0.20mm UNLESS OTHERWISE SPECIFIED

Unit: mm

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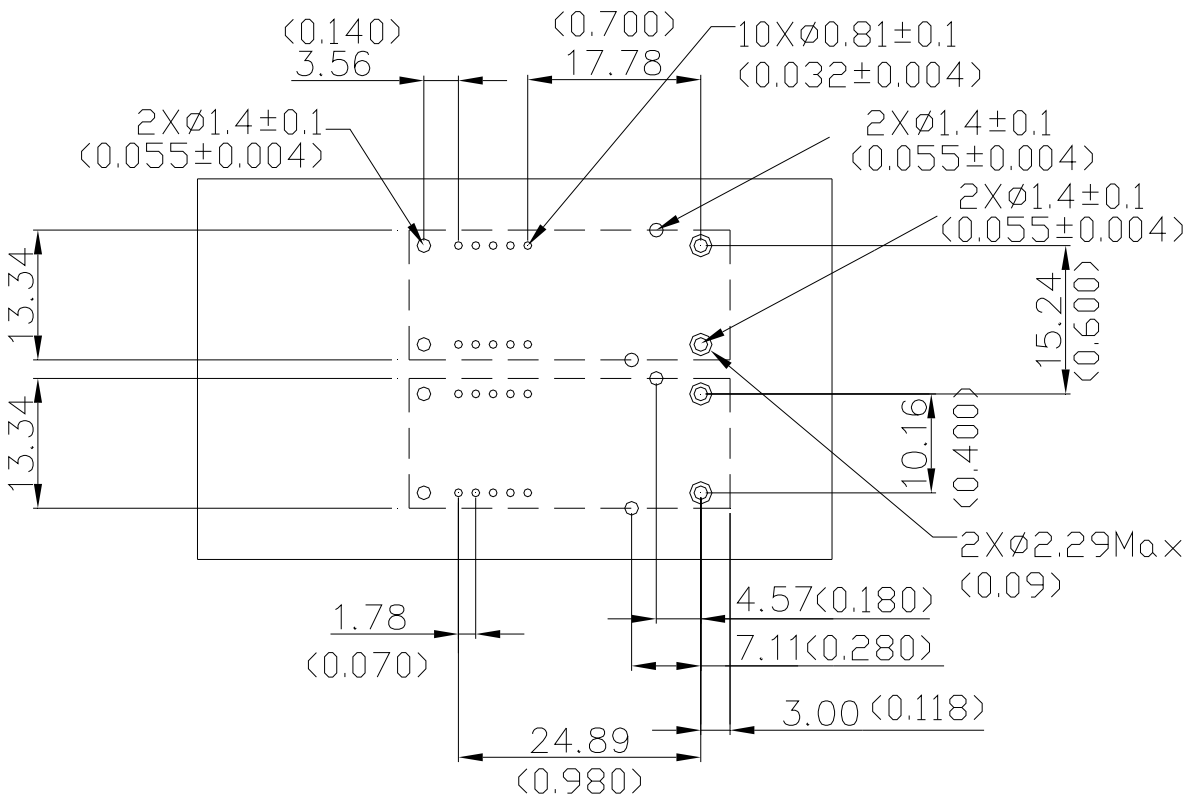
Recommended Board Layout Hole Pattern



Unit : mm(inches)

Note : All information contained in this document is subject to change without notice.

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