Zynq UltraScale+ RF SOC CRZU47DRBDevelopment Board Tutorial

Document Revision History:

time	Version	illustrate
2024.5.25	V1.0	Initial release

This tutorial will be continuously revised, optimized and supplemented based on actual development experience, providing you with more and better routines to help you become industry experts and do your best.

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Chapter 1: CRZU47DRB Development Board Introduction

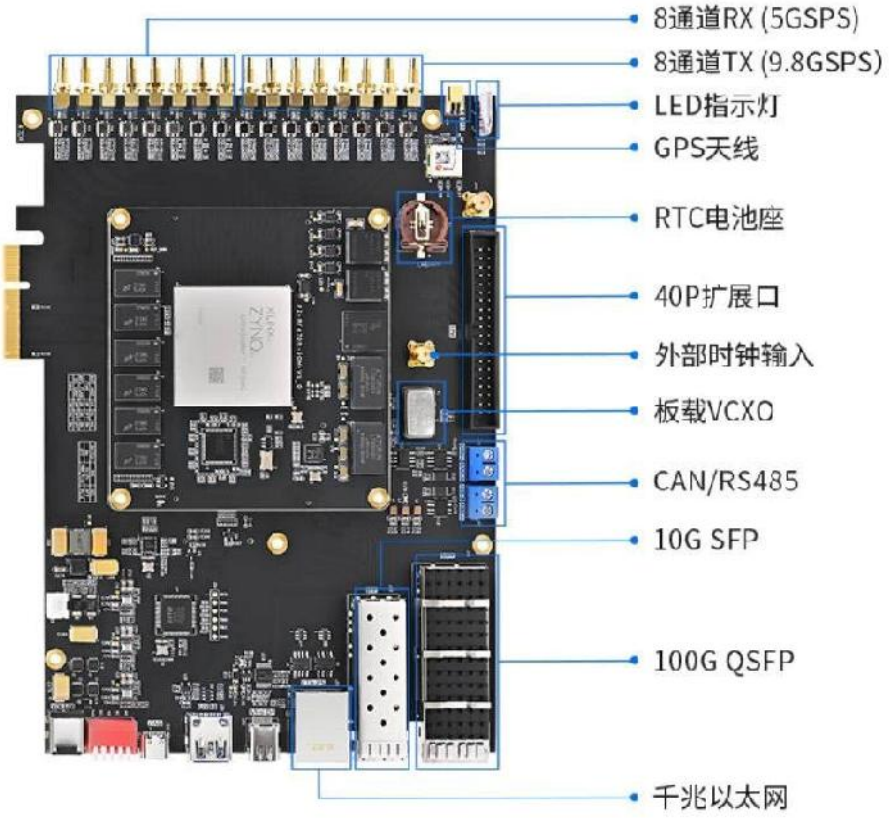
1.1 Development Board Overview

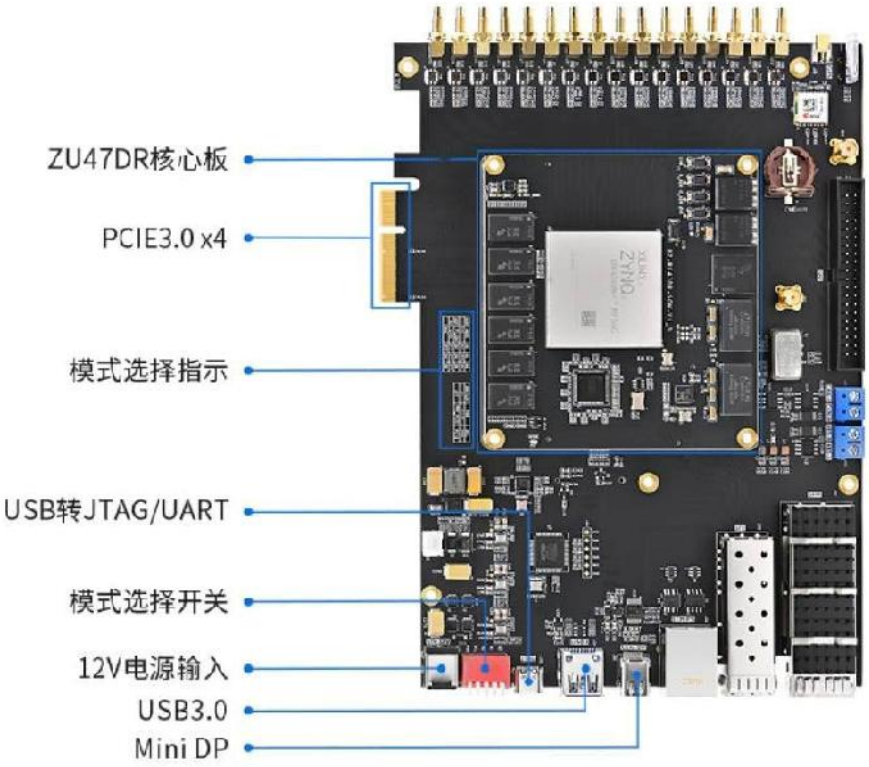
Cruetech ZYNQ UltraScale + RF SoC development board uses Xilinx 's XCZU47DR-2FFVE1156I as the main controller. The development board provides 8 groups of high- speed ADCs and 8 groups of high-speed DACs. The core board is equipped with dual groups of large-capacity DDR4 and 32GB EMMC.

In addition, the development board is also equipped with a wealth of peripheral interfaces, rich resources and powerful functions.

Cruetech ZYNQ UltraScale + The RFSoc development board is provided in the form of a core board and a baseboard. The core board is connected to the baseboard through three 0.635 pitch 240P high - speed connectors, which makes it more flexible to use. It can be used for learning and the core board can also be used for project development.

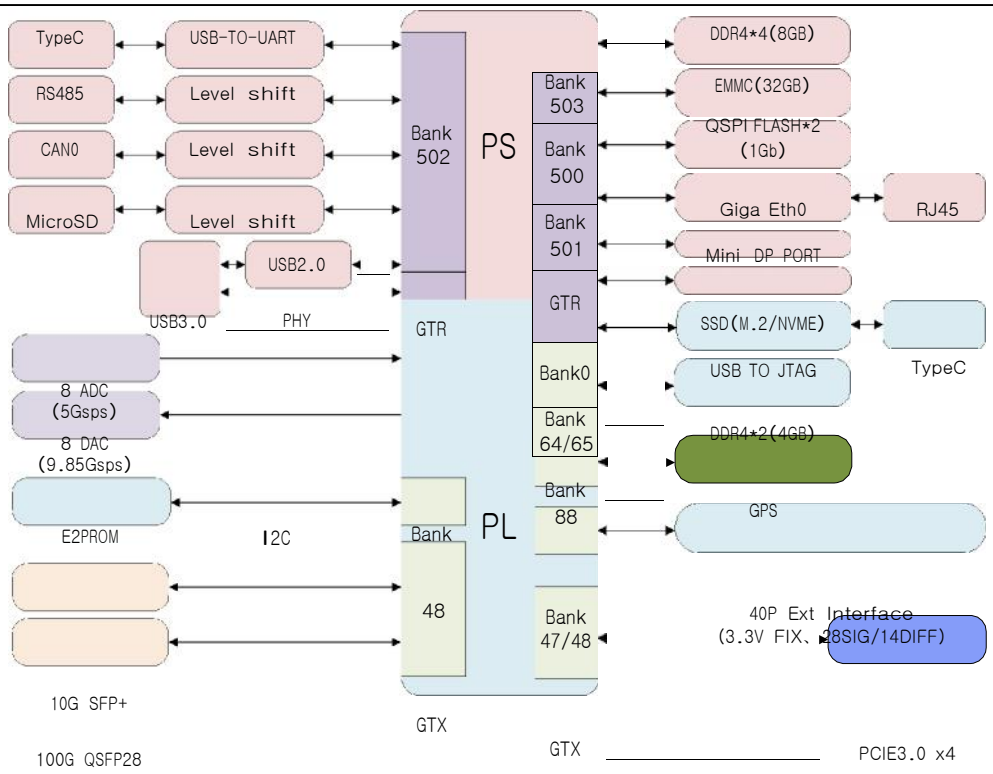
of the development board is 198x 138mm . There is a fixing hole at each of the four corners of the board for installing support columns or fixing the board. The hole diameter is 3.5mm . In addition, the development board is equipped with a dedicated heat sink and fan to ensure stable and reliable operation of the board. The following figures are the functional module position markings of the development board and the core board. Users can check the location of the peripherals according to the markings.





1.2 Development Board Resources and Block Diagram

The following table and block diagram have listed the onboard resources of the development board. The table below shows all the functions included in the development board.



The interfaces and functions included in the RF SOC development platform are as follows:

CRZU47DRC core board

By ZU47DR + 8 GB DDR4 (PS) + 4 GB DDR4 (PL) + 1 Gb QSPI Flash . In addition, the core module provides dual crystal clock sources. A single-ended 33.3333MHz active crystal is provided to the PS system, and a 200Mhz differential clock active crystal is provided to the PL system . The clock generated by the dedicated clock chip meets the clock requirements of each part of the ADC/DAC/GT/PL end.

USB to JTAG/Serial

The FT2232HL chip is used to realize the two functions of USB to JTAG and UART. The USB interface adopts TypeC . Users can communicate with the serial port by connecting it to the PC with a TypeC cable.

SD card holder

A TF card holder is placed, which can be used for SD card startup, and is also convenient for users to debug or store files.

RS485 interface

Use SP3485EN chip to realize RS485 communication.

CAN interface

Use SN65HVD230D chip to realize CAN communication.

E2PROM

A 64Kbit EEPROM chip, model AT24C64D-SSHM-T.

Mini DP port

One Mini DP output interface.

USB3.0 interface

One USB 3.0 port uses Type A and supports both HOST and SLAVE modes .

Gigabit Ethernet

One 10M100M/1000M Ethernet RJ45 interface, used for Ethernet data exchange with computers or other network devices.

QSFP28 and SFP+ interfaces

One QSFP28 interface and one SFP+. The SFP+ signal shares a pair with the PCIE model. You need to use a switch to select whether the GT signal goes through PCIE or SFP+. One QSFP28 fiber optic interface supports 40G/100G communication rates.

SSD interface/ M.2 interface

One SSD (x2 mode), interface type is M.2, using NVME protocol, used to connect M.2 SSD solid state drive.

PCIE interface

PCIE3.0 (x4 mode).

High-speed ADC/DAC

8-channel high-speed ADC and 8-channel high-speed DAC, the ADC sampling rate is up to 5GSPS, and the DAC sampling rate is up to 9.85GSPS.

LEDs

4 LEDs, namely power indicator, GPS status light, system status light, and RF status light.

GPS module

Data can be exchanged through the serial port, and GPS provides a PPS signal.

40P expansion interface

The development board has a simple 40P 2.54mm pitch header for extended signal connection.

USB to JTAG Downloader

installing the Vivado software, use a USB cable to connect the USB port corresponding to JTAG to achieve debugging and downloading.

Chapter 2: CRZU47DRC Core Board

2.1 Introduction to the core board

Cruetech ZU47DR core board uses the XCZU47DR-2FFVE1156I chip of XILINX as the main controller. The core board is connected to the motherboard with three 0.635mm pitch 240P gold -plated high-speed connectors. There are four 3.5mm fixing holes on the four feet of the core board . These holes can be fastened to the base plate with screws to ensure stable operation in a strong vibration environment.

The core board integrates dual groups of large-capacity DDR4, dual groups of large-capacity QSPI Flash, and large-capacity EMMC storage space.

In addition, the core board integrates a dedicated clock chip to provide a dedicated clock for ADC/DAC/GTH.

In addition, the chip integrates multi-channel ADC/DAC, with high integration, small size and excellent performance. At the same time, in order to match the heat dissipation of the core board, the core board is equipped with a heat sink, which further improves the performance of the core board.

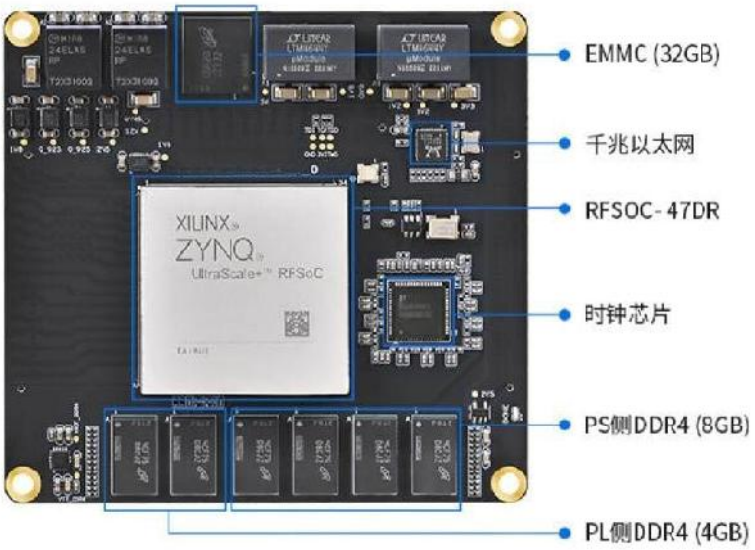
2.2Core board specifications

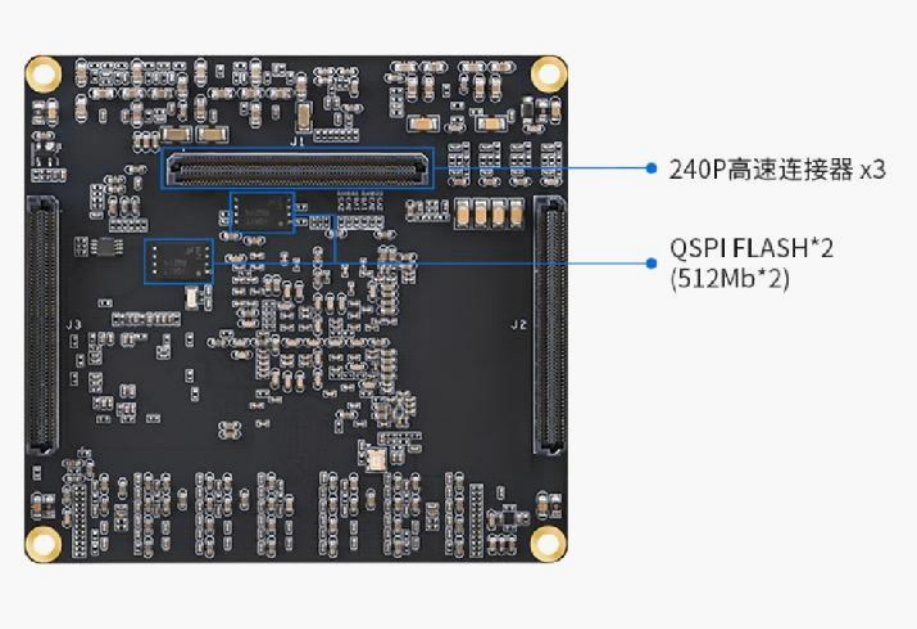
	CRZU47DRC industrial core board
Main controller name	XCZU47DR-2FFVE1156I
processor	ARM: 4 x Cortex - A53 1.333GHz RPU : 2 x Cortex - R5 533M hz
logic cells(K)	930
CLB L UTs （K）	425
Block RAM (Mb)	38
Ultra RAM (Mb)	22.5
D SP S lices	4272
D DR4/DDR4L	PS side 8 GB 2400M hz* 64 bit / PL side 4 GB 2400M hz* 32 bit
Q SPI FLASH	2 channels (Q SPO + QSPI1) / single chip 512M b , total 1Gb
E MMC	32 GB for boot files and user files
Startup method	JTAG/ Q SPI/SD/EMMC , onboard dip switch selection
Gigabit Ethernet	1 way (PS side)
ADC Channels	8 channels/sampling rate 5Gsps
DAC Channels	8 channels/sampling rate 9.85Gsps
I O quantity	MIO : 3 8 (fixed 1.8V level) HD : 44 (1.8 /2.5 / 3.3V adjustable, default3.3V)

PS side G TR	4 pairs of TX /RX
PL side GTH interface	8 pairs of TX /RX
Working voltage/m	8 - 12V / 5A (recommended
Operating temperature	- 40 ° C -- + 85 ° C
Core board size and process	90x 75 mm, matte black, immersion gold process , 0.635mm 240 P connector x 3
Core board and baseboa	5mm

2.3 Appearance of the core board

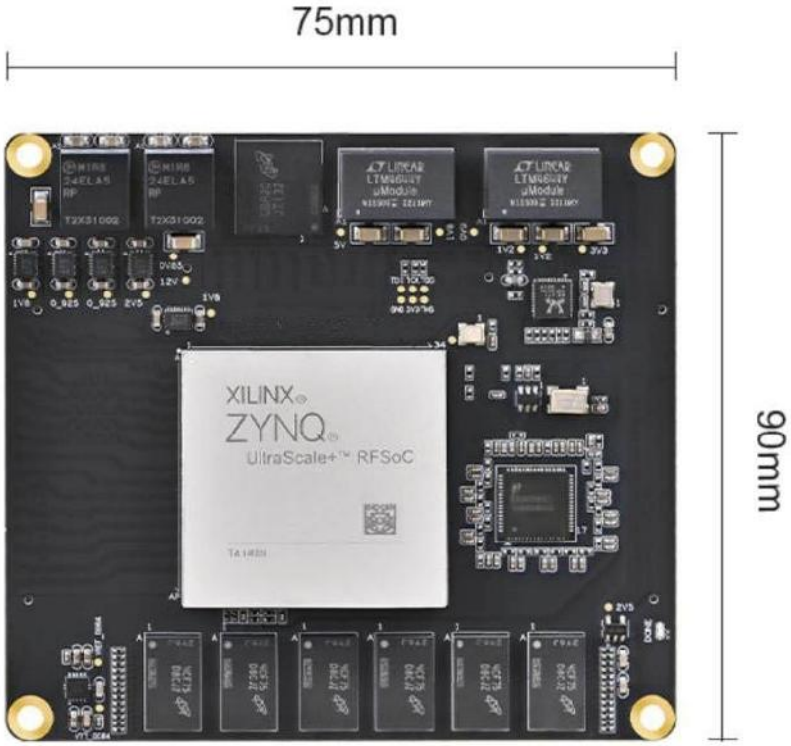
The following figure marks the location of the main electronic components of each core board on the core board for easy viewing and identification by users.





2.4 Productsize

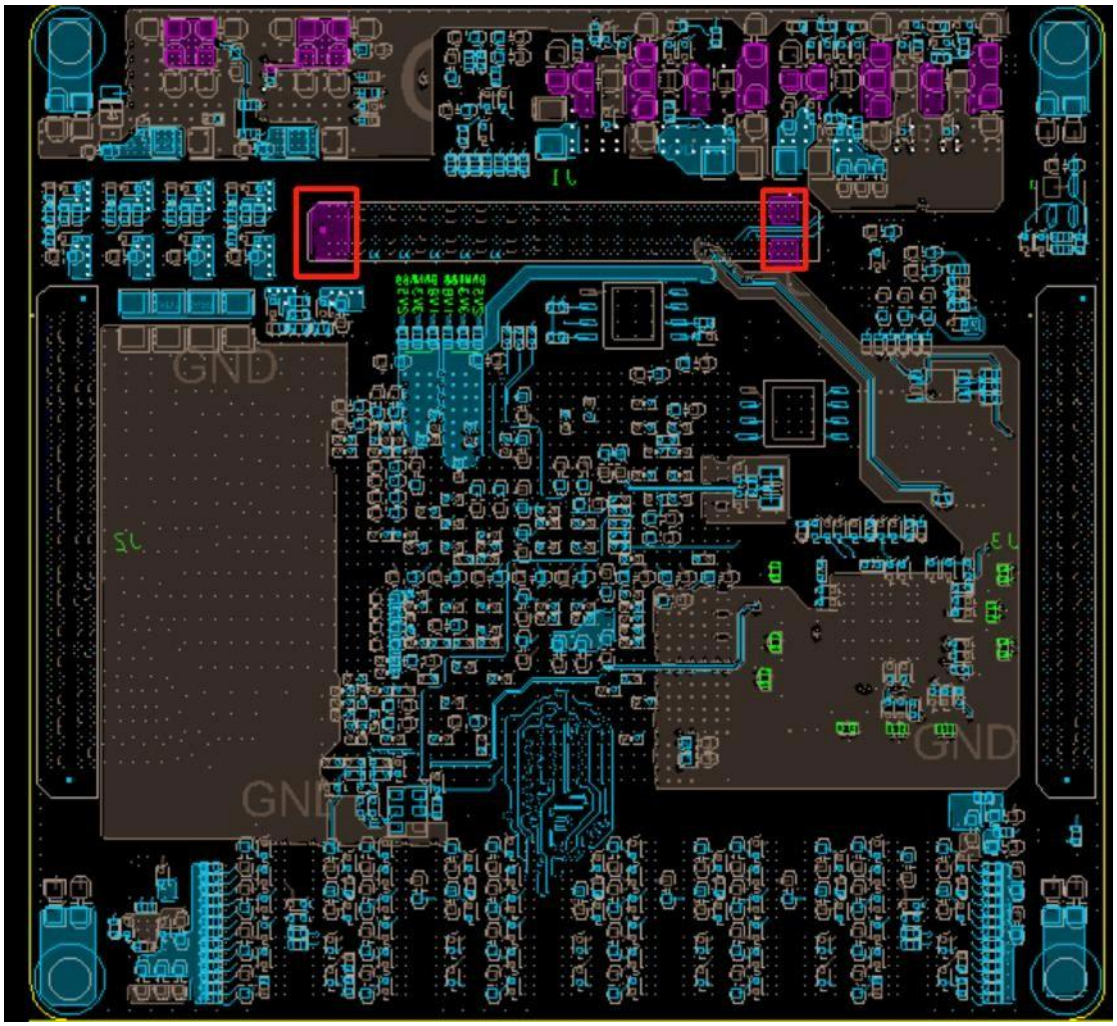
The size of the core board is 90x 75 mm. The core board is connected to the base board through three 0.635 mm /240 P gold-plated high-speed connectors on the back , with a total height of 5 mm . The following figure shows the size of the core board.



2. 5 Core board power supply

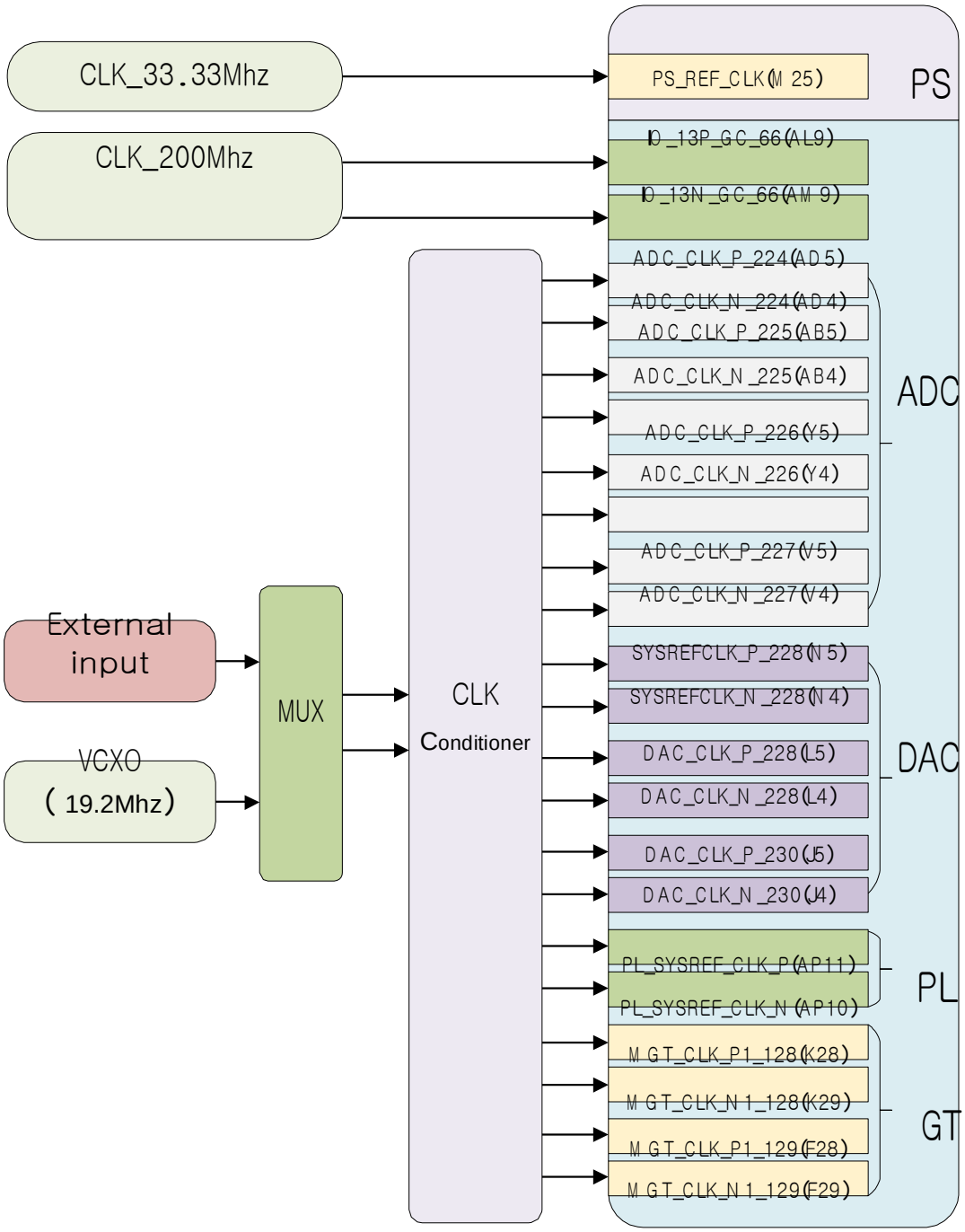
The supply voltage range of the core board is 8 - 12V , and the recommended supply voltage is 8V . There are power input pins at both corners of the core board, and the power pins have been connected inside the module. This design is to facilitate the power access of the baseboard. When designing, you only need to connect the power pin on one corner, and the core board can work. The power connection needs to be connected with copper foil and enough vias should be punched to ensure the power flow capacity . All GND signals on the core board need to be connected to the baseboard, and each GND is connected to the baseboard through two vias. The core board power supply limit current is 5A , so the external power supply needs to consider the limit current situation to ensure the stable operation of the core board.

The output voltage of the power supply for the module needs to be stable. Add a D CDC power conversion at the module power input, from high voltage to 8-12V (8 V is recommended) . The D CDC current output capacity can be selected to be 6A or above. Two 2 20 u F/25V capacitors need to be placed at the module power input to ensure the power quality.



2. 6 Core board clock

The core board provides a 33.333333Mhz clock input for the PS side , and the input pin location is PS_REF_CLK ; it provides a 200Mhz differential clock input for the PL side , the clock input pin on the PL side is IO_13P_GC_66 /IO_13N_GC_66 , and the pin location is AL9 / AM9 ; in addition, for other parts of ZU47DR, we use dedicated clock chips to generate the clock requirements of each part of the ADC/DAC/GT/PL end. The following figure lists the pin connections of each part of the clock.



2. 7 Core board global reset

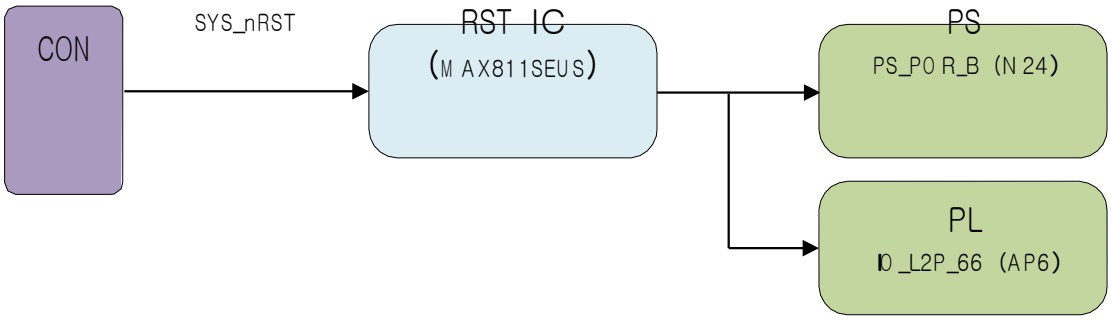
The core board provides an nGST reset circuit, which is valid at low level. This pin is also brought out to the connector, and the signal name is SYS_nRST , which is convenient for adding an external reset button or designing a watchdog reset circuit. At the same time, in order to ensure system stability, we added a reset chip MAX811SEUS to the core board . This signal can be used to reset other peripherals on the board, and the signal level is 3.3V . The reset pin is a common reset for PS/PL , connected to the PS_POR_B (N24) pin on the PS side

and the IO_L2P_66 (AP6) pin of BAN 66 on the PL side .

If a reset circuit needs to be designed on the baseboard, the following situations need to be considered.

1) The reset circuit is used internally on the baseboard. You only need to add a reset button and a 10uF capacitor in parallel to the ground.

2) 10 u F capacitor and a TVS anti -static device need to be connected in parallel to the ground .



2. 8 Core board startup mode

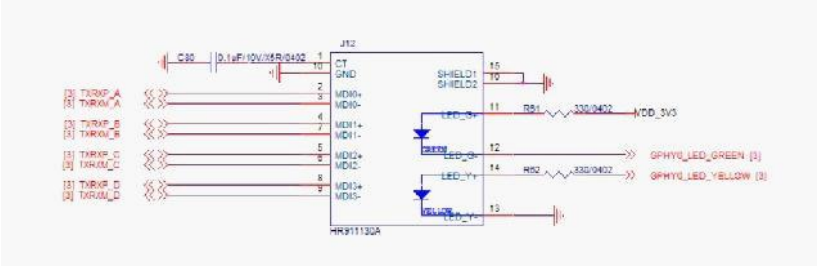
The core board supports four boot modes, namely J TAG , Q SPI Flash, E MMC , and SD card . The first three boot modes are onboard, and the SD card mode can be achieved by connecting it on the baseboard. The four boot modes can be selected by adding a dip switch on the baseboard.

2. 9 Network port chip

RTL8211FI - CG is placed on the core board . The Ethernet chip and the ZYNQ chip are interconnected through the R GMII interface. The corresponding pins are shown in the table below. Ethernet external connection only requires an R J45 with a transformer . The chip address PHY_AD[2:0]=001 . The connection schematic diagram can be referred to the figure below (the product circuit needs to add an E SD protection circuit). In addition, in actual product applications, C 80 needs to use high-voltage capacitors, such as 0.1 u F / 2 KV .

RMGII signal	Pin Name	Pin Location
GTX_CLK	MIO26_501	K19
TxD	MIO27_501	H19
TXD	MIO28_501	J19
TXD	MIO29_501	H21
XD3	MIO30_501	H20
TX_EN	MIO31_501	G20
RX_CLK	MIO32_501	F19
XDJ	MIO33_501	G21
RXD1	MIO34_501	D18
RXD2	MIO35_501	F20

XD3	MIO36_501	C18
RX_DV	MIO37_501	E19
MDC	MIO76_502	E26
MDIO	MIO77_502	D26



2.10 EMMC pin definition

onboard EMMC capacity is 32 GB , the operating temperature is - 40 ℃ -- + 85 ℃, and the pin definitions are as shown in the following table.

EMMC pin	Pin Name	Pin Location
EMMC_D0	MIO13	G18
EMMC_D1	MIO14	A15
EMMC_D2	MIO15	D16
EMMC_D3	MIO16	G17
EMMC_D4	MIO17	E16
EMMC_D5	MIO18	F18
EMMC_D6	MIO19	C16
EMMC_D7	MIO20	B16
EMMC_CLK	MIO22	E17
EMMC_CMD	MIO21	F17
EMMC_nRST	MIO23	D17

2.11 QSPI FLASH

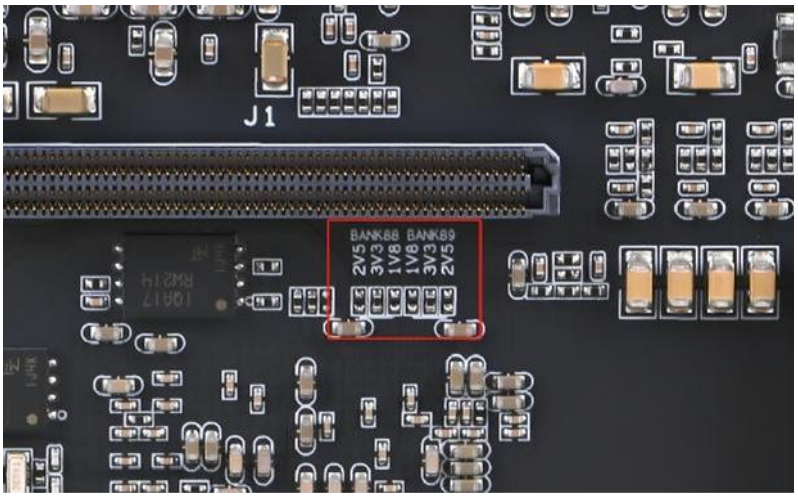
The core board is designed with two Q SPI FLASH , with a single chip capacity of 512 Mb , and two chips totaling 1Gb. Users can define it as Q SPI X8 to speed up the startup and reduce the startup time. Q SPI FLASH can be used to store startup files and user files.

QSPI FLASH pin	Pin Name	Pin Location
DATA0	MIO4	G15
DATA1	MIO1	J18
DATA2	MIO2	J16
DATA3	MIO3	K16
Q SPI_CS	MIO5	H18
Q SPI_CLK	MIO0	J17

QSPI FLASH pin	Pin Name	Pin Location
DATA0	MIO8	E15
DATA1	MIO9	F15
DATA2	MIO10	C15
DATA3	MIO11	G16
QSPI_CS	MIO7	K17
QSPI_CLK	MIO12	B15

2. 12 BANK interface level selection

BANK 88/89 on the board is HD BANK, and the BANK level can achieve three level conversions of 1.8V/2.5V/3.3V. Just change the position of the resistor. The default level is 3.3V .



2.13 PS side DDR

The PS side is equipped with four industrial-grade D DR4 chips, each with a capacity of 2 GB , and a total capacity of 8 GB. The model is MT40A1G16TB-062EIT:F . The D DR4 pin allocation can be directly called by the system allocation. You can also refer to the routines provided by our company.

2.14 PL side DDR

The PL side is equipped with two industrial-grade DDR4 chips, each with a capacity of 2 GB and model MT40A1G16TB-062EIT:F . The D DR4 pin assignment is shown in the table below.

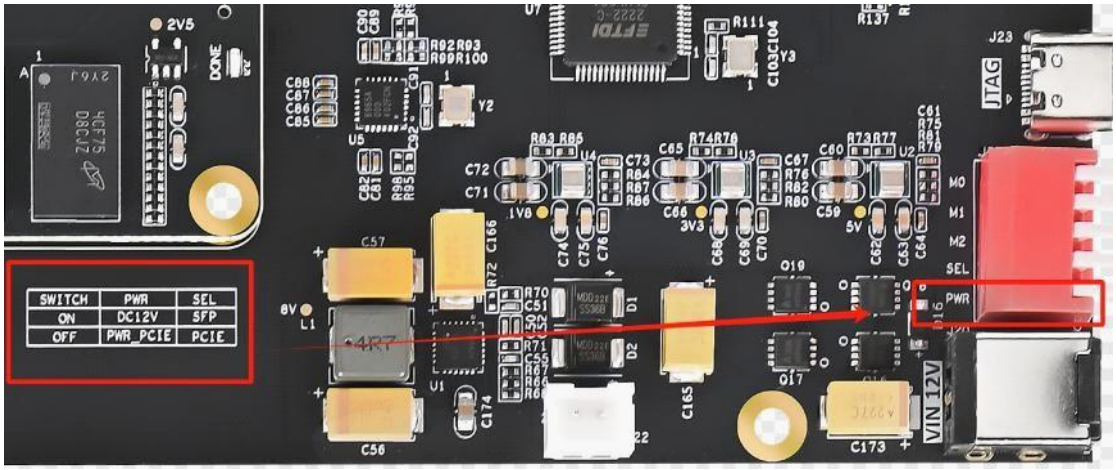
D DR4 pin	Pin Name	Pin Location
DDR4_D0	I OL 3 P-6 5	AP16
DDR 4 _D 1	I OL 6 N-6 5	AP17
DDR 4 _D 2	I OL 2N -6 5	AN15
DDR 4 _D 3	I O-L5N-6 5	AN17
DDR 4 _D 4	I OL 3 N-6 5	AP15
DDR 4 _D 5	I OL 5 P-6 5	AM17
DDR 4 _D 6	I OL 2 P-6 5	AM15
DDR 4 _D 7	I OL 6P -6 5	AN18
DDR4_D M0	I O-L1P-6 5	AM14
DDR 4 _D QS_P0	I O-L4P-6 5	AL17
DDR 4 _D QS_N0	I O-L4N-6 5	AM16
DDR 4 _D 8	I O-L11P-6 5	AJ16
DDR 4 _D 9	I OL 12 P-6 5	AJ17
DDR 4 _D 10	I OL 8 P-6 5	AK15
DDR 4 _D 11	I OL 12 N-6 5	AK16
DDR 4 _D 12	I O-L11N-6 5	AJ15
DDR 4 _D 13	I O-L9P-6 5	AK18
DDR 4 _D 14	I OL 8 N-6 5	AK14
DDR 4 _D 15	I O-L9N-6 5	AL18
DDR4_D M1	I O-L7P-6 5	AH13
DDR 4 _D QS_P1	I O-L10P-6 5	AH18
DDR 4 _D QS_N1	I O-L10N-6 5	AJ18
DDR4_D16	I O-L1 5 P-6 5	AF14
DDR 4 _D 17	I O-L1 7 N-6 5	AF16
DDR 4 _D 18	I O-L1 5N -6 5	AF13
DDR 4 _D 19	I O-L1 4N -6 5	AH17
DDR 4 _D 20	I O-L1 7P -6 5	AE16
DDR 4 _D 21	I O-L1 4P -6 5	AG17

DDR 4 _D 22	I O-L1 8 N-6 5	AF17
DDR 4 _D 23	I O-L1 8 P-6 5	AF18
DDR4_D M2	I O-L13P-6 5	AG15
DDR 4 _D QS_P2	I O-L16P-6 5	AG14
DDR 4 _D QS_N2	I O-L16N-6 5	AH14
DDR 4 _D 24	I O-L23N-6 5	AD16
DDR 4 _D 25	I O-L24P-6 5	AD18
DDR 4 _D 26	I O-L2 1P -6 5	AD15
DDR 4 _D 27	I O-L20P-6 5	AE14
DDR 4 _D 28	I O-L23P-6 5	AC17
DDR 4 _D 29	I O-L2 4 N-6 5	AE18
DDR 4 _D 30	I O-L21 N -6 5	AE15
DDR 4 _D 31	I O-L20N-6 5	AE13
DDR4_D M3	I O-L19P-6 5	AC13
DDR 4 _D QS_P3	I O-L22P-6 5	AC16
DDR 4 _D QS_N3	I O-L22N-6 5	AC15
DDR4_ A 0	I OL 20N -6 6	AH9
DDR4_ A 1	I O-L1 6 P-6 6	AL12
DDR4_ A 2	I OL 5P -6 6	AP3
DDR4_ A 3	I O-L1 8 P-6 6	AJ11
DDR4_ A 4	I O-L1 7 P-6 6	AK10
DDR4_ A 5	I OL 16 N-6 6	AL11
DDR4_ A 6	I O-L1 0 N-6 6	AM7
DDR4_ A 7	I O-L1 5 N-6 6	AL13
DDR4_ A 8	I OL 5 N-6 6	AP2
DDR4_ A 9	I O-L7 P -6 6	AP13
DDR4_ A 10	I O-L1 7 N-6 6	AK9
DDR4_ A 11	I O-L1 0 P-6 6	AM8
DDR4_ A 12	I OL 2 2N-6 6	AJ9
DDR4_ A 13	I OL 15 P-6 6	AK13
DDR4_ A 14	I O-L21N-6 6	AG9
DDR4_ A 15	I OL 18 N-6 6	AK11
DDR4_ A 16	I O-L21P-6 6	AG10
DDR4_ A 17	I O-L1P-6 6	AP8
DDR4_BA0	I O-L9N-6 6	AN7
DDR4_BA1	I OL 7N -6 6	AP12
DDR4_BG0	I O-20P-6 6	AH10
DDR4_ n CS	I OL 8N -6 6	AN12
DDR4_ n ACT	I O-L19 P -6 6	AG12
DDR4_ODT	I OL 22 P-6 6	AJ10
DDR4_ n RESET	I OL 6 P-6 6	AN2
DDR4_CLK_P	I O-L14P-6 6	AM12
DDR4_CLK_N	I O-L14N-6 6	AM11
DDR4_CKE	I OL 19N -6 6	AG11
D DR4_PARITY	I OL 9P -6 6	AN8
D DR4_ n ALERT	I OL 23 P-6 6	AF12

Chapter 3: CRZU47DRB Baseboard Introduction

3. 1 Power supply

There are two ways to power the development board: PCIE or 12V /3A adapter. You can select the power supply mode through the red dip switch on the side. After the power is connected, it is converted into 8V , 5V , 3.3V and other multiple voltages through DCDC for use by the components on the board. For the detailed circuit of the power supply, please refer to the schematic diagram corresponding to the development board.



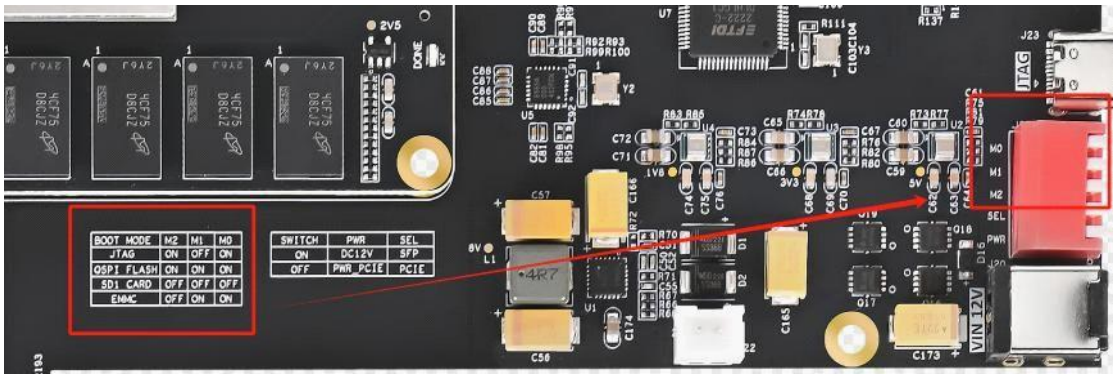
3. 2 Reset Circuit

A reset button is placed on the back of the development board, which is convenient for making a shell for the board later.

The reset pin is a common reset for PS/PL and is connected to the PS_POR_B (N24) pin on the PS side and the IO_L2P_66 (A P6) pin of B ANK 66 on the PL side .

3. 3 Startup Mode

Considering the shell production of the board, we designed a dip switch on the edge of the development board for selecting the startup mode. For detailed startup modes, please refer to the table on the left for selection.

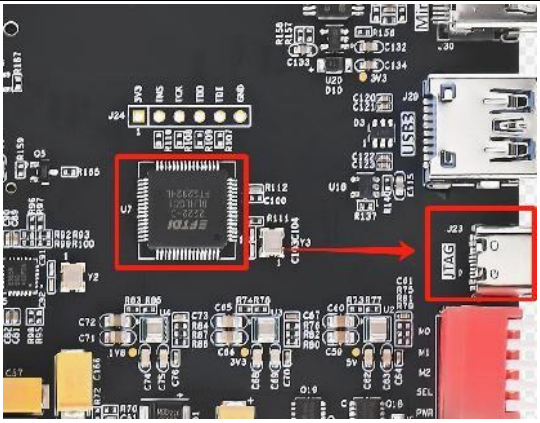


3. 4 USB to JTAG/Serial Port

The development board uses the FT2232HL chip to realize the two functions of USB to JTAG and UART . The USB interface uses TypeC . Users can communicate via serial port by connecting to the PC with a TypeC cable.

The TX/RX signals of UART are connected to BANK501 of RF SOC , and the interface level is 1.8V , so the serial port interface uses level conversion to 3.3V to connect to the serial port chip.
The following is the signal correspondence table and schematic diagram.
The TX/RX direction is defined at the MPSOC end.

UART0 Pins	RF SOC pin name	Pin Location
UART0_TX	M IO_43	A19
UART0_RX	M IO_42	E20

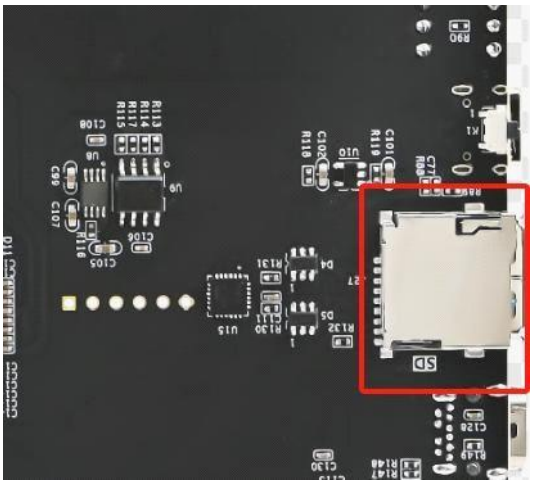


3. 5 SD card holder

TF card holder is placed on the development board , which can be used for SD card startup and is also convenient for users to debug or store files. The circuit interface level is 1.8V, the SD card signal is connected to the B ANK501 of the RF SOC , and the TF card level is 3.3V . The SD card signal is converted from 1.8V to 3.3V through a dedicated level conversion chip .

The following is the signal correspondence. For detailed circuit, please refer to the development board schematic diagram.

SD card pin	RF SOC pin name	Pin Location
S D-CLK	MIO51	B21
S D-CMD	MIO50	A22
S D-DATA0	MIO46	A20
S D-DATA1	MIO47	D21
S D-DATA2	M IO48	C21
S D-DATA3	MIO49	E21

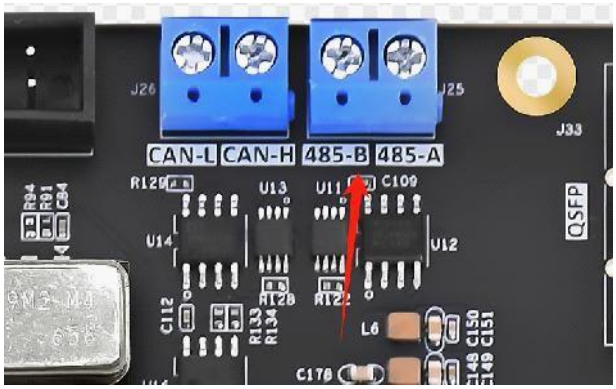


3.6 RS485 interface

The development board uses the SP3485EN chip to implement RS485 communication. The TX/RX signals of RS485 are connected to the B ANK501 of the RF SOC . The interface level is 1.8V , so the interface is converted to 3.3V and connected to the RS485 chip.

The following is the signal correspondence table and schematic diagram. The TX/RX direction is defined at the RF SOC end.

RS485 Pinout	RF SOC pin name	Pin Location
RS485_TX	MIO40	A18
RS485_RX	MIO41	C19

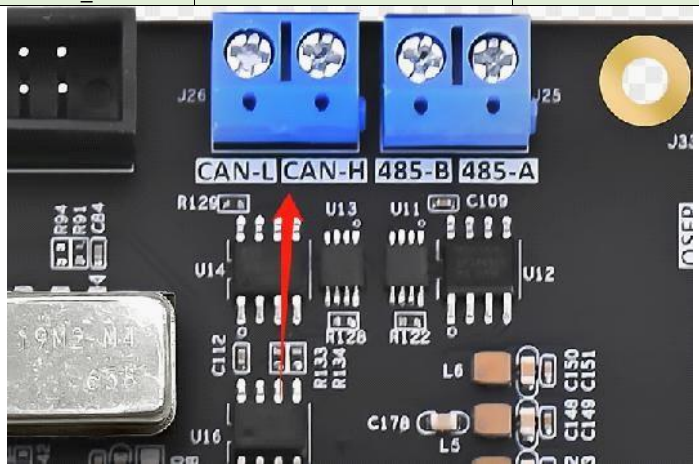


3.7 CAN interface

The development board uses the SN65HVD230D chip to implement CAN communication. The CAN's TX/RX signals are connected to the RF SOC 's B ANK501. The interface level is 1.8V , so the signal interface is converted to 3.3V and connected to the CAN chip .

The following is a signal correspondence table. The TX/RX direction is defined by the RF SOC end. For detailed circuits, refer to the development board schematic diagram.

C AN pin	RF SOC pin name	Pin Location
CAN_TX	MIO39	D19
CAN_RX	MIO38	B18

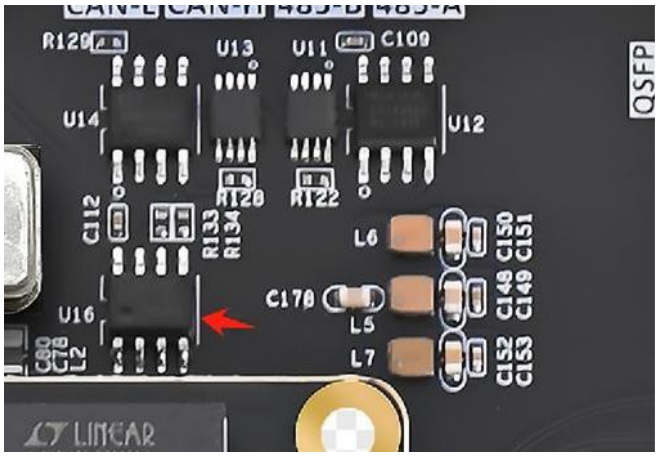


3. 8 E2PROM

64K bit EEPROM chip, model A T24C64D-SSHM-T , is placed on the development board and connected to the FPGA 's B ANK 88 through the I IC bus. The EEPROM read address is 0x A1 and the write address is 0x A0 .

The following is the pin assignment of EEPROM . For detailed circuit, please refer to the development board schematic diagram.

E EPROM Pinout	RF SOC pin name	Pin Location
IIC-CLK	I O- 1 P- 88	K15
IIC-DATA	I O- 1 N- 88	K14

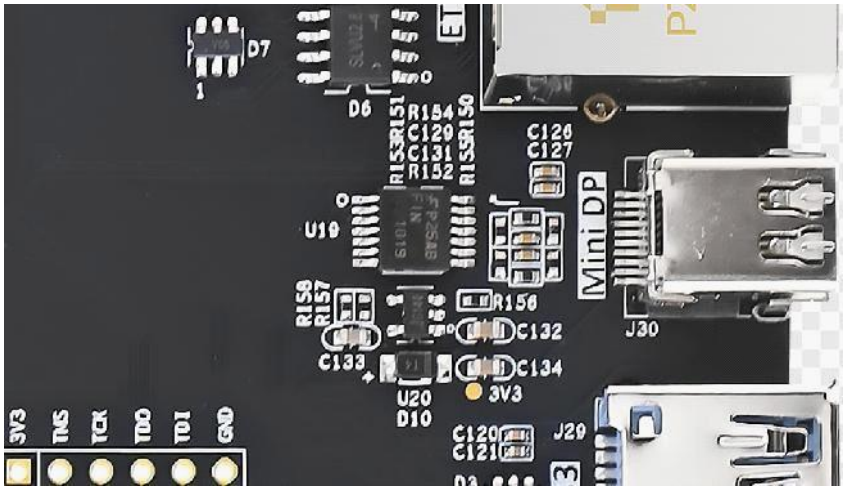


3. 9 Mini DP interface

Mini DP output interface is placed on the development board , and the interface signal is connected to the FPGA 's B ANK 88/ BANK505 . For details , please refer to the schematic diagram.

The following is the pin assignment of Mini DP . For detailed circuit, please refer to the development board schematic diagram.

Mini DP Pinout	MPSOC Pin Name	Pin Location
DP_LINE_PO	MGT_505_TX_P3	R30
DP_LINE_NO	MGT_505_TX_N3	R31
DP_HPD	I O_L 3P _ 88	J14
DP_AUX_OUT	I O_L 3 N_ 88	J13
DP_OE	I O_L 7 P_ 88	E14
DP_AUX_IN	I O_L7 N _ 88	D14
D P_CLK_P_27M	MGT_505_CLK_P 3	P28
D P_CLK_N_27M	MGT_505_CLK_N 3	P29

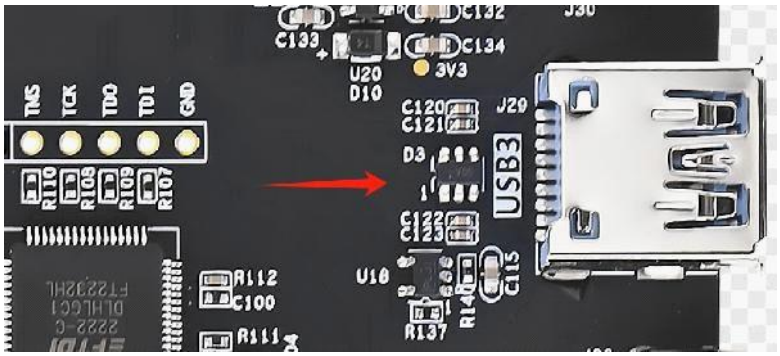


3.1 0 USB3.0 interface

USB3.0 port is designed on the development board . It uses Type A. The interface can be configured as a master port or a slave port. Users can configure it as needed. The interface signal is connected to FPGA 's BANK501 / BANK505 . For details, please refer to the schematic diagram. USB2.0 is implemented by connecting the P HY chip USB3320C-EZK to M IO . USB3.0 is extended by the H UB chip GL3523-0TY30 .

The following is the pin assignment of USB2.0/USB3.0 . For detailed circuit, please refer to the development board schematic diagram.

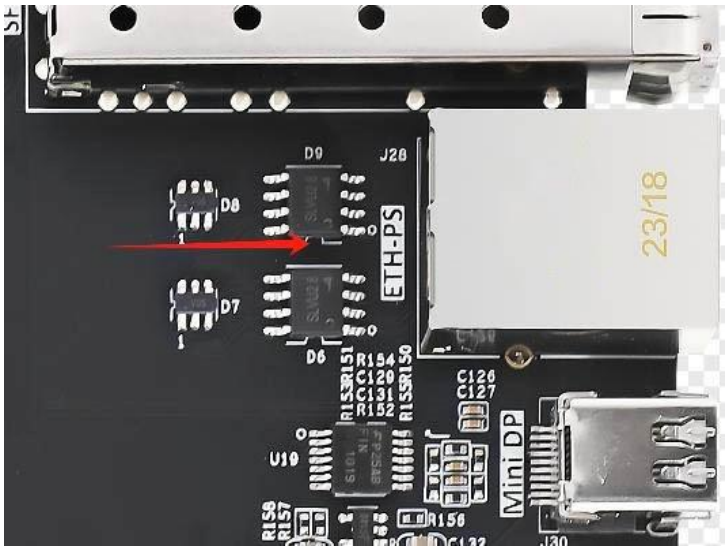
USB pins	RF SOC pin name	Pin Location
U SBPHY_DATA0	MIO56	G23
U SBPHY_DATA1	MIO57	F23
U SBPHY_DATA2	MIO54	H23
U SBPHY_DATA3	MIO59	D23
U SBPHY_DATA4	MIO60	A23
U SBPHY_DATA5	MIO61	E22
U SBPHY_DATA6	MIO62	B23
U SBPHY_DATA7	MIO63	C23
U SBPHY_STP	MIO58	B22
USBPHY_NXT	MIO55	D22
USBPHY_DIR	MIO53	F22
USBPHY_CLKOUT	MIO52	G22
USBPHY_RESET	MIO44	C20
GT 2 _USB3_SSTXP	MGT_505_TX_P 2	U31
GT 2 _USB3_SSTXN	MGT_505_TX_N 2	U32
GT 2 _USB3_SSRXP	MGT_505_RX_P 2	V33
GT 2 _USB3_SSRXN	MGT_505_RX_N 2	V34
USB3_CLK_P_26M	MGT_505_CLK_P 2	T28
USB3_CLK_N_26M	MGT_505_CLK_N 2	T29



3.1 1 Gigabit Ethernet

A PS-side Gigabit Ethernet is designed on the development board, and the PS - side network port has been integrated into the core board. The Ethernet chip and RF SOC are interconnected through the RGMII interface. The corresponding pins are shown in the table below. The PS- side network port address is PHY_AD[2:0]=001 . For detailed circuits, please refer to the development board schematic diagram.

PS network port		
R MGII signal	RF SOC pin name	Pin Location
G TX_CLK	M IO26_501	K19
TxD	M IO27_501	H19
T XD	M IO28_501	J19
T XD	M IO29_501	H21
XD3	M IO30_501	H20
T X_EN	M IO31_501	G20
R X_CLK	M IO32_501	F19
XDJ	M IO33_501	G21
R XD1	M IO34_501	D18
R XD2	M IO35_501	F20
XD3	M IO36_501	C18
R X_CTL	M IO37_501	E19
M DC	M IO76_502	E26
M DIO	M IO77_502	D26



3.1 2 QSFP28 vs. SFP + Interface

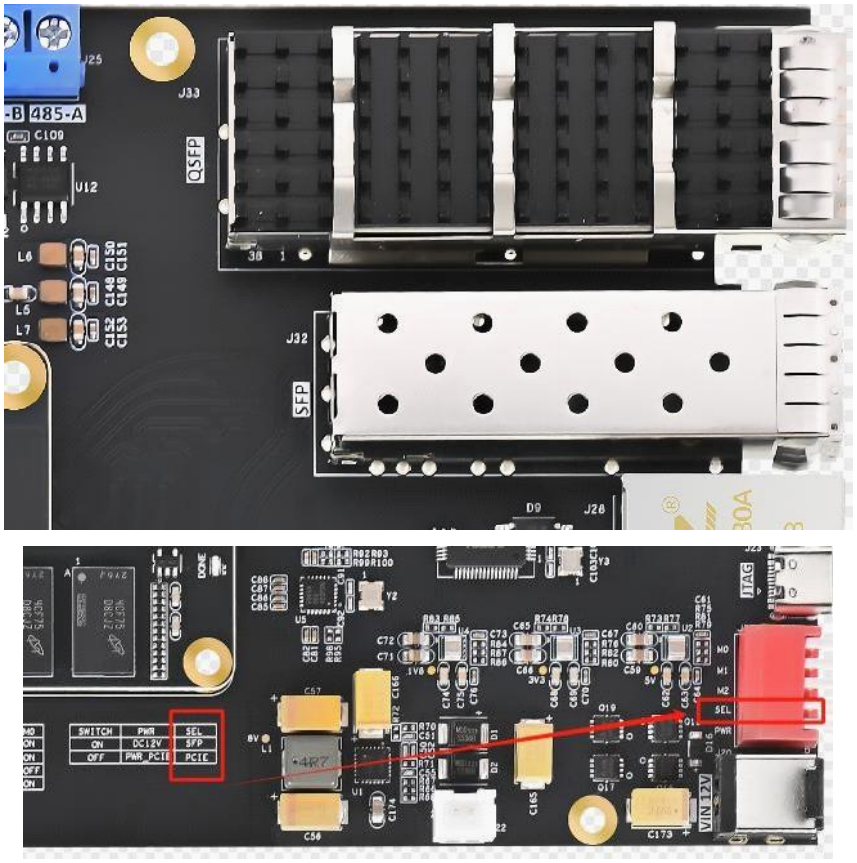
The development board is designed with one Q SFP 28 interface and

one SFP+. The communication capacity limit of QSFP28 is 100G. The SFP+ signal shares a pair with the PCIE model. It is necessary to use a switch to select whether the GT signal goes through PCIE or SFP+. The switch position and label are listed in the figure below. For more detailed circuits, please refer to the schematic diagram.

Below is the pinout for QSFP28 and SFP +.

QSFP28 Pinout	RF SOC pin name	Pin Location
Q SFP - TX-P 0	MGT-TX-P3-12 9	B28
Q SFP - TX-N 0	MGT-TX-N3-12 9	B29
Q SFP - TX-P 1	MGT-TX-P 2 -12 9	C30
Q SFP - TX-N 1	MGT-TX-N 2 -12 9	C31
Q SFP - TX-P 2	MGT-TX-P 1 -12 9	D28
Q SFP - TX-N 2	MGT-TX-N 1 -12 9	D29
Q SFP - TX-P 3	MGT-TX-P 0 -12 9	E30
Q SFP - TX-N 3	MGT-TX-N 0 -12 9	E31
Q SFP -R XP 0	MGT- R X-P3-12 9	A31
Q SFP -R XN 0	MGT- R X-N3-12 9	A32
Q SFP -R XP 1	MGT - R XP 2-12 9	B33
Q SFP -R XN 1	MGT - R XN2-129	B34
Q SFP -R XP 2	MGT- R XP 1 -12 9	D33
Q SFP -R XN 2	MGT- R XN 1 -12 9	D34
Q SFP -R XP 3	MGT- R XP 0 -12 9	F33
Q SFP -R XN 3	MGT- R XN 0 -12 9	F34
QSFP_LPMODE	I O _2 P _88	H15
I2C_SCL	I O _1 P _88	K15
I2C_SDA	I O _1N_88	K14

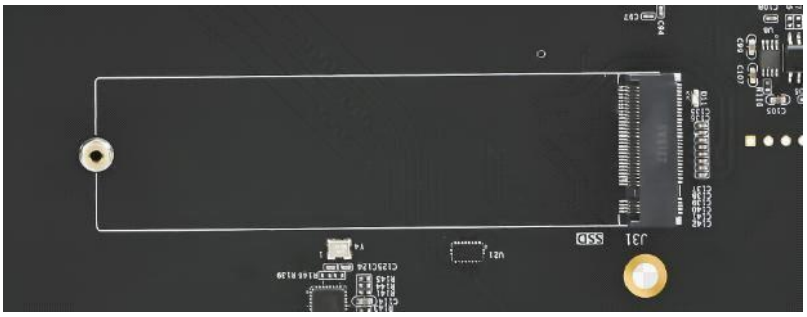
SFP + Pinout	RF SOC pin name	Pin Location
SFP - TX-P	MGT-TX- P 3-128	G30
SFP - TX-N	MGT-TX-N 3 -128	G31
SFP - RX- P	- RX-P 3-128	H33
SFP - RX-N	MGT-RX- N 3-128	H34
SFP-TX-DISABLE	I O _2N_88	H14



3.1 3 SSD interface

The development board has an SSD (x2 mode) designed on the PS side , with an M.2 interface and NVME protocol.
The pin positions of the SSD interface are shown in the following table. For detailed circuits, please refer to the development board schematic diagram.

SSD interface	MPSOC Pin Name	Pin Location
SSD_nRST	MIO6 5 _502	C24
REFCLK_P_100M	MGT_505_CLK_P0	Y29
REFCLK_N_100M	MGT_505_CLK_N0	Y30
GT0_SSD_TX_P0	MGT_505_TX_P0	AA31
GT0_SSD_TX_N 0	MGT_505_TX_N0	AA32
GT0_SSD_TX_P 1	MGT_505_TX_P 1	W31
GT0_SSD_TX_N 1	MGT_505_TX_N 1	W32
GT0_SSD_RX_P0	MGT_505_RX_P0	AB33
GT0_SSD_RX_N0	MGT_505_RX_N0	AB34
GT0_SSD_RX_P 1	MGT_505_RX_P 1	Y33
GT0_SSD_RX_N 1	MGT_505_RX_N 1	Y34



3.1 4 PCIE interface

The PL side of the development board is designed with PCIE3.0 (x 4 mode). The pin positions of the PCIE3.0 interface are shown in the following table. For detailed circuits, please refer to the schematic diagram of the development board.

PCIE3.0 interface	MPSOC Pin Name	Pin Location
P ERST_N	IO_L6 N _88	F12
R EF_CLK_P	MGT_CLK_P0_223	A D8
R EF_CLK_N	MGT_CLK_N0_223	A D7
P ER0_P	MGT_TX_P3_223	A J6
P ER0_N	MGT_TX_N3_223	A J5
P ER1_P	MGT_TX_P2_223	A L6
P ER1_N	MGT_TX_N2_223	A L5
P ER2_P	MGT_TX_P1_223	A M4
P ER2_N	MGT_TX_N1_223	A M3
P ER3_P	MGT_TX_P0_223	N6
P ER3_N	MGT_TX_N0_223	A N5
P ET0_P	MGT_RX_P3_223	A K4
P ET0_N	MGT_RX_N3_223	A K3
P ET1_P	MGT_RX_P2_223	A L2
P ET1_N	MGT_RX_N2_223	A L1
P ET2_P	MGT_RX_P1_223	A N2
P ET2_N	MGT_RX_N1_223	A N1
P ET3_P	MGT_RX_P0_223	A P4
P ET3_N	MGT_RX_N0_223	A P3

3. 15 High-speed ADC/DAC

The development board is designed with 8-channel high-speed ADC and 8-channel high-speed DAC. The sampling rate of ADC is up to 5GSPS, and the sampling rate of DAC is up to 9.85GSPS. For more detailed information, please refer to the development board schematic diagram.

3.1 6 LEDs

The development board has 4 LEDs designed on the edge, including the power indicator, GPS status indicator, system status indicator, and RF status indicator. The power and GPS indicators have fixed positions, while the system indicator and RF status indicator can be controlled by the user.

LED position number	RF SOC pin name	Pin Location
LED_SYS	IO_L9P_88	D13
LED _RF	IO_L9N_88	C13

3. 17 GPS Module

A GPS module is designed on the development board. The following figure shows the GPS module and antenna input port. The GPS module can exchange data through the serial port, and the GPS provides a PPS signal. The signal connection location is shown in the following figure.

LED position number	MPSOC Pin Name	Pin Location
GPS_UART_TXD	IO_L5P_88	F14
GPS_UART_RXD	IO_L5N_88	F13
GPS_nRESET	IO_L4P_88	H13
GPS_PPS	IO_L4N_88	G13

3. 18 40P expansion interface

The development board has a simple 40P 2.54mm pitch header for extended signal connection.

The signal level is 3.3V . The chip location of the signal is marked in the following table. For detailed connection relationship, refer to the schematic diagram .

J M1 signal sequence	RF SOC pin name	Pin Location	J M1 signal sequence	RF SOC pin name	Pin Location
5	IO_L1 2 P_ 89	K12	6	IO_L 9 P_ 89	H10
7	IO_L1 2 N_ 89	J12	8	IO_L 9 N_ 89	H9
9	IO_L1 1 P_ 89	J11	1 0	IO_L 8 P_ 89	G11
11	IO_L1 1 N_ 89	H11	1 2	IO_L 8 N_ 89	G10
13	IO_L1 0 P_ 89	K11	1 4	IO_L 6 P_ 89	E10
15	IO_L1 0 N_ 89	K10	16	IO_L 6 N_ 89	E9
17	IO_L 7 P_ 89	F10	18	IO_L 3 P_ 89	A10
19	IO_L 7 N_ 89	F9	20	IO_L 3 N_ 89	A9
twenty one	IO_L 2 P_ 89	C10	twenty two	IO_L 4 P_ 89	D9
twenty three	IO_L 2 N_ 89	B10	twenty four	IO_L 4 N_ 89	C9
25	IO_L 5 P_ 89	E11	26	IO_L1P_ 89	C11
27	IO_L 5 N_ 89	D11	28	IO_L1N_ 89	B11
29	IO_L1 2 P_ 88	B12	3 0	IO_L 8 P_ 88	E12
31	IO_L1 2 N_ 88	A12	3 2	IO_L 8 N_ 88	D12
37	-	-	3 8	-	-
39	-	-	4 0	-	-