Shenzhen Leadtek Electronics Co.,Ltd

PRODUCT SPECIFICATION

TFT-LCD MODULE

Module No：LTK050H31FPW12-V0

☑ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
		

Final Approval by Customer

Approved by	Comment

※The specification of “TBD” should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

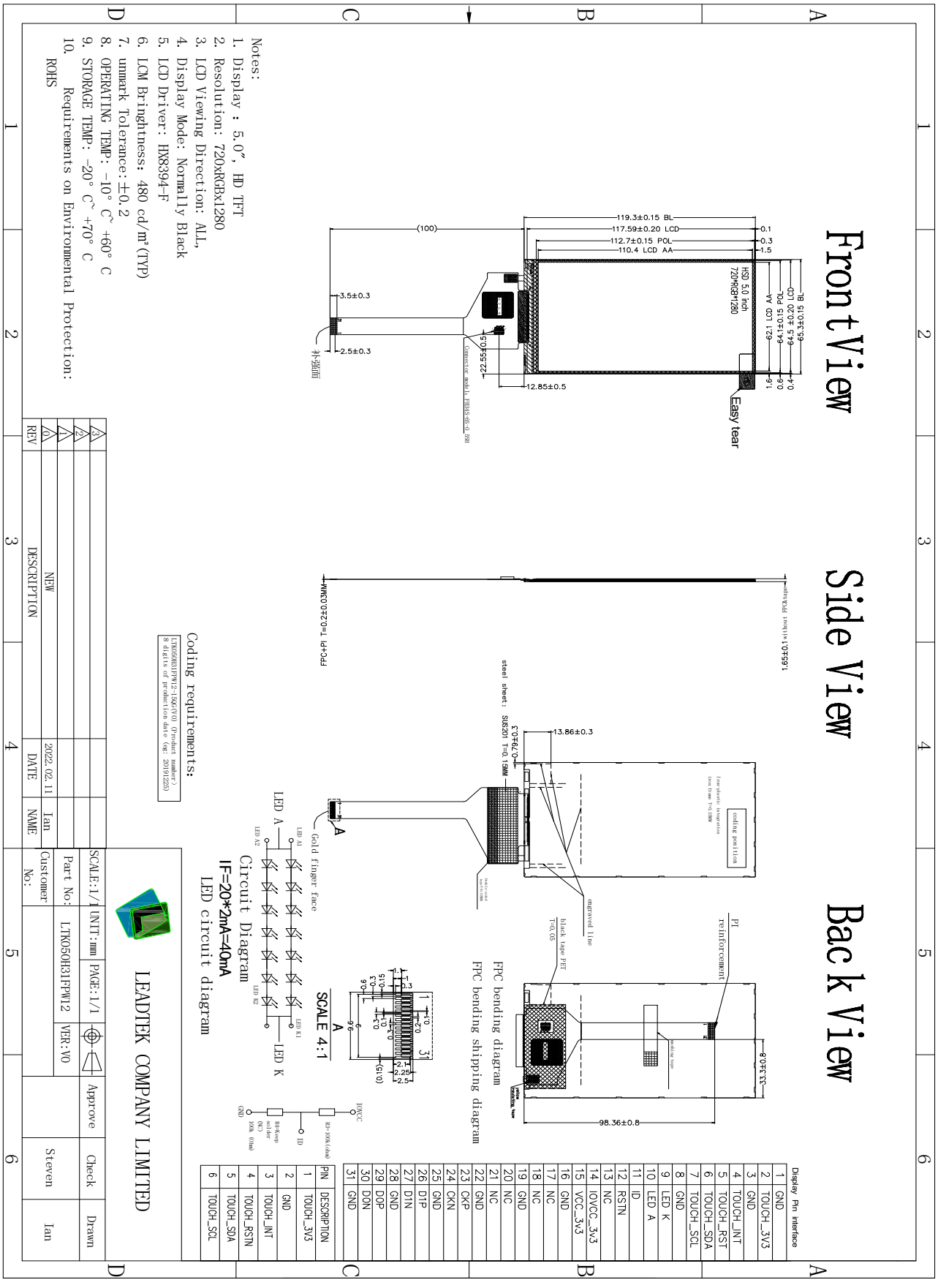
1.Document Revision History

Version	Contents	Date	Note
V0	Original	2022.02.11	

2. General Description

No	Item	Specification	Unit
1	Screen Size	5.0	inch
2	LCD Type	TFT	
3	LCD manufacturer	-	
4	Viewing Direction	ALL	Best Image
5	Display Mode	720*RGB（H）*1280 （V）	
6	Resolution	IPS(Normally Black)	Pixel
7	Active Area	62.1*110.4	mm
8	Outline Dimension	65.3*119.3*1.65	mm
9	Driver IC	HX8394F	
10	Interface	RGB	
11	Back Light	White Led*14	
12	With or Without Touch Panel	Without	

3. Outline Dimension



Display Pin interface		
1	GND	
2	TOUCH_3V3	
3	GND	
4	TOUCH_INT	
5	TOUCH_RST	
6	TOUCH_SDA	
7	TOUCH_SCL	
8	GND	
9	LED K	
10	LED A	
11	ID	
12	RSTN	
13	NC	
14	IOVCC_3v3	
15	VCC_3v3	
16	GND	
17	NC	
18	NC	
19	GND	
20	NC	
21	NC	
22	GND	
23	CKP	
24	CKN	
25	GND	
26	D1P	
27	D1N	
28	GND	
29	D0P	
30	D0N	
31	GND	

PIN	DESCRIPTION
1	TOUCH_3V3
2	GND
3	TOUCH_INT
4	TOUCH_RSTN
5	TOUCH_SDA
6	TOUCH_SCL

4. Interface Specification

NO.	Symbol	Function	Remark
1	GND	Power Ground	
2	TOUCH_3V3	Touch Panel Power supply	
3	GND	Power Ground	
4	TOUCH_INT	An interrupt signal to inform the host processor that touch data is ready for read	
5	TOUCH_RST	Touch Panel Reset Signal PIN	
6	TOUCH_SDA	Serial Data Input And Output	
7	TOUCH_SCL	Serial Clock Input	
8	GND	Power Ground	
9	LEDK	Power for LED backlight (Cathode)	
10	LEDA	Power for LED backlight (Anode)	
11	ID	ID PIN Pull High, If not use, please not connect	
12	RESET	Global reset signal(Follow IOVCC voltage)	
13	NC	No connect	
14	IOVCC_1V8	Digital power=1.8V	
15	VDD_3V3	Power supply=2.8-3.3V	
16	GND	Power Ground	
17	NC	No connect	
18	NC	No connect	
19	GND	Power Ground	
20	NC	No connect	

21	NC	No connect	
22	GND	Power Ground	
23	CLKP	MIPI-CLKPare differential small amplitude signals	
24	CLKN	MIPI-CLKNare differential small amplitude signals	
25	GND	Power Ground	
26	D1P	MIPI-D1Pare differential small amplitude signals	
27	D1N	MIPI-D1Nare differential small amplitude signals	
28	GND	Power Ground	
29	D0P	MIPI-D0Pare differential small amplitude signals	
30	D0N	D0N MIPI-D0Nare differential small amplitude signals	
31	GND	Power Ground	

4.1Touch Panel Interface PIN Define:

NO.	Symbol	Function	Remark
1	TOUCH_3V3	Touch Panel Power supply	
2	GND	Power Ground	
3	TOUCH_INT	An interrupt signal to inform the host processor that touch data is ready for read	
4	TOUCH_RST	Touch Panel Reset Signal PIN	
5	TOUCH_SDA	Serial Data Input And Output	
6	TOUCH_SCL	Serial Clock Input	

5.Operation Specifications

5.1 Absolute Maximum Ratings

Electrical Maximum Ratings (VSS=0V)

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VDD3V3	2.8	3.6	V	
	IOVCC	1.65	3.3	V	

Note: 1. VCI, GND must be maintained.
2. The modules may be destroyed if they are used beyond the absolute maximum ratings.
3.Ta=25+/-2.

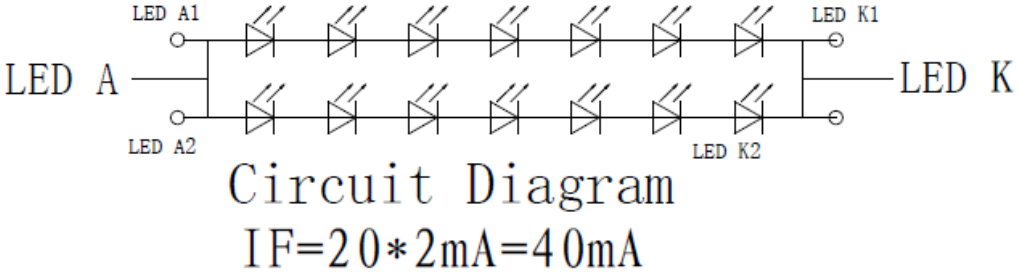
5.2 Electrical Specifications(Typical Operation Conditions, At Ta = 25 ℃)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Power Supply Voltage	IOVCC	1.7	1.8	1.9	V	-
	VDD3V3	2.8	3.3	3.6	V	-

5.3 LED Backlight Specification

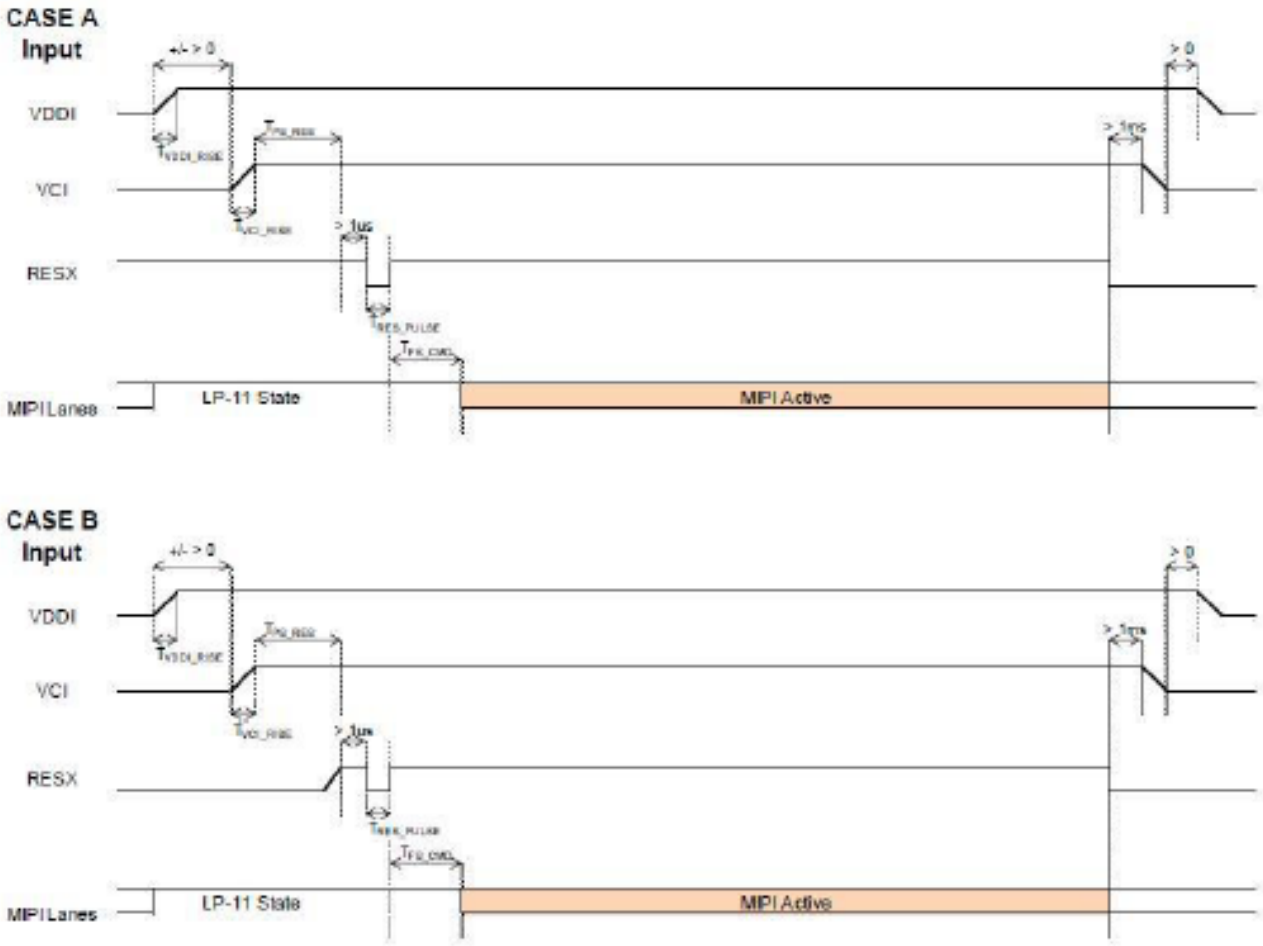
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition	Note
LED Current	IF	-	40	-	mA	-	-
Luminous	-	-	480		cd/m²	I=40mA	-
LED Voltage	VF	19.95	22.4	-	V	I=40mA	-
Life Time			20000	-	Hr.	I=40mA	-
Color	White						

LED circuit：



Circuit Diagram
IF=20*2mA=40mA

6.Power on/off Sequence



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	CASE A : VDDI Rise time	100	-	-	us
	CASE B : VDDI Rise time	10	-	-	us
T_{VCI_RISE}	CASE A : VCI Rise time	130	-	-	us
	CASE B : VCI Rise time	40	-	-	us
T_{PS_RES}	All Power on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 92: Power on/off sequence with Power Mode 3

7.AC characteristics

<Reset Input timings>

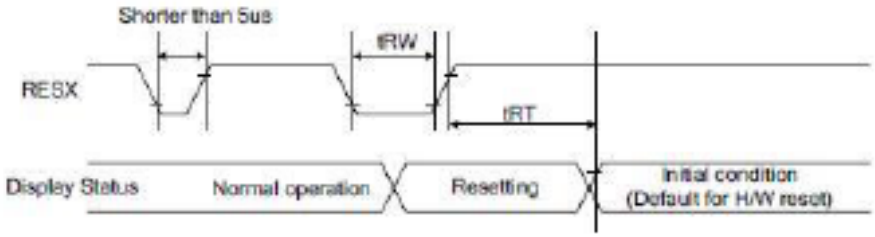


Figure 109: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

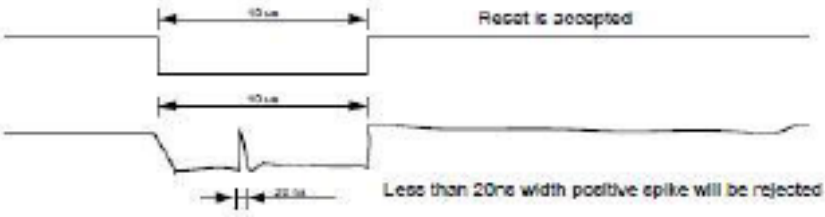


Figure 110: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.High-Speed Mode-Clock Channel Timing

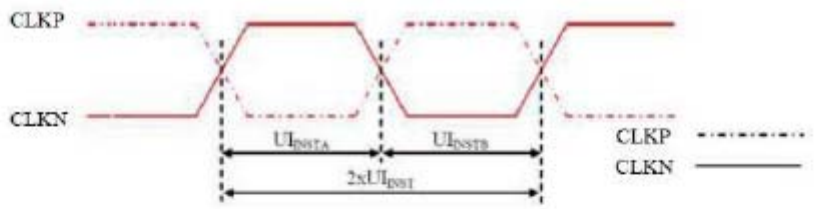


Figure 101: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	2xUI$_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	UI$_{INSTA}$,UI$_{INSTB}$ (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

8.1 High-Speed Mode-Data Clock Channel Timing

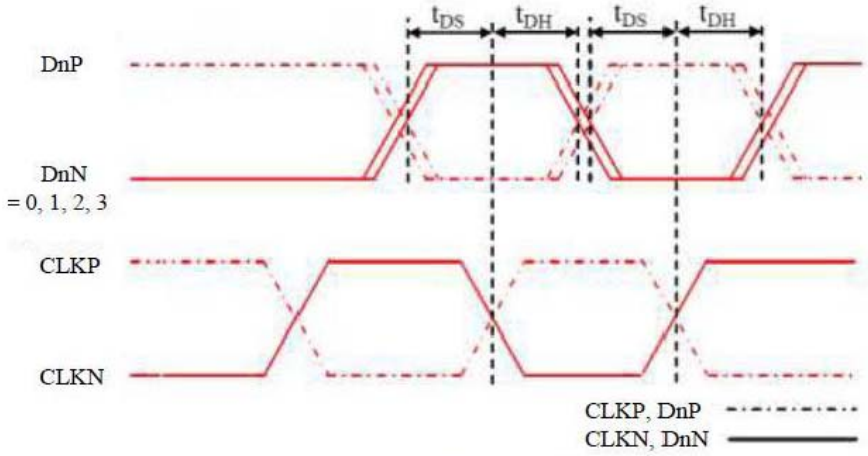


Figure 102: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0,1,2,3	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

8.2 High-Speed Mode-Rising and Falling Timing

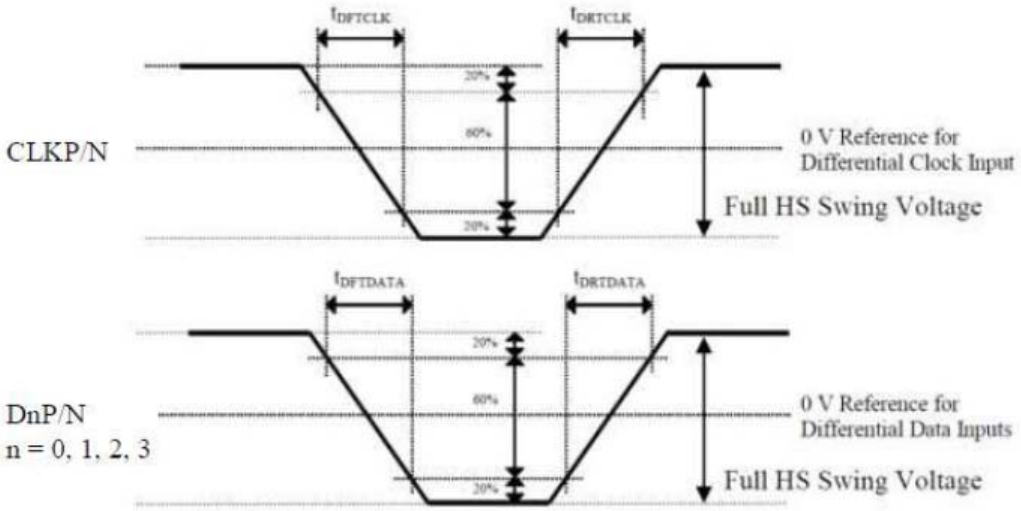


Figure 103: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

8.3 Low-Speed Mode-Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881D-03) are illustrated for reference purposes below.

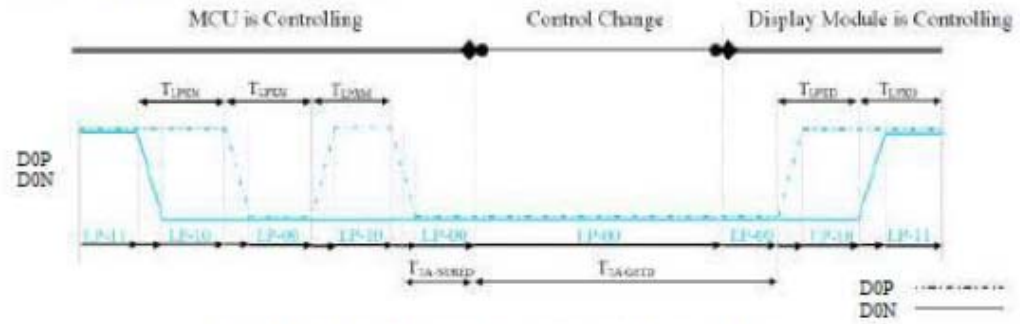


Figure 104: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881D-03) to the MCU are illustrated for reference purposes below.

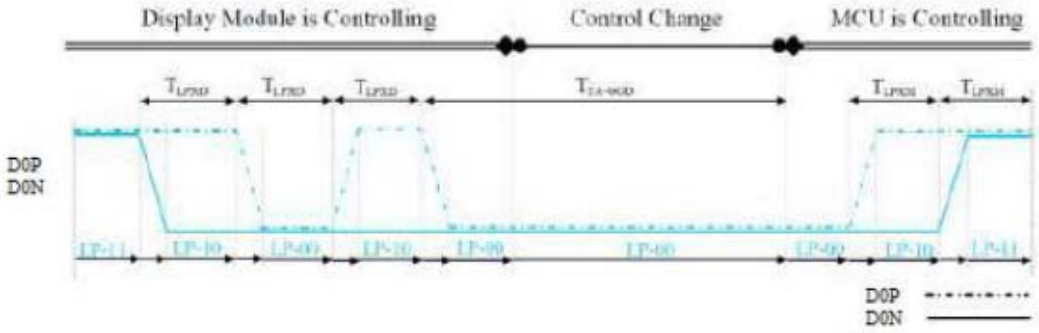


Figure 105: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881D-03)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881D-03) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881D-03) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881D-03)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

8.4 Data Lanes from Low Power Mode to High Speed Mode.

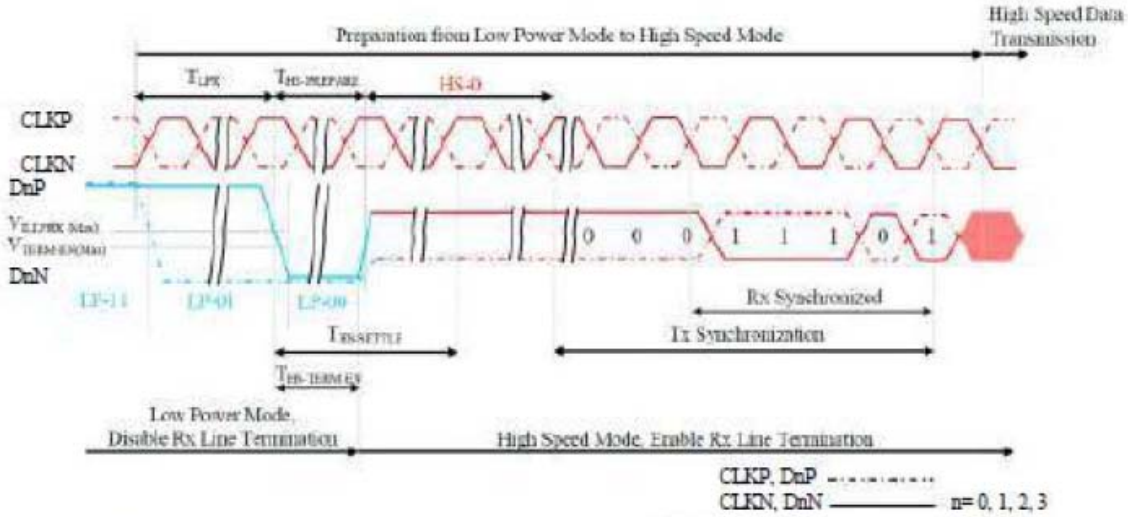


Figure 106: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0,1,2,3	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0,1,2,3	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0,1,2,3	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

8.5 Data Lanes from High Speed Mode to Low Power Mode.

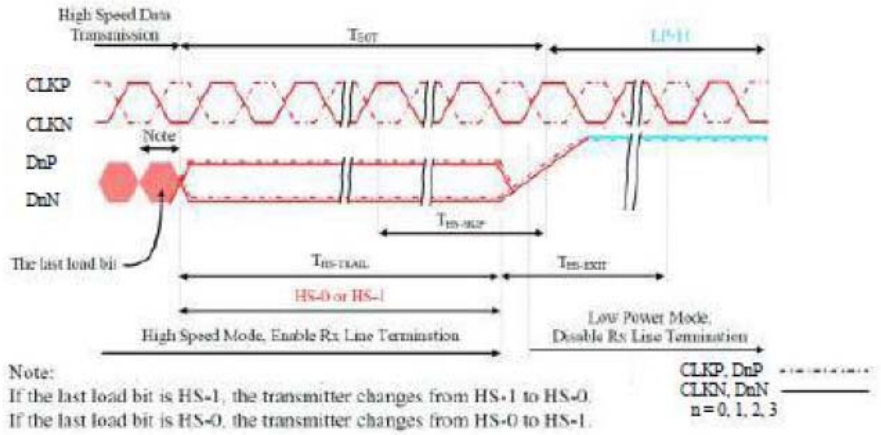


Figure 107: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0,1,2,3	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881D-03) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0,1,2,3	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

8.6 Timings for DSI Video mode.

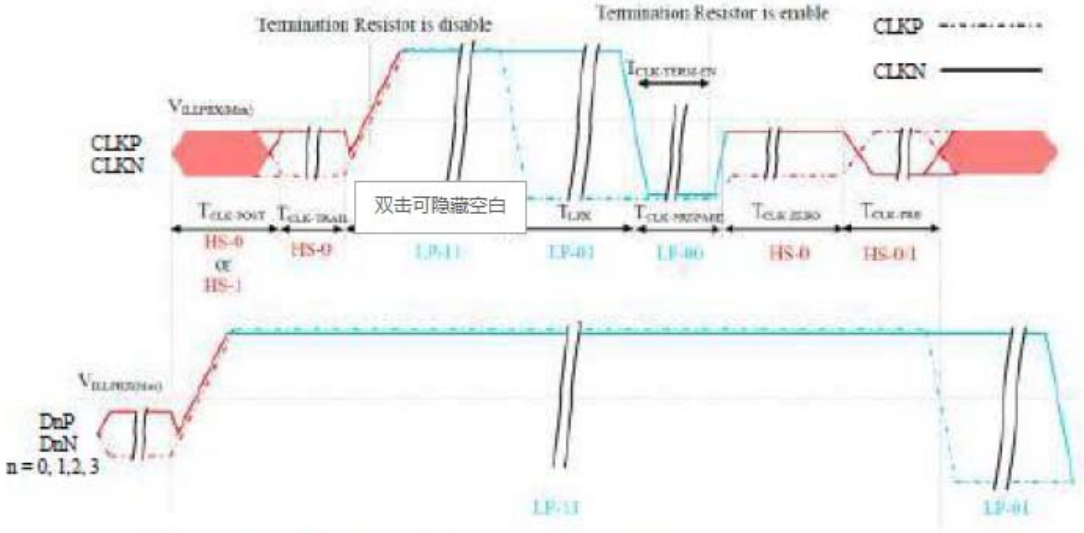
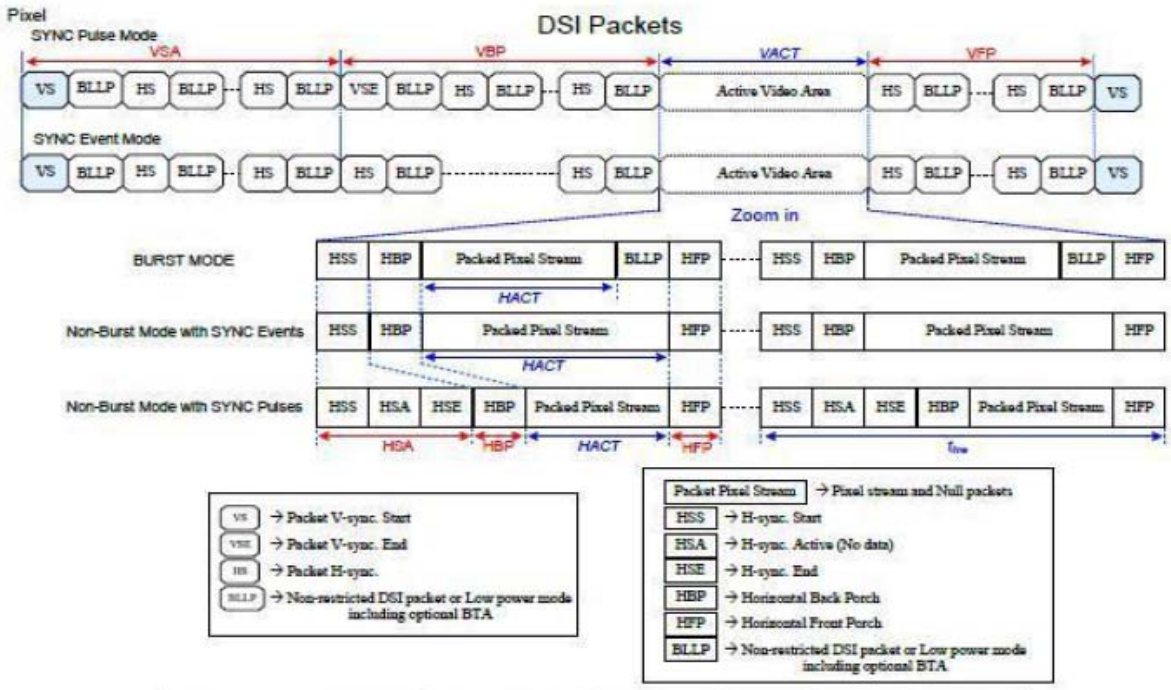


Figure 108: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

8.7 DSI Clock Burst-High Speed Mode to/from Low Power Mode.



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	4	-	Line
Vertical Back Porch	VBP	14 (Note 6)	12	-	Line
Vertical Front Porch	VFP	8 (Note 6)	18	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	12	-	Pixel
Horizontal Porch period	HSA + HBP + HFP		112	-	Pixel
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	492		Note 5	Mbps/lane

1 UI=1/Bit rate

HAS(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Exmple: Frame Rate=60Hz,VSA=4,VBP=12,VFP=18,VACT=1280,HSA=10,HBP=60,HFP=42,Lane=4, Pixel Format=24bit

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to "4.1DSI System Interface".
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~65 Hz / 4 data lanes：50~65 Hz.
5. Please reference to "Table 39: Limited Clock Channel Speed".
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

9.Optical Specification

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Response time	Tr+Tf	Θ=0O Ø=0o Ta=25˚C	-	25	35	ms	
Contrast ratio	Cr		600	1000			
Viewing angle range	Θx+	CR≧10 Ta=25˚C	-	80	-	deg	
	Θx-		-	80	-	deg	
	Θy+		-	80	-	deg	
	Θy-		-	80	-	deg	
LCM Luminance	LV	Θ=0o Ø=0o Ta=25˚C	720	900			
CIE(X,Y)Chromaticity	White(X)		0.260	0.290	0.330		
	White(Y)		0.265	0.300	0.340		
NTSC ratio				70		%	

Note1.Response time is the time required for the display to transition from White to black(Rise Time,Tr) and from black to white(Decay Time,Tf).For additional information see FIG1...

Note2.contrast Ratio(CR) is defined mathematically by the following formula ,For more information see FIG2.

Contrast Ratio(CR)=Average Surface Luminance with all white pixels/ Average Surface Luminance with all black pixels Note3.The uniformity in surface luminance(WHITE) is determined by measuring luminance at eath test p osition,and then dividing the maximum luminance of all white pixels by minimum luminance of all whit e pixels,For more information seeFIG2.

WHITE=Minimum Surface Luminance with all white pixels(P1,P2,.....)/Maximum Surface Luminance wi th all white pixels(P1,P2,.....)

10.Reliability Test Items

Item	Test Condition	Criterion
High Temperature Operation	60 ℃, 48 hrs	Note1，Note2
High Temperature Operation	-10 ℃, 48 hrs	
High Temperature Storage	70 ℃, 48 hrs	
Low Temperature Storage	-20 ℃, 48 hrs	
High Temp. & High Humidity Storage	40 ℃, 90％ RH, 48hrs	

Note1:Evaluation should be tested after storage at room temperature for two hours.

Note2:

Pass: Normal display image no line defect.

Fail: No display image, or line defects.

Partial transformation of the module parts should be ignored.

11.Precautions

Please pay attentions to the followings as using the LCD module.

Handling

(a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.

(b) Because the polarizer is very fragile and easy to be damaged, do not hit, press or rub the display s urface with hard materials.

(c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.

(d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

(e) Avoid using Ketone type materials (e.g. Acetone), Toluene, Ethyl acid or Methyl chloride to clean t he display surface. It might damage the touch panel surface permanently. The recommended solvents are water and Isopropyl alcohol.

(f) Wipe off water droplets or oil immediately.

(g) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.

(h) Do not touch the output pins directly with bare hands.

(i) Do not disassemble the LCD module.

(j) Do not lift the FPC of Touch Panel.

Storage

(a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.

(b) Do not expose the LCD modules to sunlight directly.

(c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.

(d) Avoid condensation of water. It may cause improper operation.

(e) Please stack only up to the number stated on carton box for storage and transportation. Excessive w eight will cause deformation and damage of carton box.

Operation (a) When mounting or dismounting the LCD modules, turn the power off.

(b) Protect the LCD modules from electric shock.

(c) The Driver IC control algorithms stated above should always obeyed to avoid damaging the LSI an d electronic circuit.

(d) Be careful to avoid mixing up the polarity of power supply for backlight.

(e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cau se non-recoverable damage of electronic components or, nevertheless, burning.

(f) When a static image is displayed for a long time, remnant image is likely to occur.

(g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.

(h) Most of the touch screens have air vent to equalize the inside air pressure to the outside one. The air vent must be open and liquid contact must be avoided as the liquid may be absorbed if the liq uid is accumulated near the air vent.

(i) For the fragility of ITO film, it should avoid to use too tapering pen as the input material.

Touch Panel Mounting Notes

(a) If a cushion is used between bezel/housing and film must be choose as free as enough to absorb t he expansion and contraction to avoid the distortion of film.

(b) The cushion must be placed out of the Viewing Area.

(c) Bezel/Housing edge must be posited between Key Area and Viewing Area. The edge enters the Ke y Area may cause unexpected input if the gap is too narrow or foreign particles like dusts exist be tween Bezel/Housing and ITO film.

(d) Mounting example:

The corner part has conductivity. Do not touch any metal part after mounting.

Others

a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

b) For the fragility of polarizer, it is recommended to attach a transparent protective plate over the di splay surface.

c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic c harge can be minimized

12.HSF Requirements

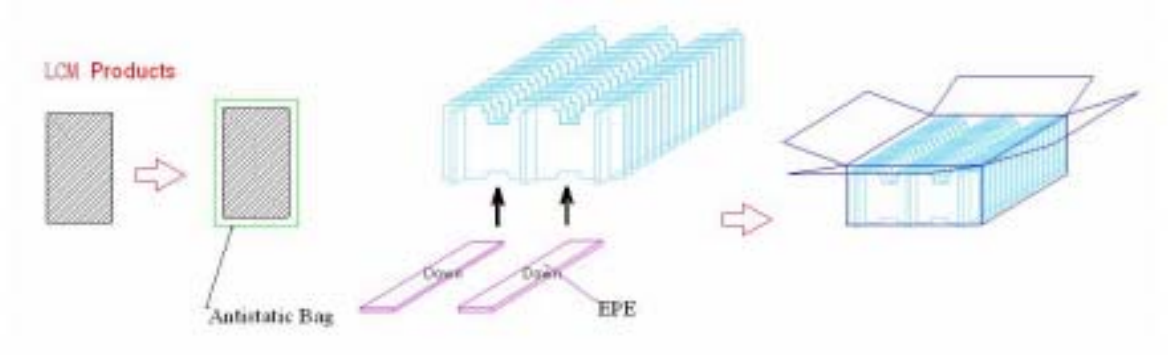
☑ RoHS(Restriction of the use of certain Hazardous Substances)

☐HF (Halogen Free)

☐REACH (Regulation the Registration, Evaluaton, Authorization and Restricton of Chemicals)

☐ Other regulations

13.Packaging diagram



第一步

将产品装入静电袋

第二步

把长卡、短卡组成卡阵（短卡朝向一致）形状和数量按照 BOM 实际物料，卡阵底部放对应的白色珍珠棉后装箱

第三步

每个卡槽内放两片产品，2 片产品显示面相对，中间粉色珍珠棉一起

First step

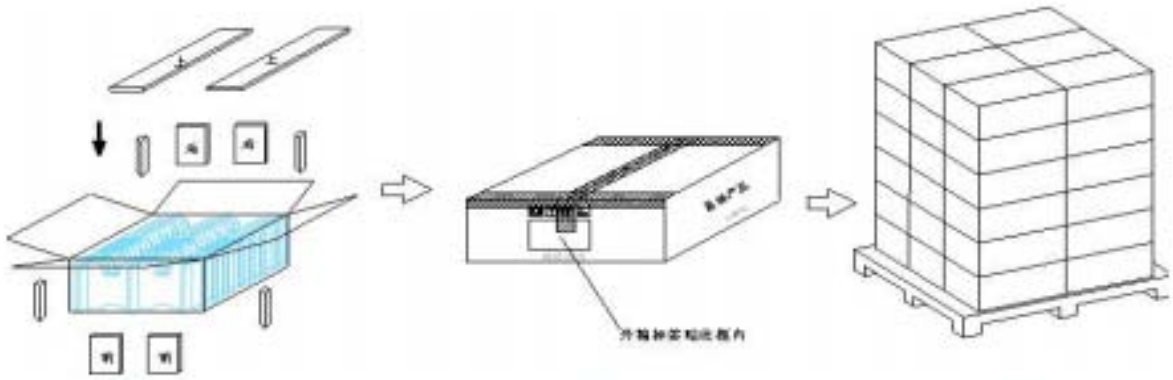
Putting every piece of LCM into anti-static bag.

Second step

Assemble a carton matrix with the right white EPE down below ,then place them into the carton.

Third step

Put a pink EPE between 2 pcs products(face to face) while insert all of them into the carton matrix.



第四步

装箱后，按照 BOM 实际物料在纸箱内侧与卡阵避空位置放白色泡棉

第五步

用胶带封箱，贴外箱标签

第六步

将箱子整齐的放在栈板上并包裹，最高可堆叠泡棉：6 层；

Fourth step

Insert all other white EPE into the right place of the carton matrix .

Fifth step

seal the carton with cellulose tape ;Stick on a carton label,

Sixth step

Place the boxes together on a pallet (6 layers at most),

14.IIS Standard

14. INSPECTION STANDARD

14.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

14.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM CHENGHAO TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 ℃ TO 40 ℃ ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

14.1.2. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (SAME AS MIL-STD-105E) , LEVEL Ⅱ SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

14.1.3. WARRANTY POLICY

CHENGHAO WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. U.R.T. WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF CHENGHAO.

14.2. CHECKING CONDITION

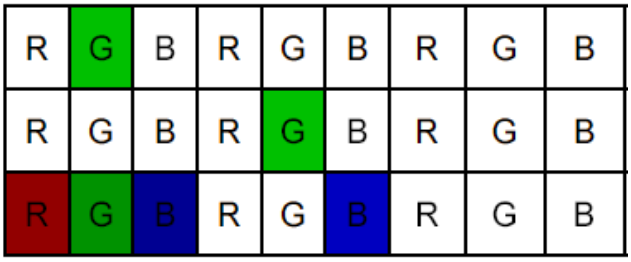
14.2.1. CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

14.2.2. CHECKER SHALL SEE OVER 300±25 mm WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

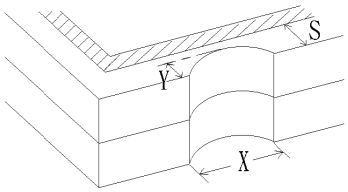
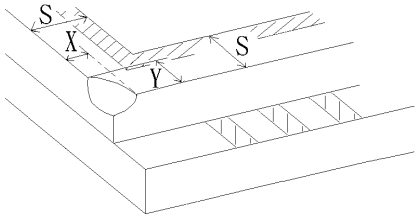
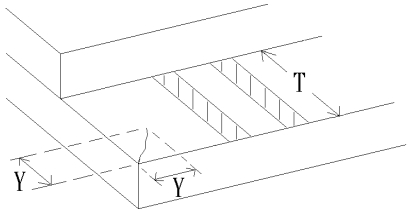
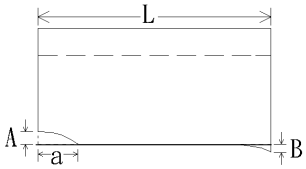
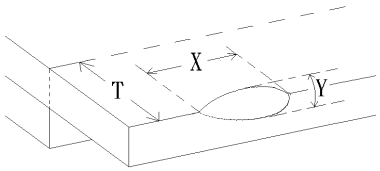
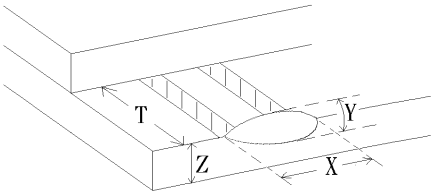
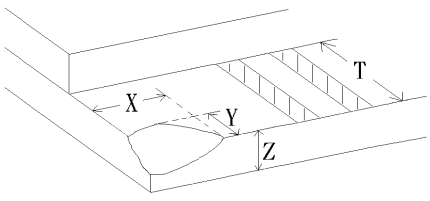
14.3. INSPECTION PLAN :

CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA ……..REJECTED	Minor
	6. BLEMISH、BLACK SPOT、 WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	7. BLEMISH、BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR (OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE (IF NEEDED, AND INSIDE VIEWING AREA)	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS (CONTRAST、VOP、 CHROMATICITY … ETC)	ACCORDING TO SPECIFICATION OR DRAWING . (INSIDE VIEWING AREA)	Critical
	11.MISSING LINE	MISSING DOT、LINE、CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT、 WRONG PATTERN DISPLAY	NO DISPLAY、WRONG PATTERN DISPLAY、CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. DOT DEFECT (FOR COLOR AND TFT)	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

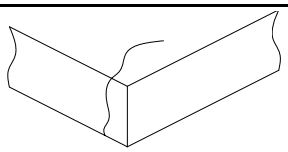
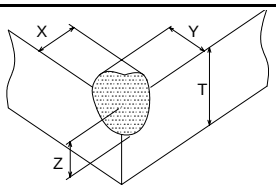
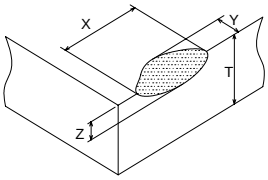
14.4. STANDARD OF VISUAL INSPECTION

<table>
<tr><th>NO.</th><th>CLASS</th><th>ITEM</th><th>JUDGEMENT</th></tr>
<tr><td>14.4.1</td><td>MINOR</td><td>BLACK AND WHITE SPOT
FOREIGN MATERIEL
DUST IN THE CELL
BLEMISH
SCRATCH</td><td>(A) ROUND TYPE: unit : mm.
<table>
<tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.25</td><td>3 (D>5mm)</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
NOTE: Φ=(LENGTH+WIDTH)/2
(B) LINEAR TYPE: unit : mm.
<table>
<tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>------</td><td>W ≦0.03</td><td>DISREGARD</td></tr>
<tr><td>L ≦ 5.0</td><td>0.03 < W ≦0.07</td><td>3 (D>5mm)</td></tr>
<tr><td>------</td><td>0.07 < W</td><td>FOLLOW ROUND TYPE</td></tr>
</table></td></tr>
<tr><td>14.4.2</td><td>MINOR</td><td>BUBBLE IN POLARIZER
DENT ON POLARIZER</td><td>unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦0.2</td><td>DISREGARD</td></tr>
<tr><td>0.2 < Φ ≦ 0.5</td><td>2 (D>5mm)</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>14.4.3</td><td>MINOR</td><td>Dot Defect</td><td>
<table>
<tr><th>Items</th><th>ACC. Q'TY</th></tr>
<tr><td>Bright dot</td><td>N≦ 4 (D>5mm)</td></tr>
<tr><td>Dark dot</td><td>N≦ 4 (D>5mm)</td></tr>
</table>
Pixel Define


Not 1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
Not 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
Not 3: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green ,blue pattern.</td></tr>
</table>

NO.	CLASS	ITEM	JUDGEMENT
14.4.4	MINOR	LCD GLASS CHIPPING	 Y > S Reject
14.4.5	MINOR	LCD GLASS CHIPPING	 X or Y > S Reject
14.4.6	MAJOR	LCD GLASS GLASS CRACK	 Y > (1/2) T Reject
14.4.7	MAJOR	LCD GLASS SCRIBE DEFECT	 1. a> L/3 , A>1.5mm. Reject 2. B : ACCORDING TO DIMENSION
14.4.8	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL AREA)	 Φ= (x+y)/2 > 2.5 mm Reject
14.4.9	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL SURFACE)	 Y > (1/3) T Reject
14.4.10	MINOR	LCD GLASS CHIPPING	 Y > T Reject

14.5 INSPECTION STANDARD OF TOUCH PANEL (Contains the CTP)

NO.	CLASS	ITEMS		JUDGEMENT	
14.5.1	MAJOR	Touch Panel Crack			Reject
14.5.2	MINOR	Touch Panel Chipping	Corner		X≦2mm, Y≦2mm, Z＜1/2T　Accept
			Edge		X≦3mm, Y≦3mm, Z＜1/2T　Accept
14.5.3	MINOR	Scratch Dust and Foreign materiel (Linear Type)		W≦0.05, L≦5.0mm	Accept
				0.05mm<W≦0.07mm；L≦5.0mm Distance between seratch＞5.0mm	Accept 3 ea Max.
				W>0.07mm	Reject
14.5.4	MINOR	Scratch Dust and Foreign materiel (Round Type：Φ=(Length+Width)/2)		Φ≦0.25mm	Accept
				0.25mm＜Φ≦0.35mm Distance between spots＞5.0mm	Accept 5 ea Max.
				Φ＞0.35mm	Reject
14.5.5	MINOR	Touch Panel Dent / Fish Eyes		Φ≦0.35mm	Accept
				0.35mm＜Φ≦1.0mm Distance ＞5.0mm	Accept 3 ea Max.
				Φ＞1.0mm	Reject
14.5.6	MINOR	Touch Panel Air Bubble		Φ≦0.2mm	Accept
				0.2mm＜Φ≦0.5mm Distance between bubbles＞5.0mm	Accept 3 ea Max.
				Φ＞0.5mm	Reject
14.5.7	MINOR	Touch Panel Printing area Scratch		0.03mm＜W≦0.05mm, L≦5mm Distance between scratch＞5.0mm	Accept 3 ea Max.
				W＞0.05mm or L＞5mm (W>0.05 Follow 8.5.4 Round type)	Reject
14.5.8	MINOR	Touch Panel White Haze Mark / Dust		Can not be removed	Reject