



**DDR5 4800 / 5200 / 5600 / 6000 / 6400
8GB With 1Gbx16 ETT / 288 Pin UDIMM**

NEO FORZA DDR5 8GB-4800 / 5200 / 5600 / 6000 / 6400 UDIMM

General Description

This chapter gives an overview of the 288-pin DDR5 unbuffered dual in-line memory modules product family and describes its main characteristics.

Features

1. 288-Pin UDIMM (Lead-Free) DDR5 SDRAM Memory Module.
2. Data transfer rates: PC5-38400 / 41600 / 44800 / 48000 / 51200.
3. Power supply: VDD: 1.067V ~ 1.166V.
4. Module organization: 1024Meg × 64.
5. DRAM organization: 1024Mb × 16.
6. 16 internal banks; 4 groups of 4 banks each.
7. 16-bit prefetch.
8. BL16, BC8 OTF, BL32, BL32 OTF supported.
9. DFE (Decision Feedback Equalization) for DQ.
10. On-Die ECC.
11. Same Bank Refresh.
12. On Die Termination(ODT) via Mode Register setting.
13. Connectivity Test (CT)

Ordering Information for Compliant Products

Part Number	Compliance Code	Number of Rank s	DRAM Organisa-tion	# of SDRAMs
MM5U8GG4PG-4800C-A00	8GB / PC5-38400 / 40-40-40	1	1Gb x16	4
MM5U8GG4PG-5200C-A00	8GB / PC5-41600 / 42-42-42	1	1Gb x16	4
MM5U8GG4PG-5600C-A00	8GB / PC5-44800 / 46-46-46	1	1Gb x16	4
MM5U8GG4PG-6000C-A00	8GB / PC5-48000 / 48-48-48	1	1Gb x16	4
MM5U8GG4PG-6400C-A00	8GB / PC5-51200 / 52-52-52	1	1Gb x16	4



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Pin Assignments

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V _{SS}	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	V _{SS}
2	RFU	38	V _{SS}	74	V _{SS}	110	DQ5_B	146	VIN_BULK	182	V _{SS}	218	V _{SS}	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	V _{SS}	147	PWR_GOOD	183	DQ23_A	219	RFU	255	V _{SS}
4	HSCL	40	V _{SS}	76	RFU	112	DQ8_B	148	HSA	184	V _{SS}	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	V _{SS}	113	V _{SS}	149	RFU	185	DQ26_A	221	V _{SS}	257	V _{SS}
6	V _{SS}	42	V _{SS}	78	CK0_B_t	114	DQ9_B	150	V _{SS}	186	V _{SS}	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	V _{SS}	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	V _{SS}
8	V _{SS}	44	V _{SS}	80	V _{SS}	116	DM1_B_n	152	RFU	188	V _{SS}	224	V _{SS}	260	DQ51_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	V _{SS}	153	V _{SS}	189	DQ53_A_c	225	RFU	261	DQ51_B_t
10	V _{SS}	46	V _{SS}	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQ53_A_t	226	RFU	262	V _{SS}
11	DQ1_A	47	DQ28_A	83	V _{SS}	119	V _{SS}	155	V _{SS}	191	V _{SS}	227	V _{SS}	263	DQ14_B
12	V _{SS}	48	V _{SS}	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	V _{SS}
13	DQ50_A_c	49	DQ29_A	85	CA8_B	121	V _{SS}	157	V _{SS}	193	V _{SS}	229	CA9_B	265	DQ15_B
14	DQ50_A_t	50	V _{SS}	86	V _{SS}	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	V _{SS}	266	V _{SS}
15	V _{SS}	51	CB0_A	87	CA6_B	123	V _{SS}	159	V _{SS}	195	V _{SS}	231	CA7_B	267	DQ18_B
16	DQ4_A	52	V _{SS}	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	V _{SS}
17	V _{SS}	53	CB1_A	89	V _{SS}	125	V _{SS}	161	V _{SS}	197	V _{SS}	233	V _{SS}	269	DQ19_B
18	DQ5_A	54	V _{SS}	90	CA2_B	126	DQ52_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	V _{SS}
19	V _{SS}	55	DQ54_A_c	91	CA0_B	127	DQ52_B_t	163	V _{SS}	199	V _{SS}	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQ54_A_t	92	V _{SS}	128	V _{SS}	164	DQ10_A	200	ALERT_n	236	V _{SS}	272	V _{SS}
21	V _{SS}	57	V _{SS}	93	CS0_B_n	129	DQ20_B	165	V _{SS}	201	V _{SS}	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	V _{SS}	130	V _{SS}	166	DQ11_A	202	CS1_A_n	238	V _{SS}	274	V _{SS}
23	V _{SS}	59	V _{SS}	95	RESET_n	131	DQ21_B	167	V _{SS}	203	V _{SS}	239	DQ54_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	V _{SS}	132	V _{SS}	168	DQ51_A_c	204	CA1_A	240	DQ54_B_t	276	V _{SS}
25	V _{SS}	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQ51_A_t	205	CA3_A	241	V _{SS}	277	DQ26_B
26	DQ12_A	62	V _{SS}	98	V _{SS}	134	V _{SS}	170	V _{SS}	206	V _{SS}	242	CB2_B	278	V _{SS}
27	V _{SS}	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	V _{SS}	279	DQ27_B
28	DQ13_A	64	CA6_A	100	V _{SS}	136	V _{SS}	172	V _{SS}	208	CA7_A	244	CB3_B	280	V _{SS}
29	V _{SS}	65	V _{SS}	101	DQ0_B	137	DM3_B_n	173	DQ15_A	209	V _{SS}	245	V _{SS}	281	DQ53_B_c
30	DQ16_A	66	CA8_A	102	V _{SS}	138	V _{SS}	174	V _{SS}	210	CA9_A	246	DQ2_B	282	DQ53_B_t
31	V _{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B	175	DQ18_A	211	CA11_A	247	V _{SS}	283	V _{SS}
32	DQ17_A	68	V _{SS}	104	V _{SS}	140	V _{SS}	176	V _{SS}	212	V _{SS}	248	DQ3_B	284	DQ30_B
33	V _{SS}	69	CA12_A	105	DQ50_B_c	141	DQ29_B	177	DQ19_A	213	RFU	249	V _{SS}	285	V _{SS}
34	DQ52_A_c	70	RFU	106	DQ50_B_t	142	V _{SS}	178	V _{SS}	214	RFU	250	DM0_B_n	286	DQ31_B
35	DQ52_A_t	71	V _{SS}	107	V _{SS}	143	RFU	179	DM2_A_n	215	V _{SS}	251	V _{SS}	287	V _{SS}



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Pin Assignments (Continued)

288-Pin DDR5 UDIMM Front							288-Pin DDR5 UDIMM Back								
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
36	V _{SS}	72	CK0_A_t	108	DQ4_B	144	RFU	180	V _{SS}	216	CK1_A_t	252	DQ6_B	288	RFU



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Pin Descriptions

Symbol	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command / Address bus
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select
DQ0_A – DQ31_A, DQ0_B – DQ31_B,	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)

Symbol	Description
HSCL	SidebandBus clock
HSDA	SidebandBus data
HAS	SidebandBus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a known state
V _{in} _BULK	5V power input supply to the PMIC for analog circuits
V _{ss}	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

Note:

DDR5 UDIMM has 2 channels (channel-A and channel-B) of signal bus.

The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B



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DIMM Voltage Requirements

Symbol	Parameter	Voltage Rating (V)			Maximum Expected Current (A)	Power State
		Min.	Typ.	Max.		
V _{IN_BULK}	Host Supply Voltage	4.25	5.0	5.5	2.5 / 2.0	Operational
SWA, SWB	PMIC Output Supply Voltage	-	1.1	-	6	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	12	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	2	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020	Operational

Note:

1. During first power on the input voltage supply must reach minimum 4.25V for PMIC to detect valid input supply.
2. The ramp up rate between 300 mV and 4.0V.
3. The ramp down rate between 4V and 300 mV.
4. The area under the curve above V_{IN_Bulk} = TBD V. V_{IN_Bulk_AC} spec must also be satisfied.
5. The minimum input current requirement is to deliver the maximum output current on V_{OUT_1.8V} and V_{OUT_1.0V} LDO plus the current.
6. V_{IN_Bulk} = 5.0V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR_EN signal is static.
7. V_{IN_Bulk} = 5.0V. Measured at room temperature. All output regulators and LDOs are on with 0 A output load.. VR_EN signal is static.
8. 20MHz bandwidth limited measurement for all voltage in the table.
9. Voltages are measured at the DIMM gold fingers and at PMIC output pins.
10. The SDRAM specification must be met and take precedence over this document.
11. Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances.
12. Typical voltage is platform dependent. This is a suggested value only.
13. Follow JEDEC specification.

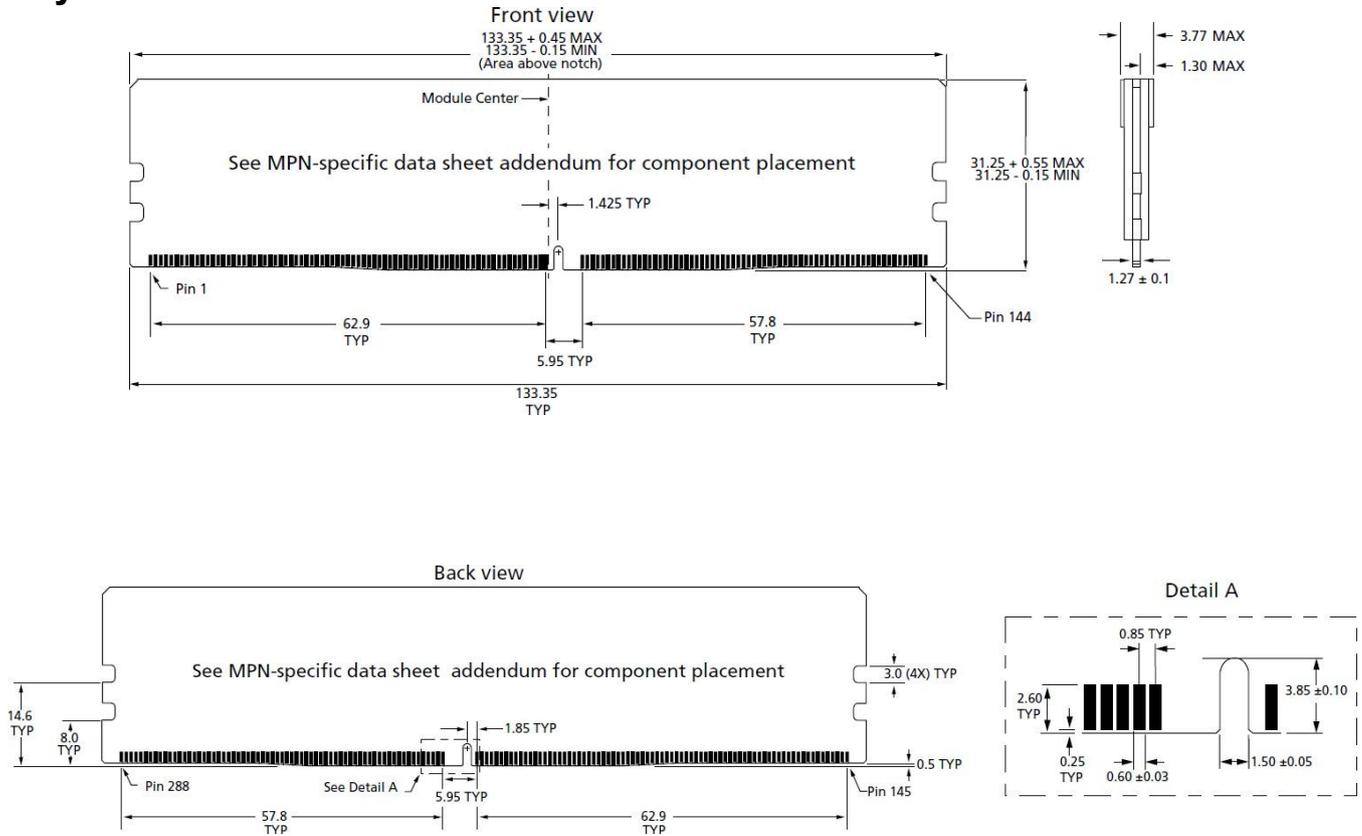
Recommended Operating Temperature Ranges

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,3

Note:

- The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer to JESD51-2.
- Normal is the maximum limit when device is operating in the Normal Temperature Mode.
- Extended is the maximum limit when device is operating in the Extended Temperature Mode.

Physical Dimensions



- Note: 1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
 2. Tolerance on all dimensions ± 0.15 unless otherwise specified.
 3. The dimensional diagram is for reference only.