AMD Zynq UltraScale+ RFSoC
CRZU49DRB
User Manual

Version Records:

Data	Version	Description
2025.02.25	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

Content

Part 1: Zynq UltraScale+ RFSoC General Description

The RFSoC (Radio Frequency System-on-Chip) is a highly integrated chip solution that combines components such as an RF front-end, ADC/DAC (analogue-to-digital converter/digital-to-analogue converter), processor, and FPGA (Field Programmable Gate Array) into a single chip. The following is a detailed description of RFSoC:

✓ **Composition & Structure**

RFSoCs typically consist of two parts, PL (programmable logic) and PS (processing system). Of these, the RF-related part is hardware-based but programmable.

The key parts of an RFSoC include:

RF Data Converter (RFDC) block: an integrated ADC and DAC that operates at high sampling rates and directly samples many radio signals. also contains digital upconverters (DUCs) and digital downconverters (DDCs) for converting between baseband (near 0Hz signals) and modulation frequencies.

Soft Decision Forward Error Correction (SD-FEC) blocks: soft-decision forward error correction modules used to mitigate errors introduced by the radio channel.

Gigabit Transceivers (GTY Transceivers): RFSoCs are used to implement radio front ends, but require high speed links to the core network, these are usually implemented as wired or optical. the RF SoCs support the required interfaces, which are provided by hardened GTY transceiver blocks, high rate serial interfaces.

Programmable Logic (PL): programmable hardware resources for implementing custom radio architectures.

Processing System (PS): Includes a quad-core Application Processing Unit (APU), a dual-core Real-time Processing Unit (RPU), as well as Platform Management (PMU) and security features. There is also local memory, interconnect and peripheral interfaces.

✓ **Features and Advantages**

Highly integrated: RFSoC integrates RF transmit and receive functions, as well as computation and security capabilities, resulting in a higher level of integration compared to traditional MPSOCs.

High performance: RFSoC supports high sample rate ADCs and DACs with excellent dynamic range performance to provide high quality RF signal processing and conversion.

Programmable: RFSoC provides rich programmable logic resources, allowing users to customise the radio architecture to achieve flexible application scenarios.

Low Power Consumption: RFSoC adopts advanced processes and technologies to achieve low power RF signal processing, which is suitable for scenarios with stringent requirements on power consumption.

✓ **Application**

RFSoCs are widely used in communication, radar, satellite communication and other fields, specifically including but not limited to:

Communication field: RFSoC is particularly used in 5G base stations, enabling miniaturisation and low power consumption, which is crucial for the deployment of Massive MIMO technology. With the

development of 5G technology, the application of RFSoC in communication base stations is promising.

Radar system: RFSoC can be used as a hardware processing platform for radar system boards composed of ADC+FPGA+DSP/ARM, etc., which helps to improve the performance of radar, especially in radar systems that are developing in the direction of MIMO and digital arrays.

Satellite communication: RFSoC provides high speed multifunctional instruments for signal generation and signal analysis, which have a wide range of applications in the field of satellite communication.

Education and Research: RFSoC is also used in education and research, for example, the PYNQ team released the RFSoC-PYNQ open source framework, which provides rich resources for learning and research.

Test and Measurement: Designers can use RFSoC for signal generation and signal analysis to build high-speed multifunctional instruments, which has potential applications in the test and measurement field.

✓ **Development Trend**

As technology continues to advance and application needs continue to grow, the main trends in RFSoC development include:

Higher integration: future RFSoCs will integrate more RF components and functions to further improve integration and performance.

Lower power consumption: using advanced processes and technologies to reduce the power consumption of RFSoC to meet the application scenarios that have strict requirements on power consumption.

Stronger programmable: Provide more programmable logic resources and interfaces to support user-defined radio architectures and algorithms for more flexible application scenarios.

Broader application areas: With the continuous development of 5G, IoT, autonomous driving and other technologies, the application areas of RFSoC will be further expanded.

In summary, RFSoC, as a highly integrated chip solution, has a wide range of application prospects and development potential in the field of communications, radar, satellite communications and other areas.

The Zynq UltraScale+ RFSoC device resources are listed in the table below, and we have chosen the ZU49DR as the main controller for the SOM:

Zynq™ UltraScale+™ RFSoCs

Section	Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
		Gen 1					Gen 2	Gen 3					
PS		**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz, **Dual-core** Arm Cortex-R5F MPCore up to 533MHz											
RF Data Converter	12-bit RF-ADC w/DDC # of ADCs	0	8	8	8	16	16	–	–	–	–	–	–
RF Data Converter	12-bit RF-ADC w/DDC Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–	–
RF Data Converter	14-bit RF-ADC w/DDC # of ADCs	–	–	–	–	–	–	8 2	4	8 4	8	8	16
RF Data Converter	14-bit RF-ADC w/DDC Max Rate (GSPS)	–	–	–	–	–	–	2.5 5.0	5.0	2.5 5.0	5.0	5.0	2.5
RF Data Converter	14-bit RF-DAC w/DUC # of DACs	0	8	8	8	16	16	8	4	12	8	8	16
RF Data Converter	14-bit RF-DAC w/DUC Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	9.85[3]	9.85[3]	9.85[3]	9.85[3]	9.85[3]	9.85[3]
RF Data Converter	SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0
RF Data Converter	Digital Front-End (DFE)	–	–	–	–	–	–	–	–	–	–	–	–
RF Data Converter	Number of DDCs per RF-ADC[1]	0	1	1	1	1	1	1	2	1	1	1	1
RF Data Converter	RF input Freq max. GHz	4					5	6					
RF Data Converter	Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x					
Programmable Logic (PL)	System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930
Programmable Logic (PL)	CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425
Programmable Logic (PL)	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0
Programmable Logic (PL)	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0
Programmable Logic (PL)	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5
Programmable Logic (PL)	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272
Programmable Logic (PL)	GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16
Programmable Logic (PL)	PCIe® Gen3 x16	2	1	2	2	2	2	–	–	–	–	–	–
Programmable Logic (PL)	PCIe® Gen3 x16/Gen4 x8 / CCIX[2]	–	–	–	–	–	–	0	2	2	2	2	2
Programmable Logic (PL)	150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1
Programmable Logic (PL)	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2
Programmable Logic (PL)	System Monitor	2	2	2	2	2	2	2	2	2 2	2	2	2
Programmable Logic (PL)	Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI
Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
D1156	35x35	214, 72, 208 4, 16 0, 0											
E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	
G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8	
F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16
H1760	42.5x42.5									214, 48, 312 4, 16 12, 12			

Part 2: CRZU49DRB FPGA Board Overview

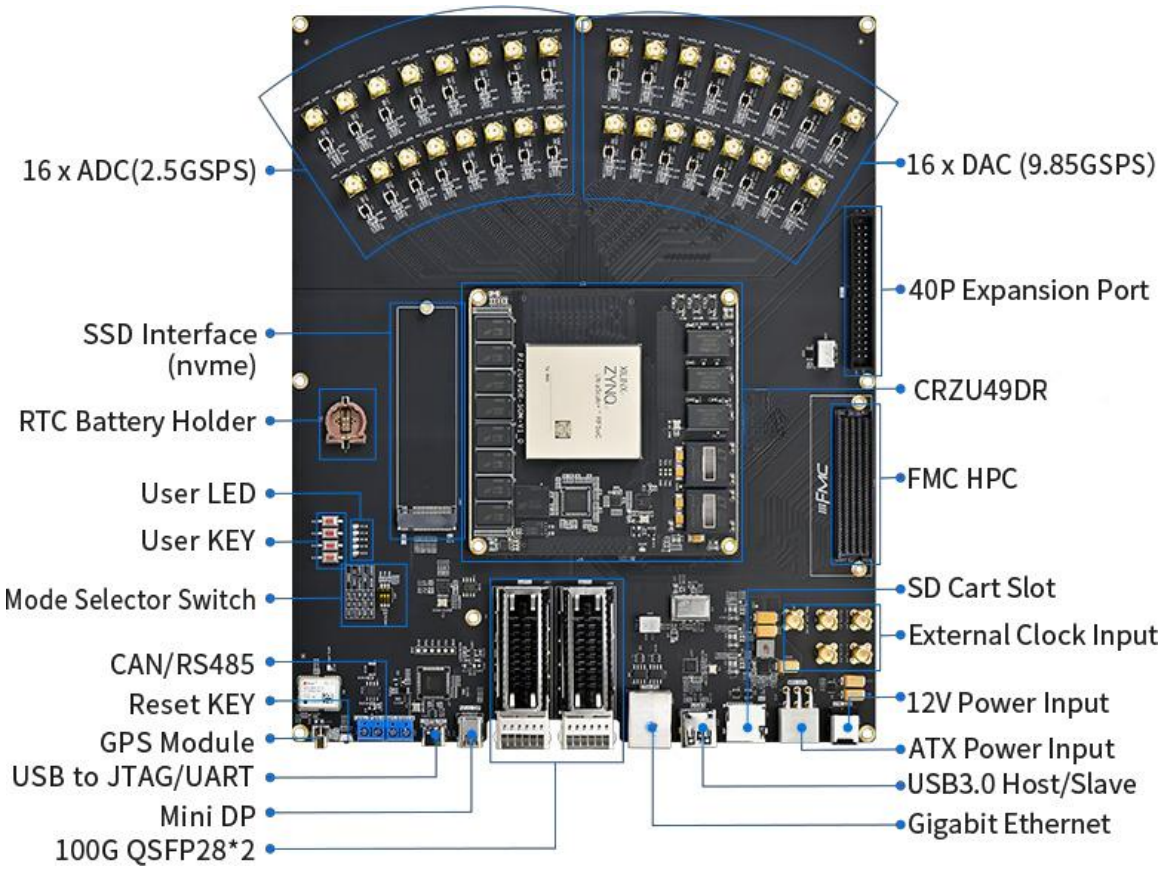
Part 2.1: CRZU49DRB Introduction

The CRZU49DRB FPGA development board uses AMD Xilinx XCZU49DR-2FFVF1760I as the main controller, and is equipped with a high-capacity dual-bank DDR4, mass storage EMMC, and a 16T16R multi-channel ADC/DAC.

The CRZU49DRB FPGA development board adopts the mode of “Core board + Carrier board”. The core board is snapped to the carrier board with four 0.635mm pitch 240P high-speed connectors for more flexible use. It can be used for learning or for project development.

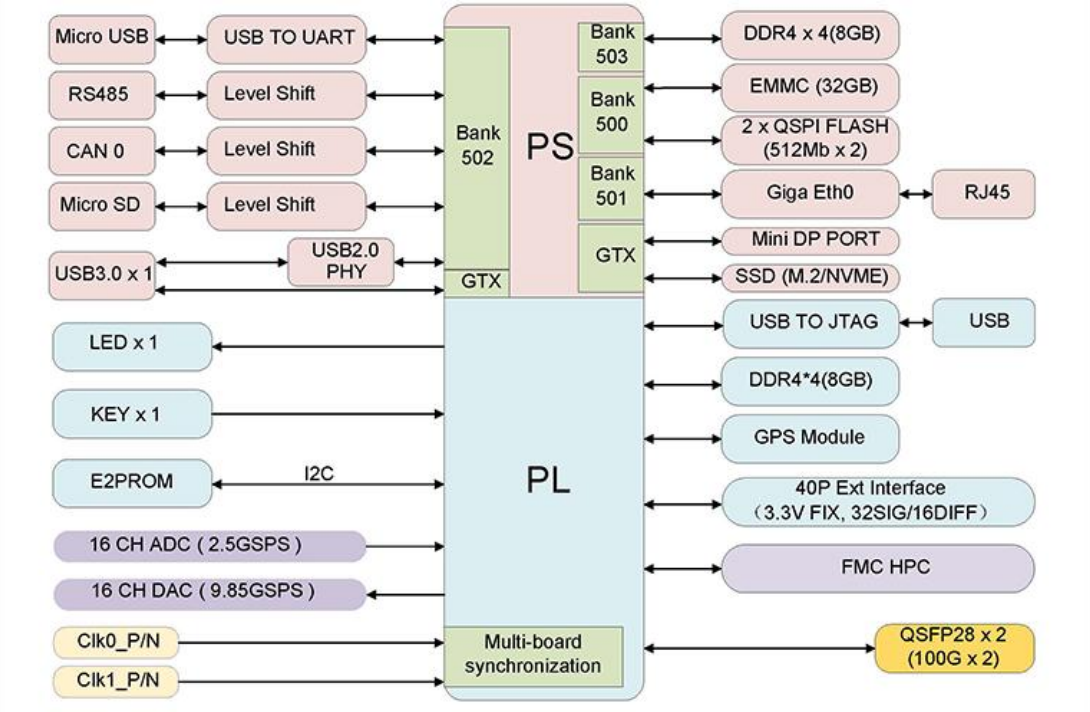
In addition, the board integrates rich peripheral resources and provides detailed development routines, which accelerates the user's learning or project advancement. In addition, the development board also integrates a JTAG debugger, so that a USB cable and a 12V power cable can make the development board work, more convenient to use.

For detailed descriptions of the core board and carrier board, please refer to the corresponding sections below.



Part 2.2: CRZU49DRB Block Diagram

In this section, we will show the configuration details of the product in detail through the product block diagram, as shown below.



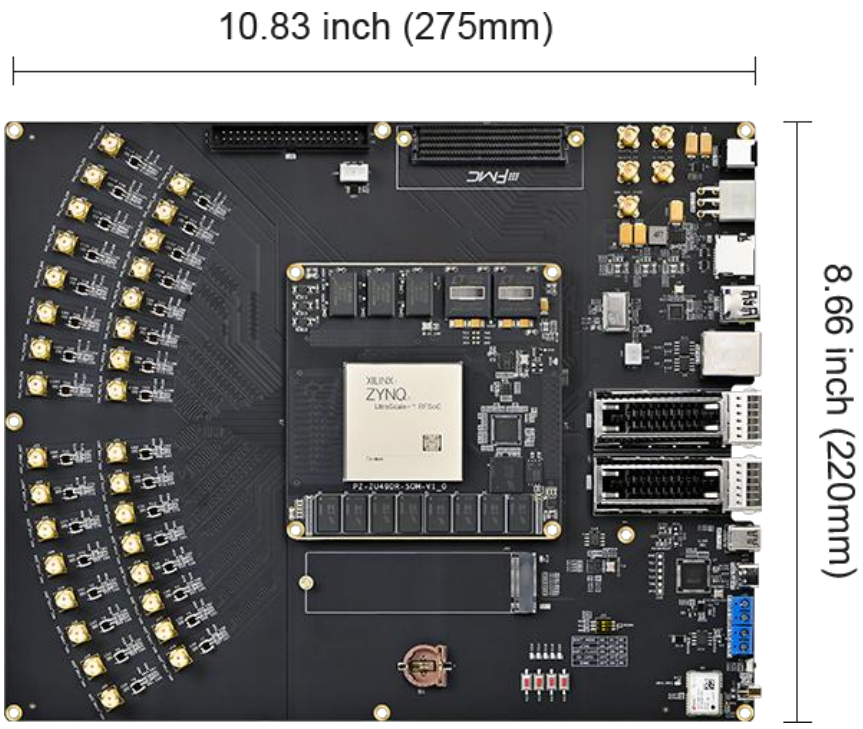
FPGA Development Board	CRZU49DR
FPGA Chip	XCZU49DR-2FFVF1760I
Processor Core	ARM: 4 x Cortex-A53 1.333Ghz RPU: 2 x Cortex-R5 533Mhz
Speed Grade	2
Chip Level	Industrial Grade (-40°C~+85°C)
Logic Cells	930k
Lookup Tables (LUTs)	425k
DSP Slices	4272
BLOCK RAM	38Mb
DDR4	PS Side 8GB 2400Mhz*64bit / PL Side 8GB 2400Mhz*64bit
QSPI FLASH	2 Channel (QSP0+QSPI1)/512Mb per Chip, 1Gb Total
EMMC	32GB, to Store Startup Files and User Files
Start-up Mode	JTAG/QSPI/SD/EMMC, Onboard DIP Switch Selection
ADC Channel	16 Channels / Sample Rate 2.5Gsps
DAC Channel	16 Channels / Sample Rate 9.85Gsps
PS Side GTR Interface	4 Paris of TX/RX
PL Side GTY Interface	16 Paris of TX/RX
Number of Expansion IOs	MIO: 38 (Fixed 1.8V) HP: 144 (1.2/1.8V adjustable, default 1.8V) HD: 96 (1.8/2.5/3.3V adjustable, default 3.3V)
Crystal Oscillator	One Single-ended 33.3333MHz crystal for PS One Differential 200MHz crystal for PL One Differential 125M crystal for GT interface One Dedicated Clock Chip for ADC/DAC
Core Board Form Factors	3.94 inch x 3.94 inch (100mm x 100mm)

Interfaces and Function

JTAG Downloader	1
UART/RS485/CAN	1/ 1/ 1
SD Card Slot Interface	1
PS Side SSD	1
Gigabit Ethernet	PS Side 1
Mini DP Output	1
USB3.0 Master-Slave Port	1
SSD Memory	1
QSFP28 Interface	2/ 100G
GPS Module	1
FMC Interface	FMC HPC, Full Signal Connection
Voltage / Current	12V/3A
Board Form Factors	10.83 inch x 8.66 inch (275mm x 220mm)
Technology	Black Matte, Immersion Gold Process
40Pin Expansion Port	Total of 32 signals (Including 5V power supply , 3V power supply 6 Ground, 32 IOs)

Part 2.3: CRZU49DRB Form Factors

The Form Factors of the FPGA development board is 275mm x 220mm (10.83inch x 8.66inch). The four corners of the FPGA development board is placed in each of the four fixing holes, for the installation of support columns or fixed veneer, hole diameter of 3.5mm. The FPGA development board configured with a fan, heatsink and acrylic protective plate, for the convenience of display, and not installed on the FPGA development board.

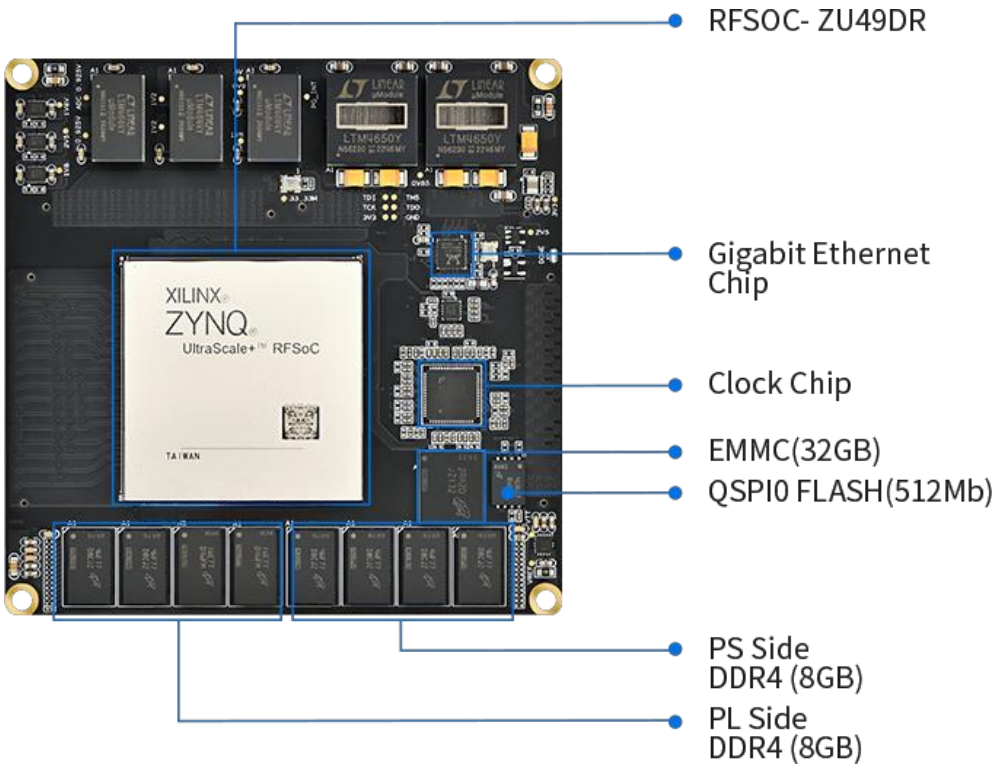


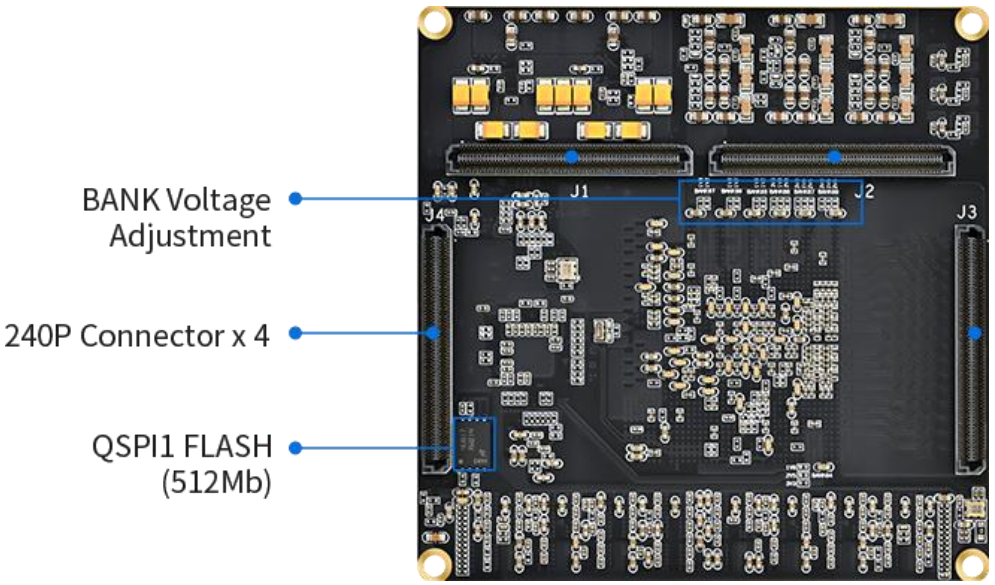
The heat dissipation is made up of customized fans, heat sinks. and acrylic protective plate, for the convenience of display, and not installed on the FPGA development board. The form factors of the heat dissipation as below:

Part 3: CRZU49DRC Overview

Part 3.1: SOM Introduction

The CRZU49DRC core board provides a wealth of on-board resources, and the following diagram details the functional modules of the core board.

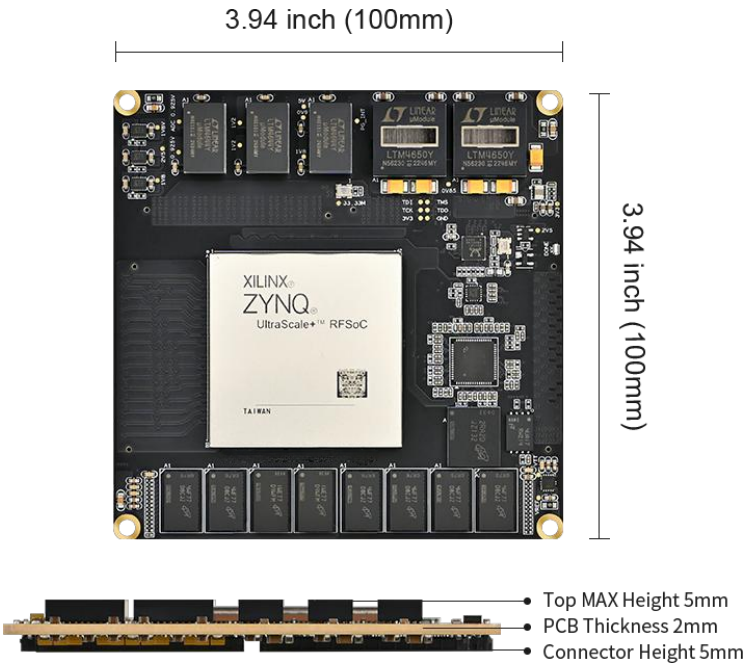




Part 3.2: SOM Specification and Form Factors

The following table lists all the on-board resources of the core board, and details the core board Form Factors.

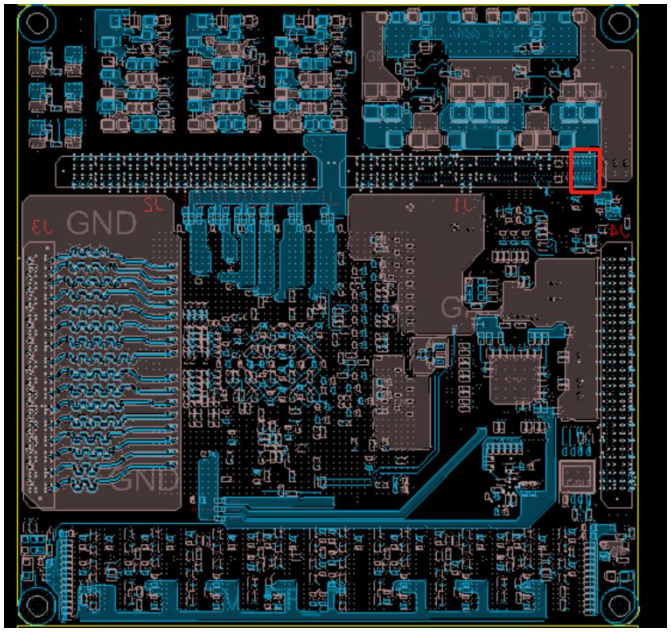
CRZU49DRC Industrial Core Board Specifications	
FPGA Chip	XCZU49DR-2FFVF1760I
Processors	ARM : 4 x Cortex-A53 1.333Ghz RPU : 2 x Cortex-R5 533Mhz
logic cells(K)	930
CLB LUTs（K)	425
Block RAM(Mb)	38
Ultra RAM(Mb)	22.5
DSP Slices	4272
DDR4/DDR4L	PS Side 8GB 2400Mhz * 64bit / PL Side 8GB 2400Mhz * 64bit
QSPI FLASH	2-way (QSP0+QSPI1)/ Single 512Mb, total 1Gb
EMMC	32GB, to Store Startup Files and User Files
Start-up Mode	JTAG/QSPI/SD/EMMC, on-board DIP Switch Selection
Gigabit Ethernet	1 (PS Side)
ADC Channel	16-way/ Sampling Rate 2.5Gsps
DAC Channel	16-way/ Sampling Rate 9.85Gsps
Number of IOs	MIO : 38 IOs (Fixed 1.8V Level) HP : 144 IOs (1.2V/1.8V Adjustable, Default 1.8V) HP : 96 IOs (1.2V/ 2.5V/ 3.3V Adjustable, Default 3.3V)
PS Side GTR Interface	4 Paris of TX/RX
PL Side GTY Interface	16 Paris of TX/RX
Voltage/ Current	8-12V/5A (Recommended Voltage 8V)
Chip Level	Industrial Grade(-40°C~+85°C)
Core Board Form Factors	3.94 inch x 3.94 inch (100mm x100mm)
Technology	Black Matte, Immersion Gold Process, 0.635mm 240 Connectors x 4



Part 3.3: SOM Power Connection

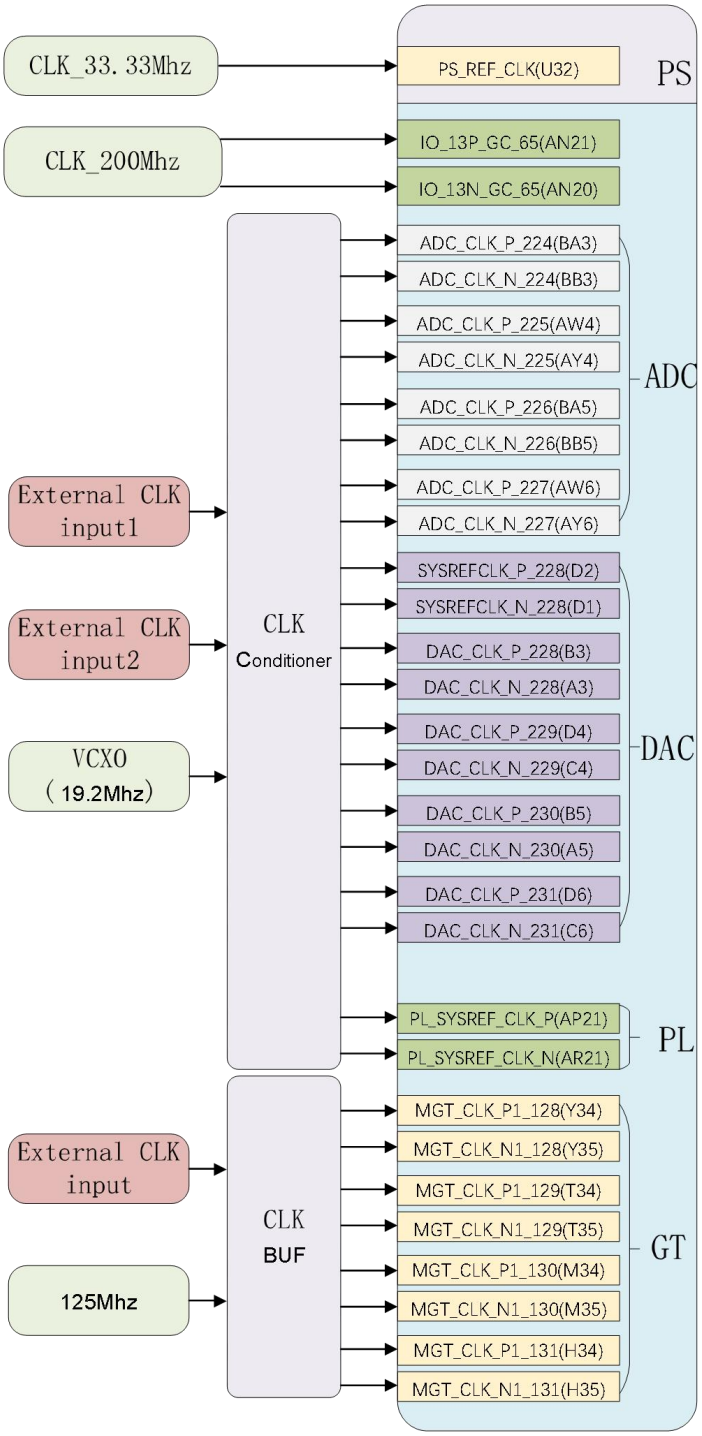
The power supply voltage of the core board is 8-12V, the power supply connection needs to be connected with copper skin and enough holes to ensure the power supply current capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier board through two via holes. Due to the different logic usage of the core board, the limit current of the core board power supply is 12V/6A, so the external power supply needs to take the limit current into consideration to ensure the stability of the core board.

Power supply output voltage to the module needs to be stable, and need to consider the power surge, the core board power input port needs to add a few larger capacitors **(220uF/10V)**, you can add a level of DC2DC chip, to ensure stable power supply.



Part 3.4: SOM Clock

The core board provides a **33.333333Mhz** clock input for the **PS** side, and the pin location of the input is **PS_REF_CLK**; a **200Mhz** differential clock input is provided for the **PL** side, and the clock input pins on the **PL** side are **IO_13P_GC_65/IO_13N_GC_65**, and the pin locations are **AN21/AN20**; The **ZU49DR** uses a dedicated clock chip to generate the clock requirements for each part of the **ADC/DAC/GT/PL** side, and the following figure lists the pin connections for each part of the clock respectively.



Part 3.5: Core Board Reset

The reset circuit is designed on SOM, but there is no reserved reset KEY, the reset KEY is designed on the carrier board.

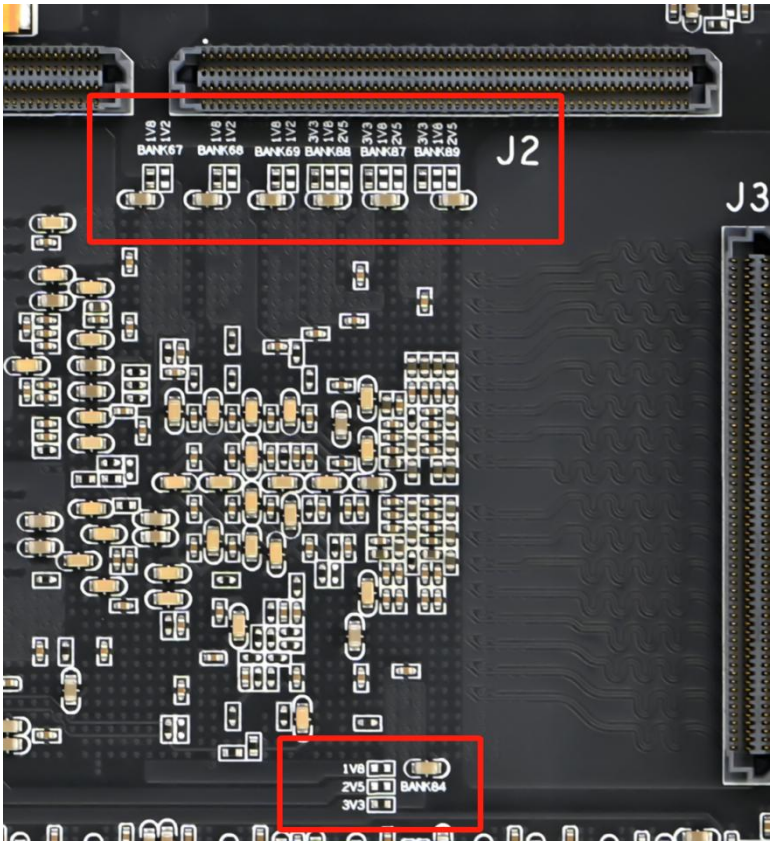
The reset pin is a **PS/PL** shared reset, connected to the **PS_POR_B (U32)** pin on the **PS** side and the **IO_L2P_65 (BA18)** pin on the **PL** side **BANK65**.

Part 3.6: Boot Mode Selection

The main chip supports four boot modes: **JTAG**, **QSPI Flash**, **SD**, and **eMMC**. The **M2/M1/M0** boot mode selection signal is routed via a connector to the carrier board. These four boot modes can be selected using the DIP switches on the development board. For further details, please refer to the core board schematic provided.

Part 3.7: BANK Interface Level Selection

The **BANK67/68/69** on the core board are HP BANK, the interface level is configured as **1.2/1.8V**, the default level is **1.8V**. **BANK84/87/88/89** are **HD BANK**, the interface level can be adjusted **1.8/2.5/3.3V**, the default level is **3.3V**, and the voltage can be adjusted by resistance welding through the instructions provided on the carrier board. The corresponding resistor labeling locations are shown below.



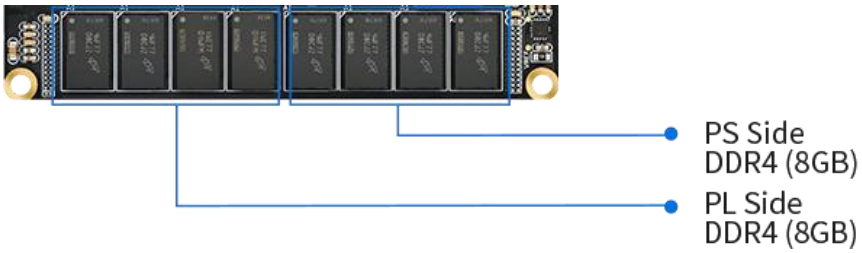
Part 3.8: DDR4

The core board features four **DDR4** modules each on the **PS** and **PL** sides, with a capacity of **2GB** per module, totalling **8GB + 8GB**. The **DDR4** pins on the **PS** side are fixed in position and can be allocated directly within the software. For pin allocation on the **PL** side, refer to the table below. For more detailed information, consult the schematic or example code provided.

PL-DDR4 Pin	Pin Name	Pin Position
PL_DDR4_DQ0	IO_L3N_T0L_N5_AD15N_64	BA12
PL_DDR4_DQ1	IO_L5P_T0U_N8_AD14P_64	BA15
PL_DDR4_DQ2	IO_L3P_T0L_N4_AD15P_64	BA13
PL_DDR4_DQ3	IO_L6P_T0U_N10_AD6P_64	AY15
PL_DDR4_DQ4	IO_L5N_T0U_N9_AD14N_64	BA14
PL_DDR4_DQ5	IO_L2N_T0L_N3_64	BB17
PL_DDR4_DQ6	IO_L6N_T0U_N11_AD6N_64	AY14
PL_DDR4_DQ7	IO_L2P_T0L_N2_64	BA17
PL_DDR4_DM0	IO_L1P_T0L_N0_DBC_64	BB13
PL_DDR4_DQS_P0	IO_L4P_T0U_N6_DBC_AD7P_64	BB16
PL_DDR4_DQS_N0	IO_L4N_T0U_N7_DBC_AD7N_64	BB15
PL_DDR4_DQ8	IO_L12N_T1U_N11_GC_64	AU13
PL_DDR4_DQ9	IO_L11N_T1U_N9_GC_64	AV15
PL_DDR4_DQ10	IO_L8P_T1L_N2_AD5P_64	AV13
PL_DDR4_DQ11	IO_L9N_T1L_N5_AD12N_64	AW16
PL_DDR4_DQ12	IO_L12P_T1U_N10_GC_64	AT13
PL_DDR4_DQ13	IO_L11P_T1U_N8_GC_64	AV16
PL_DDR4_DQ14	IO_L8N_T1L_N3_AD5N_64	AW13
PL_DDR4_DQ15	IO_L9P_T1L_N4_AD12P_64	AW17
PL_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_64	AY17
PL_DDR4_DQS_P1	IO_L10P_T1U_N6_QBC_AD4P_64	AV14
PL_DDR4_DQS_N1	IO_L10N_T1U_N7_QBC_AD4N_64	AW14
PL_DDR4_DQ16	IO_L17N_T2U_N9_AD10N_64	AR15
PL_DDR4_DQ17	IO_L14N_T2L_N3_GC_64	AU15
PL_DDR4_DQ18	IO_L17P_T2U_N8_AD10P_64	AR16
PL_DDR4_DQ19	IO_L14P_T2L_N2_GC_64	AT15
PL_DDR4_DQ20	IO_L18N_T2U_N11_AD2N_64	AP13
PL_DDR4_DQ21	IO_L15N_T2L_N5_AD11N_64	AT17
PL_DDR4_DQ22	IO_L18P_T2U_N10_AD2P_64	AN13
PL_DDR4_DQ23	IO_L15P_T2L_N4_AD11P_64	AR17
PL_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_64	AU17
PL_DDR4_DQS_P2	IO_L16P_T2U_N6_QBC_AD3P_64	AR14
PL_DDR4_DQS_N2	IO_L16N_T2U_N7_QBC_AD3N_64	AT14
PL_DDR4_DQ24	IO_L24N_T3U_N11_64	AK14
PL_DDR4_DQ25	IO_L21P_T3L_N4_AD8P_64	AM16

PL_DDR4_DQ26	IO_L23P_T3U_N8_64	AK16
PL_DDR4_DQ27	IO_L20P_T3L_N2_AD1P_64	AL14
PL_DDR4_DQ28	IO_L24P_T3U_N10_64	AJ14
PL_DDR4_DQ29	IO_L21N_T3L_N5_AD8N_64	AN15
PL_DDR4_DQ30	IO_L23N_T3U_N9_64	AK15
PL_DDR4_DQ31	IO_L20N_T3L_N3_AD1N_64	AM13
PL_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_64	AN16
PL_DDR4_DQS_P3	IO_L22P_T3U_N6_DBC_AD0P_64	AL15
PL_DDR4_DQS_N3	IO_L22N_T3U_N7_DBC_AD0N_64	AM15
PL_DDR4_DQ32	IO_L6N_T0U_N11_AD6N_66	AW24
PL_DDR4_DQ33	IO_L6P_T0U_N10_AD6P_66	AV24
PL_DDR4_DQ34	IO_L3P_T0L_N4_AD15P_66	BA23
PL_DDR4_DQ35	IO_L2N_T0L_N3_66	BB25
PL_DDR4_DQ36	IO_L5N_T0U_N9_AD14N_66	BA22
PL_DDR4_DQ37	IO_L2P_T0L_N2_66	BA25
PL_DDR4_DQ38	IO_L5P_T0U_N8_AD14P_66	AY22
PL_DDR4_DQ39	IO_L3N_T0L_N5_AD15N_66	BA24
PL_DDR4_DM4	IO_L1P_T0L_N0_DBC_66	BB22
PL_DDR4_DQS_P4	IO_L4P_T0U_N6_DBC_AD7P_66	AY24
PL_DDR4_DQS_N4	IO_L4N_T0U_N7_DBC_AD7N_66	AY25
PL_DDR4_DQ40	IO_L11N_T1U_N9_GC_66	AT24
PL_DDR4_DQ41	IO_L8P_T1L_N2_AD5P_66	AU25
PL_DDR4_DQ42	IO_L9N_T1L_N5_AD12N_66	AU22
PL_DDR4_DQ43	IO_L8N_T1L_N3_AD5N_66	AV25
PL_DDR4_DQ44	IO_L11P_T1U_N8_GC_66	AT23
PL_DDR4_DQ45	IO_L12N_T1U_N11_GC_66	AR26
PL_DDR4_DQ46	IO_L9P_T1L_N4_AD12P_66	AT22
PL_DDR4_DQ47	IO_L12P_T1U_N10_GC_66	AP26
PL_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_66	AU23
PL_DDR4_DQS_P5	IO_L10P_T1U_N6_QBC_AD4P_66	AR25
PL_DDR4_DQS_N5	IO_L10N_T1U_N7_QBC_AD4N_66	AT25
PL_DDR4_DQ48	IO_L17N_T2U_N9_AD10N_66	AM23
PL_DDR4_DQ49	IO_L18P_T2U_N10_AD2P_66	AN24
PL_DDR4_DQ50	IO_L15P_T2L_N4_AD11P_66	AN23
PL_DDR4_DQ51	IO_L14N_T2L_N3_GC_66	AR24
PL_DDR4_DQ52	IO_L17P_T2U_N8_AD10P_66	AL23
PL_DDR4_DQ53	IO_L14P_T2L_N2_GC_66	AP24
PL_DDR4_DQ54	IO_L15N_T2L_N5_AD11N_66	AP23
PL_DDR4_DQ55	IO_L18N_T2U_N11_AD2N_66	AN25
PL_DDR4_DM6	IO_L13P_T2L_N0_GC_QBC_66	AP22
PL_DDR4_DQS_P6	IO_L16P_T2U_N6_QBC_AD3P_66	AM26
PL_DDR4_DQS_N6	IO_L16N_T2U_N7_QBC_AD3N_66	AN26
PL_DDR4_DQ56	IO_L24N_T3U_N11_66	AJ24

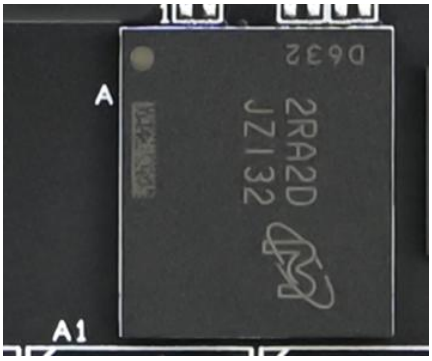
PL_DDR4_DQ57	IO_L20N_T3L_N3_AD1N_66	AM25
PL_DDR4_DQ58	IO_L23N_T3U_N9_66	AK24
PL_DDR4_DQ59	IO_L20P_T3L_N2_AD1P_66	AL24
PL_DDR4_DQ60	IO_L24P_T3U_N10_66	AH24
PL_DDR4_DQ61	IO_L21N_T3L_N5_AD8N_66	AL25
PL_DDR4_DQ62	IO_L23P_T3U_N8_66	AJ23
PL_DDR4_DQ63	IO_L21P_T3L_N4_AD8P_66	AK25
PL_DDR4_DM7	IO_L19P_T3L_N0_DBC_AD9P_66	AJ22
PL_DDR4_DQS_P7	IO_L22P_T3U_N6_DBC_AD0P_66	AJ26
PL_DDR4_DQS_N7	IO_L22N_T3U_N7_DBC_AD0N_66	AK26
PL_DDR4_A0	IO_L16P_T2U_N6_QBC_AD3P_65	AM18
PL_DDR4_A1	IO_L17N_T2U_N9_AD10N_65	AM20
PL_DDR4_A2	IO_L19P_T3L_N0_DBC_AD9P_65	AK19
PL_DDR4_A3	IO_L21P_T3L_N4_AD8P_65	AK21
PL_DDR4_A4	IO_L16N_T2U_N7_QBC_AD3N_65	AN18
PL_DDR4_A5	IO_L21N_T3L_N5_AD8N_65	AK20
PL_DDR4_A6	IO_L19N_T3L_N1_DBC_AD9N_65	AL19
PL_DDR4_A7	IO_L23P_T3U_N8_I2C_SCLK_65	AH21
PL_DDR4_A8	IO_L18P_T2U_N10_AD2P_65	AL18
PL_DDR4_A9	IO_L10P_T1U_N6_QBC_AD4P_65	AT20
PL_DDR4_A10	IO_L15P_T2L_N4_AD11P_65	AN19
PL_DDR4_A11	IO_L20N_T3L_N3_AD1N_65	AK17
PL_DDR4_A12	IO_L17P_T2U_N8_AD10P_65	AM21
PL_DDR4_A13	IO_L6P_T0U_N10_AD6P_65	AV19
PL_DDR4_A14	IO_L15N_T2L_N5_AD11N_65	AP19
PL_DDR4_A15	IO_L22P_T3U_N6_DBC_AD0P_65	AH18
PL_DDR4_A16	IO_L22N_T3U_N7_DBC_AD0N_65	AJ18
PL_DDR4_A17	IO_L8N_T1L_N3_AD5N_65	AU18
PL_DDR4_BA0	IO_L10N_T1U_N7_QBC_AD4N_65	AT19
PL_DDR4_BA1	IO_L7N_T1L_N1_QBC_AD13N_65	AY21
PL_DDR4_BG0	IO_L20P_T3L_N2_AD1P_65	AJ17
PL_DDR4_NCS	IO_L9P_T1L_N4_AD12P_65	AU21
PL_DDR4_ODT	IO_L7P_T1L_N0_QBC_AD13P_65	AW21
PL_DDR4_NRESET	IO_L18N_T2U_N11_AD2N_65	AL17
PL_DDR4_CLK_P	IO_L14P_T2L_N2_GC_65	AP18
PL_DDR4_CLK_N	IO_L14N_T2L_N3_GC_65	AP17
PL_DDR4_CKE	IO_L5P_T0U_N8_AD14P_65	AY20
PL_DDR4_NACT	IO_L9N_T1L_N5_AD12N_65	AU20
PL_DDR4_NALERT	IO_L5N_T0U_N9_AD14N_65	BA20
PL_DDR4_PARITY	IO_L8P_T1L_N2_AD5P_65	AT18



Part 3.9: EMMC

The core board is designed with a 32GB EMMC on the ARM side. The operating temperature of EMMC is from -40℃ to +85℃, the following is the pin assignment of EMMC. For more detailed information, please refer to the schematic provided.

EMMC Pin	Pin Name	Pin Position
EMMC_DATA0	MIO13	AU26
EMMC_DATA1	MIO14	AU27
EMMC_DATA2	MIO15	AT27
EMMC_DATA3	MIO16	AU28
EMMC_DATA4	MIO17	AT28
EMMC_DATA5	MIO18	AP28
EMMC_DATA6	MIO19	AR27
EMMC_DATA7	MIO20	AP27
EMMC_CLK	MIO22	AL27
EMMC_CMD	MIO21	AN28
EMMC_nRST	MIO23	AM27



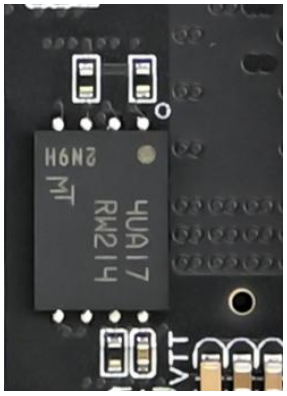
Part 3.10: QSPI FLASH

The SOM core board is designed with two QSPI FLASHs, with a single capacity of 512Mb and two pieces totally 1GB, which can be defined by the user as QSPI x 8 to accelerate the startup and reduce the startup time. the QSPI FLASHs can be used to store the startup file and the user file.

QSPI0 FLASH Pin	Pin Name	Pin Position

QSPI0_D0	MIO4	BA28
QSPI0_D1	MIO1	BA27
QSPI0_D2	MIO2	BB26
QSPI0_D3	MIO3	BB28
QSPI0_CS	MIO5	BA29
QSPI0_CLK	MIO0	BB27

QSPI1 FLASH Pin	Pin Name	Pin Position
QSPI1_D0	MIO8	AW27
QSPI1_D1	MIO9	AW26
QSPI1_D2	MIO10	AV26
QSPI1_D3	MIO11	AW28
QSPI1_CS	MIO7	AY27
QSPI1_CLK	MIO12	AV28



Part 3.11: Core Board Signal and Equal Length

The signals leading out of the core board to the connectors are strictly equalized, refer to the excel of “CRZU49DRC Core Board Pins and Equal Length”, which detailed list of signal names and signal alignment lengths.

Part 3.12: Core Board Package Library

In order to facilitate the user to quickly use the core board, we provide the corresponding package library, the relative position of the connector and the core board frame silkscreen have been placed, you can directly call to use it. The schematic package provides two versions of **AD/ORCAD**, and the PCB package provides two versions of **AD/Allegro**, which are stored in the corresponding folder.

Part 3.13: Core Board Connectors

The core board is connected to the carrier board via four 0.635mm/240P gold-plated high-speed connectors on the bottom. The connector model used on the carrier board is **ADM6-60-01.5-L-4-2-A-TR.**

Part 4: Carrier Board Introduction

In this section, will describe in detail all the interface resources on the carrier board.

Part 4.1: Power Supply

The board provides two power supply modes, adapter power supply or ATX power supply, the choice of the two power supply modes depends on the user's convenience, the power supply part of the detailed circuitry can be referred to the corresponding schematic diagram of the FPGA development board.

Part 4.2: System Clock

The clock circuit is mainly on the core board, you can refer to the core board clock section for reference

Part 4.3: System Reset

One Reset key is reserved on the FPGA carrier board and the user can select the button according to convenience. After the key, a reset chip is placed on the SOM core board, the model is MAX811TEUS

Reset pins are connected to the PS and PL side of the chip, PS side connected to BANK0, the corresponding pin is PS_POR_B, pin position is U32, PL side BANK65 IO_L2P_65 (BA18) pin, pin level is 1.2 V. Reset part of the detailed circuit can be referred to the carrier board schematic.

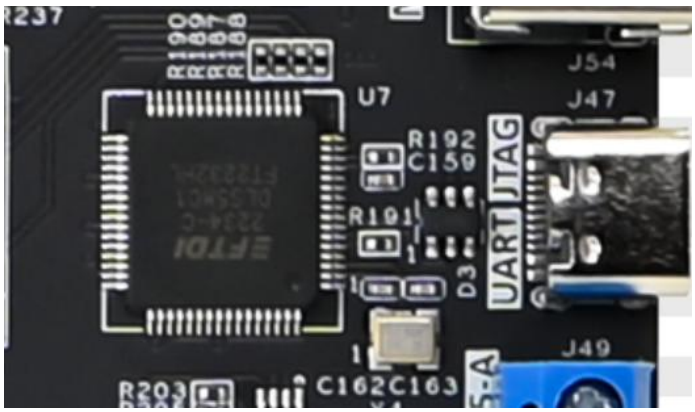
Part 4.4: USB to UART

The FPGA carrier board uses "**Silicon Labs CP2102GM**" chip to realize USB to UART, and the USB interface adopts "**Micro USB**". Users only need to use a Micro USB cable to connect to the PC for serial communication.

The "**TX/RX**" signal of the UART is connected with the "**BANK501**" of the "**RFSOC**", and the interface level is 1.8V, so the serial port interface adopts the level conversion to 3.3V and connects with the serial port chip.

The following is the signal correspondence table and schematic, the TX/RX direction is defined for the RFSOC side.

UART0 Pin	Pin Name	Pin Position
UART0_TX	MIO_43	G31
UART0_RX	MIO_42	H31



Part 4.5: SD Card Slot Interface

The SD card holder is placed on the carrier board (On the bottom of the board), It can be used for SD card startup, and is also convenient for user debugging or file storage. The circuit interface level is 1.8V, the SD card signal is connected to the RFSOC BANK501. TF card level is 3.3V, through the special level conversion chip to achieve the SD card signal 1.8V to 3.3V. The following is the pin assignment and schematic diagram of SD card interface, details refer to the schematic.

SD Card Slot	Pin Name	Pin Position
SD-CLK	MIO51	M31
SD-CMD	MIO50	M30
SD-CD	MIO45	L30
SD-DATA0	MIO46	J31
SD-DATA1	MIO47	L32
SD-DATA2	MIO48	M32
SD-DATA3	MIO49	K31

Part 4.6: RS485 Interface

The development board uses the SP3485EN chip to achieve RS485 communication, the TX/RX signal of RS485 is connected to the BANK501 of MPSOC, and the interface level is 1.8V, so the interface is connected to the RS485 chip using a level conversion to 3.3V.

The following is the signal correspondence table and schematic diagram, TX/RX direction is defined by RFSOC side.

RS485 Pin	Pin Name	Pin Position
RS485_TX	MIO40	F32
RS485_RX	MIO41	K32

Part 4.7: CAN Interface

The carrier board uses the **SN65HVD230D** chip to achieve **CAN** communication, the **CAN TX/RX** signals are connected to the **MPSOC BANK501**, the interface level is **1.8V**, so the signal interface is connected to the CAN chip using a level conversion to **3.3V**.

The following is the signal correspondence table, **TX/RX** direction is defined for **RFSOC** end, detailed circuitry refer to the carrier board schematic.

CAN Pin	Pin Name	Pin Position
CAN_TX	MIO39	J32
CAN_RX	MIO38	G32

Part 4.8: E2PROM

The **64Kbit EEPROM** chip is placed on the FPGA carrier board, the model is AT24C64D-SSHM-T Connect with **BANK84** of **FPGA** through **IIC** bus. The **EEPROM** read address is **0xA1**, and the write address is **0xA0**. The following is the pin assignment of the **EEPROM**, the detailed circuit can refer to the schematic diagram of the development board.

E2PROM Pin	Pin Name	Pin Position
IIC-CLK	IO-12P-84	AP11
IIC-DATA	IO-12N-84	AP10

Part 4.9: MIPI Interface

Two MIPI interfaces are designed on the FPGA carrier board. The interface signals are connected to the BANK84/BANK505 of the FPGA, please refer to the schematic for details.

Mini DP Pin	Pin Name	Pin Position
DP_LINE_P0	MGT_505_TX_P3	AE37
DP_LINE_N0	MGT_505_TX_N3	AE38
DP_HPD	IO_L7P_HDGC_84	AU10
DP_AUX_OUT	IO_L7N_HDGC_84	AV10
DP_OE	IO_L1P_84	BB11
DP_AUX_IN	IO_L1N_84	BB10
DP_CLK_P_27M	MGT_505_CLK_P3	AB34
DP_CLK_N_27M	MGT_505_CLK_N3	AB35

Part 4.10: USB3.0 Interface

Four **USB3.0** main interfaces are placed on the FPGA Carrier board, and the main interfaces are compatible with USB2.0/3.0. The interface signals are connected to the BANK501/BANK505 of the FPGA, details refer to the schematic. The USB2.0 is realized by connecting the PHY chip USB3320C-EZK to the MIO.USB3.0 is extended by HUB chip GL3523-OTY30.

The following is the pin assignment of USB2.0/USB3.0, please refer to the schematic of the development board for detailed circuit.

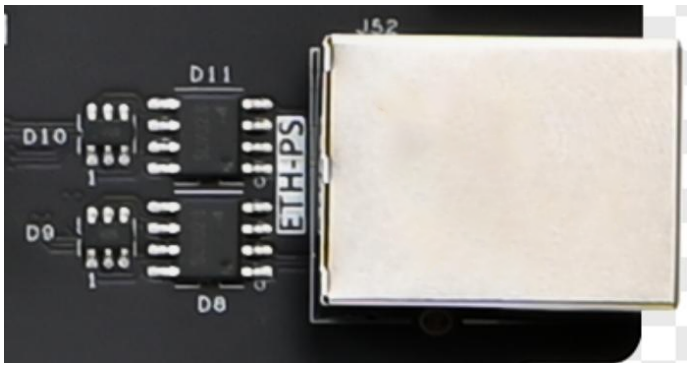
USB Pin	Pin Name	Pin Position
USBPHY_DATA0	MIO56	N29
USBPHY_DATA1	MIO57	R29
USBPHY_DATA2	MIO54	N28
USBPHY_DATA3	MIO59	T30
USBPHY_DATA4	MIO60	U28
USBPHY_DATA5	MIO61	T28
USBPHY_DATA6	MIO62	V28
USBPHY_DATA7	MIO63	T29
USBPHY_STP	MIO58	R30
USBPHY_NXT	MIO55	P29
USBPHY_DIR	MIO53	N30
USBPHY_CLKOUT	MIO52	P28
USBPHY_RESET	MIO44	K30
GT1_USB3_SSTXP	MGT_505_TX_P2	AF39

GT1_USB3_SSTXN	MGT_505_TX_N2	AF40
GT1_USB3_SSRXP	MGT_505_RX_P2	AG41
GT1_USB3_SSRXN	MGT_505_RX_N2	AG42
USB3_CLK_P_26M	MGT_505_CLK_P2	AC36
USB3_CLK_N_26M	MGT_505_CLK_N2	AC37

Part 4.11: Gigabit Ethernet

The FPGA carrier board are designed with one way Gigabit Ethernet. The PHY chip has been integrated on the SOM core board and the signal is connected to the PS side. The Ethernet chip and **FPGA** are interconnected through the **RGMII** interface. Connect the corresponding pins as shown in the table below, the address of the PS Side network port is **PHY_AD[2:0]=001**, you can refer to the schematic for the detailed circuit.

RMGII Signal	Pin Name	Pin Position
GTX_CLK	MIO26_501	A34
TXD0	MIO27_501	B34
TXD1	MIO28_501	A33
TXD2	MIO29_501	B33
TXD3	MIO30_501	C34
TX_EN	MIO31_501	D33
RX_CLK	MIO32_501	D34
RXD0	MIO33_501	D32
RXD1	MIO34_501	D31
RXD2	MIO35_501	C33
RXD3	MIO36_501	E31
RX_DV	MIO37_501	E32
MDC	MIO76_502	AB30
MDIO	MIO77_502	AA30



Part 4.12: QSFP28 Interface

Two 10G SFP interfaces are designed on the FPGA carrier board. The interface signals are connected to the BANK48/BANK128 of the RFSOC. For details, please refer to the schematic.

The following is the pin assignment of **QSFP**, the detailed circuit can refer to the schematic of the FPGA development board.

QSFP1 Pin	Pin Name	Pin Position	QSFP2 Pin	Pin Name	Pin Position
QSFP1-TX-P0	MGT_TX_P0_129	P38	QSFP2-TX-P0	MGT_TX_P0_128	V38
QSFP1-TX-N0	MGT_TX_N0_129	P39	QSFP2-TX-N0	MGT_TX_N0_128	V39
QSFP1-TX-P1	MGT_TX_P1_129	N36	QSFP2-TX-P1	MGT_TX_P1_128	U36
QSFP1-TX-N1	MGT_TX_N1_129	N37	QSFP2-TX-N1	MGT_TX_N1_128	U37
QSFP1-TX-P2	MGT_TX_P2_129	M38	QSFP2-TX-P2	MGT_TX_P2_128	T38
QSFP1-TX-N2	MGT_TX_N2_129	M39	QSFP2-TX-N2	MGT_TX_N2_128	T39
QSFP1-TX-P3	MGT_TX_P3_129	L36	QSFP2-TX-P3	MGT_TX_P3_128	R36
QSFP1-TX-N3	MGT_TX_N3_129	L37	QSFP2-TX-N3	MGT_TX_N3_128	R37
QSFP1-RX-P0	MGT_RX_P0_129	W41	QSFP2-RX-P0	MGT_RX_P0_128	AC41
QSFP1-RX-N0	MGT_RX_N0_129	W42	QSFP2-RX-N0	MGT_RX_N0_128	AC42
QSFP1-RX-P1	MGT_RX_P1_129	U41	QSFP2-RX-P1	MGT_RX_P1_128	AB39
QSFP1-RX-N1	MGT_RX_N1_129	U42	QSFP2-RX-N1	MGT_RX_N1_128	AB40
QSFP1-RX-P2	MGT_RX_P2_129	R41	QSFP2-RX-P2	MGT_RX_P2_128	AA41
QSFP1-RX-N2	MGT_RX_N2_129	R42	QSFP2-RX-N2	MGT_RX_N2_128	AA42
QSFP1-RX-P3	MGT_RX_P3_129	N41	QSFP2-RX-P3	MGT_RX_P3_128	Y39
QSFP1-RX-N3	MGT_RX_N3_129	N42	QSFP2-RX-N3	MGT_RX_N3_128	Y40
QSFP1_LPMODE	IO_3P_84	AY9	QSFP2_LPMODE	IO_4N_84	AY10
QSFP1_I2C_SCL	IO_3N_84	BA9	QSFP2_I2C_SCL	IO_2P_84	BA10
QSFP1_I2C_SDA	IO_4P_84	AY11	QSFP2_I2C_SDA	IO_2N_84	BB9

Part 4.13: SSD Interface

The PS side of the FPGA development board is designed with a SSD (x1 mode), the interface type is M.2, and the protocol is NVME. The pin locations of the SSD interface are listed in the table below, and you can refer to the schematic diagram of the development board for detailed circuitry.

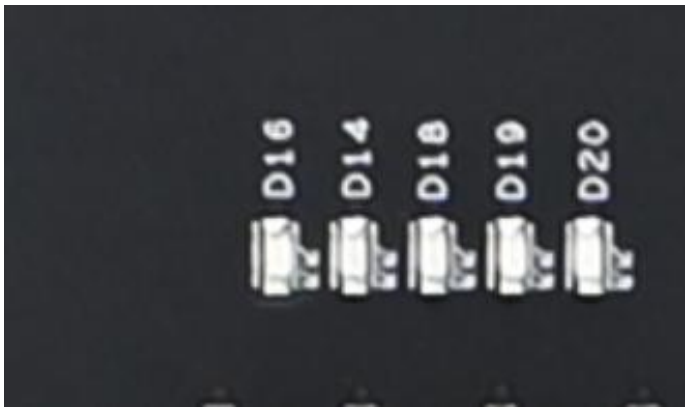
SSD Interface	Pin Name	Pin Position
SSD_nRST	MIO65	V30
REFCLK_P_100M	MGT_505_CLK_P0	AF34
REFCLK_N_100M	MGT_505_CLK_N0	AF35
GT0_SSD_TX_P0	MGT_505_TX_P0	AH35
GT0_SSD_TX_N0	MGT_505_TX_N0	AH36
GT0_SSD_TX_P1	MGT_505_TX_P1	AG37
GT0_SSD_TX_N1	MGT_505_TX_N1	AG38
GT0_SSD_RX_P0	MGT_505_RX_P0	AJ41
GT0_SSD_RX_N0	MGT_505_RX_N0	AJ42
GT0_SSD_RX_P1	MGT_505_RX_P1	AH39
GT0_SSD_RX_N1	MGT_505_RX_N1	AH40

Part 4.14: LED

Four LEDs are designed on the FPGA carrier board. The light is on when the LED is high and off when it is low. The pin definitions are listed in the table below, and you can refer to the schematic.

LED Bits	Pin Name	Pin Position

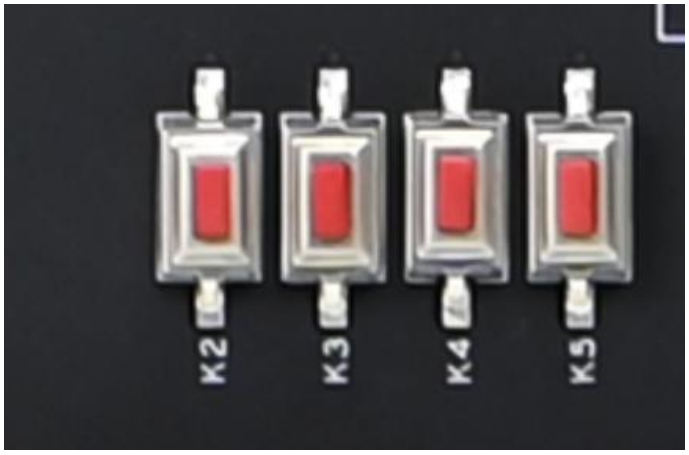
LED1	IO-9P-84	AR12
LED2	IO-9N-84	AT12
LED3	IO-10P-84	AR10
LED4	IO-10N-84	AT10



Part 4.15: KEY

The FPGA development board is designed with four KEYs. The KEY defaults to a high level, and the KEY is pressed to a low level. The KEY is connected to the PL side. The pin positions of the KEYs are as follows.

KEY Bits	Pin Name	Pin Position
KEY1	IO-L8P-84	AU12
KEY2	IO-L8N-84	AU11
KEY3	IO-L6P-84	AV9
KEY4	IO-L6N-84	AW9



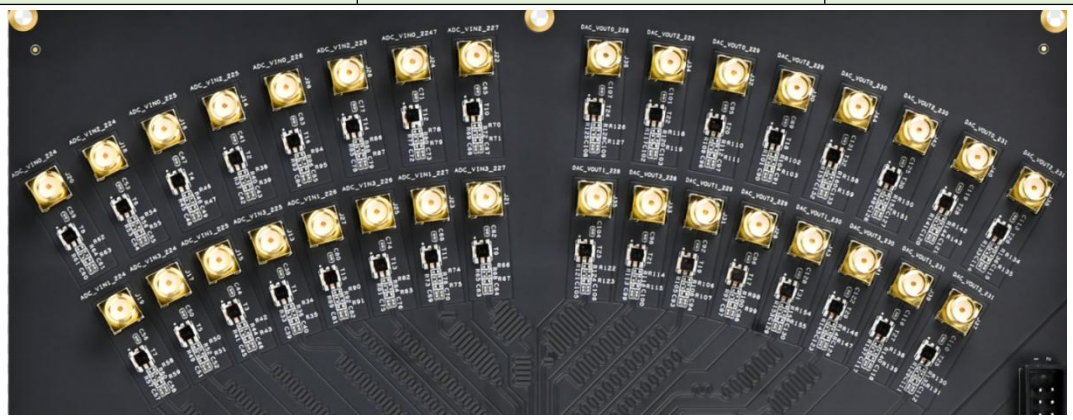
Part 4.16: RF Input and Output

Development board supports 16-way 14-bit ADC 2.5GSPS input, 16-way 14-bit DAC 9.85 GSPS

output, RF connector is a standard SMA RF header, single-ended signal input and output, through the Barron device for differential single-ended interconversion function, complete the data transmission and reception, and the VCM signal is also led to the measurement point, so that users can easily adjust the common mode voltage.

ADC&DAC	Pin Name	Pin Position
ADC224_T0_CH0_P	ADC_VIN0_P_224	AU5
ADC224_T0_CH0_N	ADC_VIN0_N_224	AU4
ADC224_T0_CH1_P	ADC_VIN1_P_224	AU2
ADC224_T0_CH1_N	ADC_VIN1_N_224	AU1
ADC224_T0_CH2_P	ADC_VIN2_P_224	AR5
ADC224_T0_CH2_N	ADC_VIN2_N_224	AR4
ADC224_T0_CH3_P	ADC_VIN3_P_224	AR2
ADC224_T0_CH3_N	ADC_VIN3_N_224	AR1
ADC225_T1_CH0_P	ADC_VIN0_P_225	AN5
ADC225_T1_CH0_N	ADC_VIN0_N_225	AN4
ADC225_T1_CH1_P	ADC_VIN1_P_225	AN2
ADC225_T1_CH1_N	ADC_VIN1_N_225	AN1
ADC225_T1_CH2_P	ADC_VIN2_P_225	AL5
ADC225_T1_CH2_N	ADC_VIN2_N_225	AL4
ADC225_T1_CH3_P	ADC_VIN3_P_225	AL2
ADC225_T1_CH3_N	ADC_VIN3_N_225	AL1
ADC226_T2_CH0_P	ADC_VIN0_P_226	AJ5
ADC226_T2_CH0_N	ADC_VIN0_N_226	AJ4
ADC226_T2_CH1_P	ADC_VIN1_P_226	AJ2
ADC226_T2_CH1_N	ADC_VIN1_N_226	AJ1
ADC226_T2_CH2_P	ADC_VIN2_P_226	AG5
ADC226_T2_CH2_N	ADC_VIN2_N_226	AG4
ADC226_T2_CH3_P	ADC_VIN3_P_226	AG2
ADC226_T2_CH3_N	ADC_VIN3_N_226	AG1
ADC227_T3_CH0_P	ADC_VIN0_P_227	AE5
ADC227_T3_CH0_N	ADC_VIN0_N_227	AE4
ADC227_T3_CH1_P	ADC_VIN1_P_227	AE2
ADC227_T3_CH1_N	ADC_VIN1_N_227	AE1
ADC227_T3_CH2_P	ADC_VIN2_P_227	AC5
ADC227_T3_CH2_N	ADC_VIN2_N_227	AC4
ADC227_T3_CH3_P	ADC_VIN3_P_227	AC2
ADC227_T3_CH3_N	ADC_VIN3_N_227	AC1
DAC228_T0_CH0_P	DAC_VOUT0_P_228	Y5
DAC228_T0_CH0_N	DAC_VOUT0_N_228	Y4
DAC228_T0_CH1_P	DAC_VOUT1_P_228	Y2
DAC228_T0_CH1_N	DAC_VOUT1_N_228	Y1
DAC228_T0_CH2_P	DAC_VOUT2_P_228	V5

DAC228_T0_CH2_N	DAC_VOUT2_N_228	V4
DAC228_T0_CH3_P	DAC_VOUT3_P_228	V2
DAC228_T0_CH3_N	DAC_VOUT3_N_228	V1
DAC229_T1_CH0_P	DAC_VOUT0_P_229	T5
DAC229_T1_CH0_N	DAC_VOUT0_N_229	T4
DAC229_T1_CH1_P	DAC_VOUT1_P_229	T2
DAC229_T1_CH1_N	DAC_VOUT1_N_229	T1
DAC229_T1_CH2_P	DAC_VOUT2_P_229	P5
DAC229_T1_CH2_N	DAC_VOUT2_N_229	P4
DAC229_T1_CH3_P	DAC_VOUT3_P_229	P2
DAC229_T1_CH3_N	DAC_VOUT3_N_229	P1
DAC230_T2_CH0_P	DAC_VOUT0_P_230	M5
DAC230_T2_CH0_N	DAC_VOUT0_N_230	M4
DAC230_T2_CH1_P	DAC_VOUT1_P_230	M2
DAC230_T2_CH1_N	DAC_VOUT1_N_230	M1
DAC230_T2_CH2_P	DAC_VOUT2_P_230	K5
DAC230_T2_CH2_N	DAC_VOUT2_N_230	K4
DAC230_T2_CH3_P	DAC_VOUT3_P_230	K2
DAC230_T2_CH3_N	DAC_VOUT3_N_230	K1
DAC231_T3_CH0_P	DAC_VOUT0_P_231	H5
DAC231_T3_CH0_N	DAC_VOUT0_N_231	H4
DAC231_T3_CH1_P	DAC_VOUT1_P_231	H2
DAC231_T3_CH1_N	DAC_VOUT1_N_231	H1
DAC231_T3_CH2_P	DAC_VOUT2_P_231	F5
DAC231_T3_CH2_N	DAC_VOUT2_N_231	F4
DAC231_T3_CH3_P	DAC_VOUT3_P_231	F2
DAC231_T3_CH3_N	DAC_VOUT3_N_231	F1



Part 4.17: 40P 2.54mm Expansion Port

One 40P 2.54mm pitch simple horn socket is designed on the FPGA development board , which are used to expand the signal connection. The signals are connected to the FPGA's BANK88/89 at a

level of 3.3V. The following table indicates the chip position where the signal is located. For the detailed connection relationship, please refer to the schematic diagram.

JM1 Signal Sequence	Pin Name	Pin Position	JM1 Signal Sequence	Pin Name	Pin Position
5	IO_L2P_88	N15	6	IO_L3P_88	N14
7	IO_L2N_88	M15	8	IO_L3N_88	M14
9	IO_L8P_HDGC_88	J16	10	IO_L9P_88	J14
11	IO_L8N_HDGC_88	H16	12	IO_L9N_88	J13
13	IO_L2P_89	J12	14	IO_L3P_89	H10
15	IO_L2N_89	J11	16	IO_L3N_89	H9
17	IO_L7P_HDGC_89	E10	18	IO_L1P_89	K12
19	IO_L7N_HDGC_89	E9	20	IO_L1N_89	K11
21	IO_L5P_HDGC_89	G12	22	IO_L4P_89	H11
23	IO_L5N_HDGC_89	G11	24	IO_L4N_89	G10
25	IO_L11P_89	C10	26	IO_L6P_HDGC_89	F10
27	IO_L11N_89	B10	28	IO_L6N_HDGC_89	F9
29	IO_L12P_89	A10	30	IO_L10P_89	C11
31	IO_L12N_89	A9	32	IO_L10N_89	B11
37	IO_L8P_89	E11	38	IO_L9P_89	D9
39	IO_L8N_89	D11	40	IO_L9N_89	C9

Part 4.18: FMC Expansion Port

One **FMC HPC** connector is designed on the FPGA carrier board, However, due to the limited number of pins on the chip, not all of them are actually connected, only 4 pairs of MGT and LA signals are connected, and the following table lists the signal correspondences.Refer to the schematic for details

Number	FMC HPC Pin	Pin Name	Pin Position
A2	DP1_M2C_P	MGT_RX_P1_130	J41
A3	DP1_M2C_N	MGT_RX_N1_130	J42
A6	DP2_M2C_P	MGT_RX_P2_130	G41
A7	DP2_M2C_N	MGT_RX_N2_130	G42
A10	DP3_M2C_P	MGT_RX_P3_130	F39
A11	DP3_M2C_N	MGT_RX_N3_130	F40
A14	DP4_M2C_P	MGT_RX_P0_131	E41
A15	DP4_M2C_N	MGT_RX_N0_131	E42
A18	DP5_M2C_P	MGT_RX_P1_131	D39
A19	DP5_M2C_N	MGT_RX_N1_131	D40
A22	DP1_C2M_P	MGT_TX_P1_130	J36
A23	DP1_C2M_N	MGT_TX_N1_130	J37

A26	DP2_C2M_P	MGT_TX_P2_130	H38
A27	DP2_C2M_N	MGT_TX_N2_130	H39
A30	DP3_C2M_P	MGT_TX_P3_130	G36
A31	DP3_C2M_N	MGT_TX_N3_130	G37
A34	DP4_C2M_P	MGT_TX_P0_131	F34
A35	DP4_C2M_N	MGT_TX_N0_131	F35
A38	DP5_C2M_P	MGT_TX_P1_131	E36
A39	DP5_C2M_N	MGT_TX_N1_131	E37
B12	DP7_M2C_P	MGT_RX_P3_131	B39
B13	DP7_M2C_N	MGT_RX_N3_131	B40
B16	DP6_M2C_P	MGT_RX_P2_131	C41
B17	DP6_M2C_N	MGT_RX_N2_131	C42
B20	GBTCLK1_M2C_P	MGT_CLK0_P_131	K34
B21	GBTCLK1_M2C_N	MGT_CLK0_N_131	K35
B32	DP7_C2M_P	MGT_TX_P3_131	A36
B33	DP7_C2M_N	MGT_TX_N3_131	A37
B36	DP6_C2M_P	MGT_TX_P2_131	C36
B37	DP6_C2M_N	MGT_TX_N2_131	C37
C2	DP0_C2M_P	MGT_TX_P0_130	K38
C3	DP0_C2M_N	MGT_TX_N0_130	K39
C6	DP0_M2C_P	MGT_RX_P0_130	L41
C7	DP0_M2C_N	MGT_RX_N0_130	L42
C10	LA06_P	IO_L22P_67	B28
C11	LA06_N	IO_L22N_67	A28
C14	LA10_P	IO_L2P_67	R25
C15	LA10_N	IO_L2N_67	R26
C18	LA14_P	IO_L7P_67	L28
C19	LA14_N	IO_L7N_67	L29
C22	LA18_P_CC	IO_L13P_MRCC_6	F30
C23	LA18_N_CC	IO_L13N_MRCC_6	E30
C26	LA27_P	IO_L5P_68	N23
C27	LA27_N	IO_L5N_68	N24
C30	SCL	IO_L11P_88	H15
C31	SDA	IO_L11N_88	H14
D4	GBTCLK0_M2C_P	MGT_CLK0_P_130	P34
D5	GBTCLK0_M2C_N	MGT_CLK0_N_130	P35
D8	LA01_P_CC	IO_L11P_SRCC_67	H30
D9	LA01_N_CC	IO_L11N_SRCC_67	G30
D11	LA05_P	IO_L20P_67	B27
D12	LA05_N	IO_L20N_67	A27
D14	LA09_P	IO_L19P_67	C30
D15	LA09_N	IO_L19N_67	C31
D17	LA13_P	IO_L10P_67	J27
D18	LA13_N	IO_L10N_67	J28
D20	LA17_P_CC	IO_L14P_SRCC_67	G27
D21	LA17_N_CC	IO_L14N_SRCC_67	G28
D23	LA23_P	IO_L21P_67	B30
D24	LA23_N	IO_L21N_67	B31

D26	LA26_P	IO_L10P_68	H23
D27	LA26_N	IO_L10N_68	G23
E2	HA01_P_CC	IO_L14P_SRCC_68	F23
E3	HA01_N_CC	IO_L14N_SRCC_68	F24
E6	HA05_P	IO_L2P_68	R22
E7	HA05_N	IO_L2N_68	P23
E9	HA09_P	IO_L8P_68	K22
E10	HA09_N	IO_L8N_68	J22
E12	HA13_P	IO_L1P_69	R20
E13	HA13_N	IO_L1N_69	R19
E15	HA16_P	IO_L12P_MRCC_6	G22
E16	HA16_N	IO_L12N_MRCC_6	F22
E18	HA20_P	IO_L16P_68	E22
E19	HA20_N	IO_L16N_68	D22
E21	HB03_P	IO_L2P_69	R17
E22	HB03_N	IO_L2N_69	P17
E24	HB05_P	IO_L16P_69	E17
E25	HB05_N	IO_L16N_69	D17
E27	HB09_P	IO_L4P_87	B13
E28	HB09_N	IO_L4N_87	B12
E30	HB13_P	IO_L8P_69	J18
E31	HB13_N	IO_L8N_69	J17
E33	HB19_P	IO_L10P_87	D16
E34	HB19_N	IO_L10N_87	C16
E36	HB21_P	IO_L2P_87	D13
E37	HB21_N	IO_L2N_87	D12
F4	HA00_P_CC	IO_L11P_SRCC_68	H24
F5	HA00_N_CC	IO_L11N_SRCC_68	H25
F7	HA04_P	IO_L4P_68	R24
F8	HA04_N	IO_L4N_68	P24
F10	HA08_P	IO_L3P_68	N21
F11	HA08_N	IO_L3N_68	M21
F13	HA12_P	IO_L22P_68	B22
F14	HA12_N	IO_L22N_68	B23
F16	HA15_P	IO_L20P_68	D24
F17	HA15_N	IO_L20N_68	C24
F19	HA19_P	IO_L7P_69	K21
F20	HA19_N	IO_L7N_69	K20
F22	HB02_P	IO_L22P_69	B17
F23	HB02_N	IO_L22N_69	A17
F25	HB04_P	IO_L6P_69	M18
F26	HB04_N	IO_L6N_69	L18
F28	HB08_P	IO_L10P_69	H18
F29	HB08_N	IO_L10N_69	G18
F31	HB12_P	IO_L15P_69	G21
F32	HB12_N	IO_L15N_69	F20
F34	HB16_P	IO_L9P_87	E16
F35	HB16_N	IO_L9N_87	E15

F37	HB20_P	IO_L6P_HDGC_87	F15
F38	HB20_N	IO_L6N_HDGC_87	E14
J2	CLK3_M2C_P	IO_L8P_HDGC_87	B16
J3	CLK3_M2C_N	IO_L8N_HDGC_87	B15
J6	HA03_P	IO_L6P_68	M22
J7	HA03_N	IO_L6N_68	M23
J9	HA07_P	IO_L18P_68	D23
J10	HA07_N	IO_L18N_68	C23
J12	HA11_P	IO_L21P_69	B21
J13	HA11_N	IO_L21N_69	B20
J15	HA14_P	IO_L19P_69	D21
J16	HA14_N	IO_L19N_69	C21
J18	HA18_P	IO_L18P_69	D19
J19	HA18_N	IO_L18N_69	D18
J21	HA22_P	IO_L20P_69	C19
J22	HA22_N	IO_L20N_69	C18
J24	HB01_P	IO_L5P_69	M20
J25	HB01_N	IO_L5N_69	L20
J27	HB07_P	IO_L11P_87	A15
J28	HB07_N	IO_L11N_87	A14
J30	HB11_P	IO_L17P_69	E21
J31	HB11_N	IO_L17N_69	E20
J33	HB15_P	IO_L7P_HDGC_87	C15
J34	HB15_N	IO_L7N_HDGC_87	C14
J36	HB18_P	IO_L1P_87	F12
J37	HB18_N	IO_L1N_87	E12
K4	CLK2_M2C_P	IO_L3P_87	D14
K5	CLK2_M2C_N	IO_L3N_87	C13
K7	HA02_P	IO_L1P_68	R21
K8	HA02_N	IO_L1N_68	P21
K10	HA06_P	IO_L4P_69	P19
K11	HA06_N	IO_L4N_69	N18
K13	HA10_P	IO_L23P_69	A20
K14	HA10_N	IO_L23N_69	A19
K16	HA17_P_CC	IO_L13P_MRCC_6	H26
K17	HA17_N_CC	IO_L13N_MRCC_6	G26
K19	HA21_P	IO_L9P_69	J19
K20	HA21_N	IO_L9N_69	H19
K22	HA23_P	IO_L24P_69	B18
K23	HA23_N	IO_L24N_69	A18
K25	HB00_P_CC	IO_L11P_SRCC_69	J21
K26	HB00_N_CC	IO_L11N_SRCC_69	H21
K28	HB06_P_CC	IO_L12P_MRCC_6	G17
K29	HB06_N_CC	IO_L12N_MRCC_6	F17
K31	HB10_P	IO_L3P_69	N20
K32	HB10_N	IO_L3N_69	N19
K34	HB14_P	IO_L12P_87	F14
K35	HB14_N	IO_L12N_87	F13

K37	HB17_P_CC	IO_L14P_SRCC_69	F19
K38	HB17_N_CC	IO_L14N_SRCC_69	F18
G2	CLK1_M2C_P	IO_L13P_MRCC_6	H20
G3	CLK1_M2C_N	IO_L13N_MRCC_6	G20
G6	LA00_P_CC	IO_L12P_MRCC_6	H28
G7	LA00_N_CC	IO_L12N_MRCC_6	H29
G9	LA03_P	IO_L8P_67	K26
G10	LA03_N	IO_L8N_67	J26
G12	LA08_P	IO_L16P_67	F27
G13	LA08_N	IO_L16N_67	F28
G15	LA12_P	IO_L17P_67	D29
G16	LA12_N	IO_L17N_67	C29
G18	LA16_P	IO_L15P_67	F29
G19	LA16_N	IO_L15N_67	E29
G21	LA20_P	IO_L5P_67	M27
G22	LA20_N	IO_L5N_67	M28
G24	LA22_P	IO_L1P_67	R27
G25	LA22_N	IO_L1N_67	P27
G27	LA25_P	IO_L17P_68	E26
G28	LA25_N	IO_L17N_68	D26
G30	LA29_P	IO_L23P_68	A24
G31	LA29_N	IO_L23N_68	A25
G33	LA31_P	IO_L9P_68	K24
G34	LA31_N	IO_L9N_68	J24
G36	LA33_P	IO_L24P_68	A22
G37	LA33_N	IO_L24N_68	A23
H4	CLK0_M2C_P	IO_L5P_HDGC_87	A13
H5	CLK0_M2C_N	IO_L5N_HDGC_87	A12
H7	LA02_P	IO_L4P_67	N25
H8	LA02_N	IO_L4N_67	M25
H10	LA04_P	IO_L18P_67	E27
H11	LA04_N	IO_L18N_67	D27
H13	LA07_P	IO_L6P_67	L25
H14	LA07_N	IO_L6N_67	K25
H16	LA11_P	IO_L9P_67	K29
H17	LA11_N	IO_L9N_67	J29
H19	LA15_P	IO_L23P_67	B32
H20	LA15_N	IO_L23N_67	A32
H22	LA19_P	IO_L3P_67	N26
H23	LA19_N	IO_L3N_67	M26
H25	LA21_P	IO_L24P_67	A29
H26	LA21_N	IO_L24N_67	A30
H28	LA24_P	IO_L19P_68	C26
H29	LA24_N	IO_L19N_68	B26
H31	LA28_P	IO_L15P_68	G25
H32	LA28_N	IO_L15N_68	F25
H34	LA30_P	IO_L21P_68	C25
H35	LA30_N	IO_L21N_68	B25

H37	LA32_P	IO_L7P_68	L23
H38	LA32_N	IO_L7N_68	L24

Part 4.19: USB to JTAG Programmer

USB to **JTAG** Programmer onboard is designed on the FPGA carrier board. After installing the **Vivado** software, use a **USB** cable to connect the USB port corresponding to JTAG. You can realize debugging and downloading, which is very convenient. The following is the location of the interface on the FPGA development board.