

QSFP28- 100GBASE-SR4 Transceiver

Compliance with the 100GBASE-SR4 of the IEEE 802.3bm standard.
850nm Links of up to 70/100m reach via OM3/OM4 fiber



Description

APAC QSFP28 100GBASE-SR4 Transceiver product is a new high speed module with a MPO connector. This interconnecting module offers 4 channels and maximum bandwidth of 100Gbps. The TRxs utilize multimode fiber with 850-nm VCSELs and PIN PDs. This module provides high performance and excellent efficiency in the optical communication.

Features

- Compliant with 100G Ethernet IEEE 802.3bm 100GBASE-SR4 standards
- Compliant to SFF-8636 QSFP28 MSA
- QSFP footprint (Quad small form-factor, pluggable)
- Power consumption < 3.5W
- Full Digital Diagnostics Monitor Interface
- 0 to 70°C case temperature operating range
- Hot pluggable electrical interface
- RoHS-6 Compliant

Application

- 100GBASE-SR4 Ethernet links
- Infiniband EDR, FDR & QDR interconnects

Ordering information

PART NUMBER	TEMPERATURE	Distance	NOTE
LM2C-L3S-TC-N	0°C to 70 °C	OM3=70m/OM4=100m	



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Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_s	-20	85	°C	
3.3V Power Supply Voltage	V_{cc}	-0.5	3.6	V	
Data Input Voltage — Single Ended		-0.5	$V_{cc}+0.5$	V	
Relative Humidity	RH	5	85	%	

Recommend Operating Condition

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Case Temperature	T_c	0		70	°C	
3.3V Power Supply Voltage	V_{cc}	3.14	3.3	3.46	V	
Signal Rate per Channel	B		25.78125		GB/s	
Control Input Voltage High	V_{ih}	2		$V_{cc}+0.3$	V	
Control Input Voltage Low	V_{il}	-0.3		0.8	V	
Two Wire Serial(TWS)Interface Clock Rate				400	KHz	
Receiver Differential Data Output Load	Z_d		100		Ohms	
Power Consumption	P			3.5	W	
Power Supply Current	I_{cc}			1060	mA	



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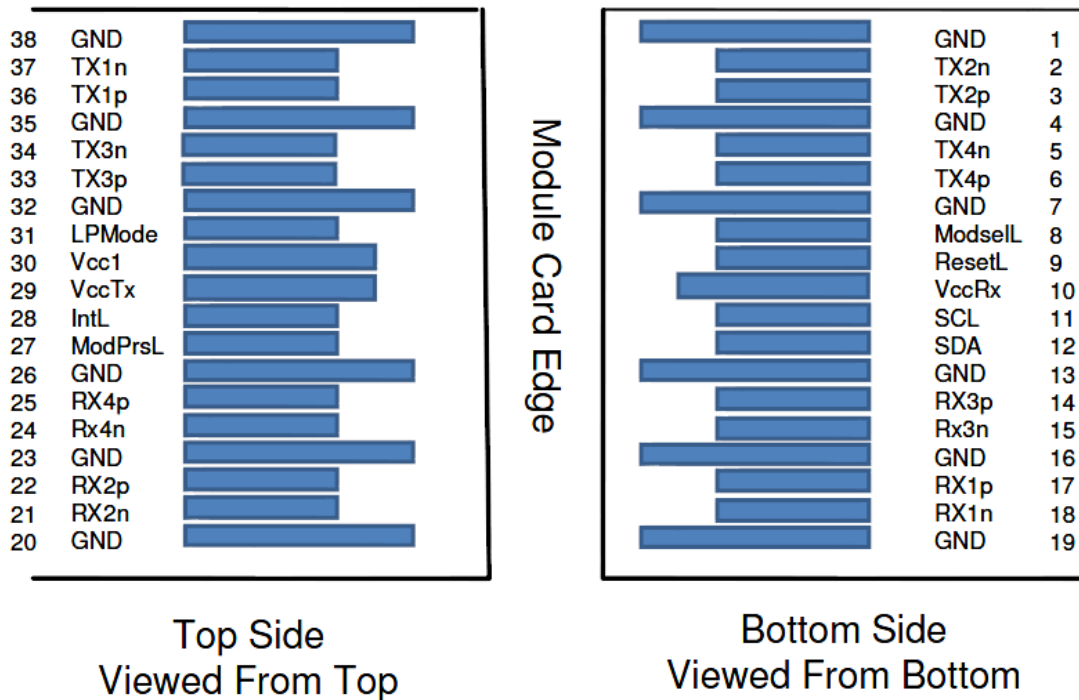
Transmitter Electro-optical characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Central Wavelength	λ	840		860	nm	
Spectral Width – RMS	$\Delta\lambda$			0.6	nm	
Average Output Power, each lane	PO	-8.4		+2.4	dBm	
Optical Modulation Amplitude (OMA)	$POMA$	-6.4		+3	dBm	
Launch power in OMA minus TDEC, each Lane		-7.3			dBm	
Transmitter and dispersion eye closure (TDEC), each Lane	$TDEC$			4.3	dB	
Optical Extinction Ratio	ER	2			dB	
Disabled Output Optical Power	PO_OFF			-30	dBm	
Eye Mask Coordinates: X1, X2, X3; Y1, Y2, Y3.		0.3, 0.38, 0.45, 0.35, 0.41, 0.5			UI	
Optical Return Loss Tolerance				12	dB	
Differential data input voltage	V_{DIFF}	180		1000	mV	

Receiver Electro-optical characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Central wavelength, each lane	λ	840	850	860	nm	
Damage Threshold	DTH	3.4			dBm	
Average Receiver Power, each Lane	PIN_AVG	-10.3		+2.4	dBm	
Stressed sensitivity(OMA)	PIN_s-oma			-5.2	dBm	
LOS Assert	P_A	-30			dBm	
LOS De-Assert	P_D			-11	dBm	
LOS Hysteresis		0.5			dB	
Rise & Fall Time (20%~80%)	Tr/Tf			35	ps	
Differential data output voltage	$V_{out,pp}$	300		1000	mV	

Pad assignment and Description



PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	



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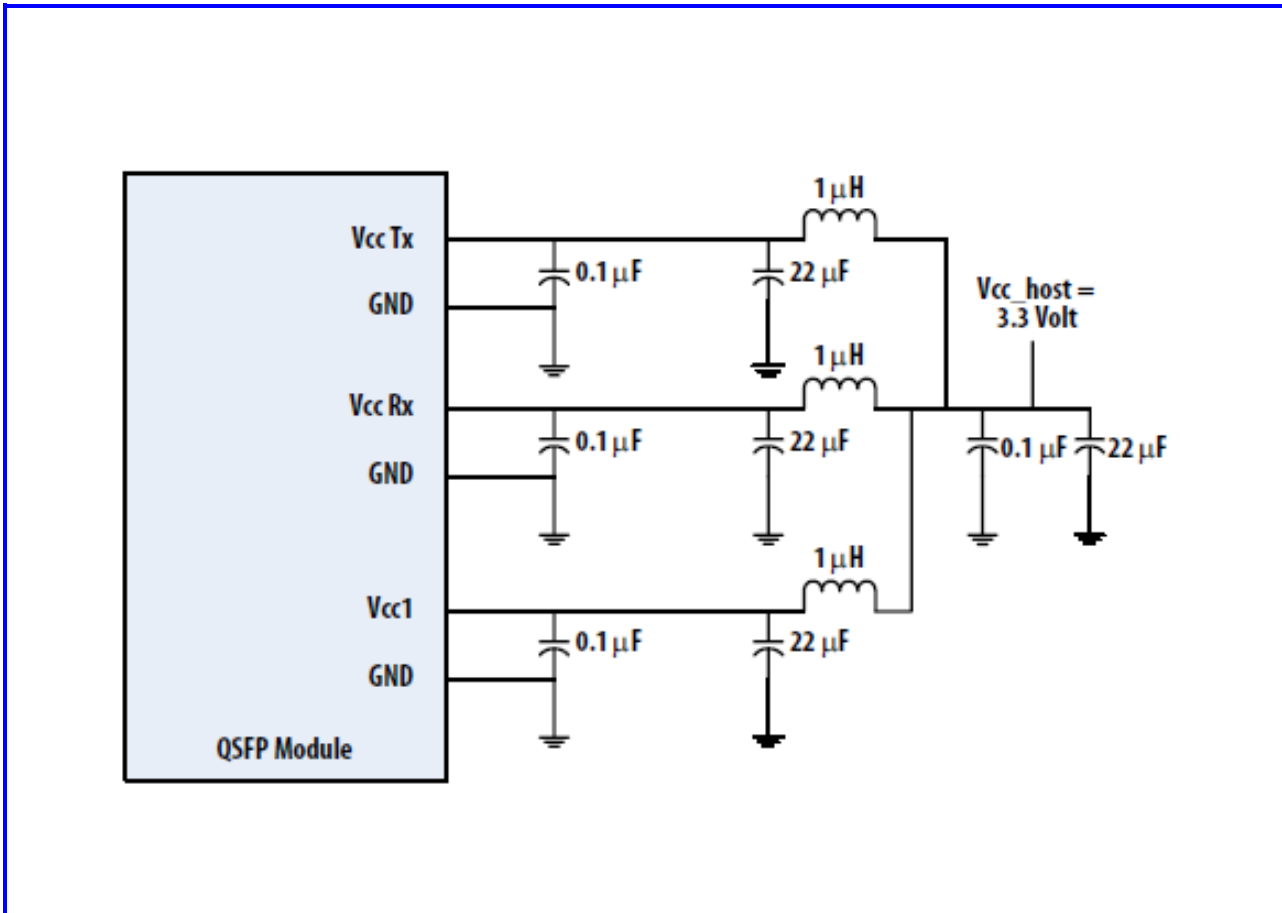
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PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVC MOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

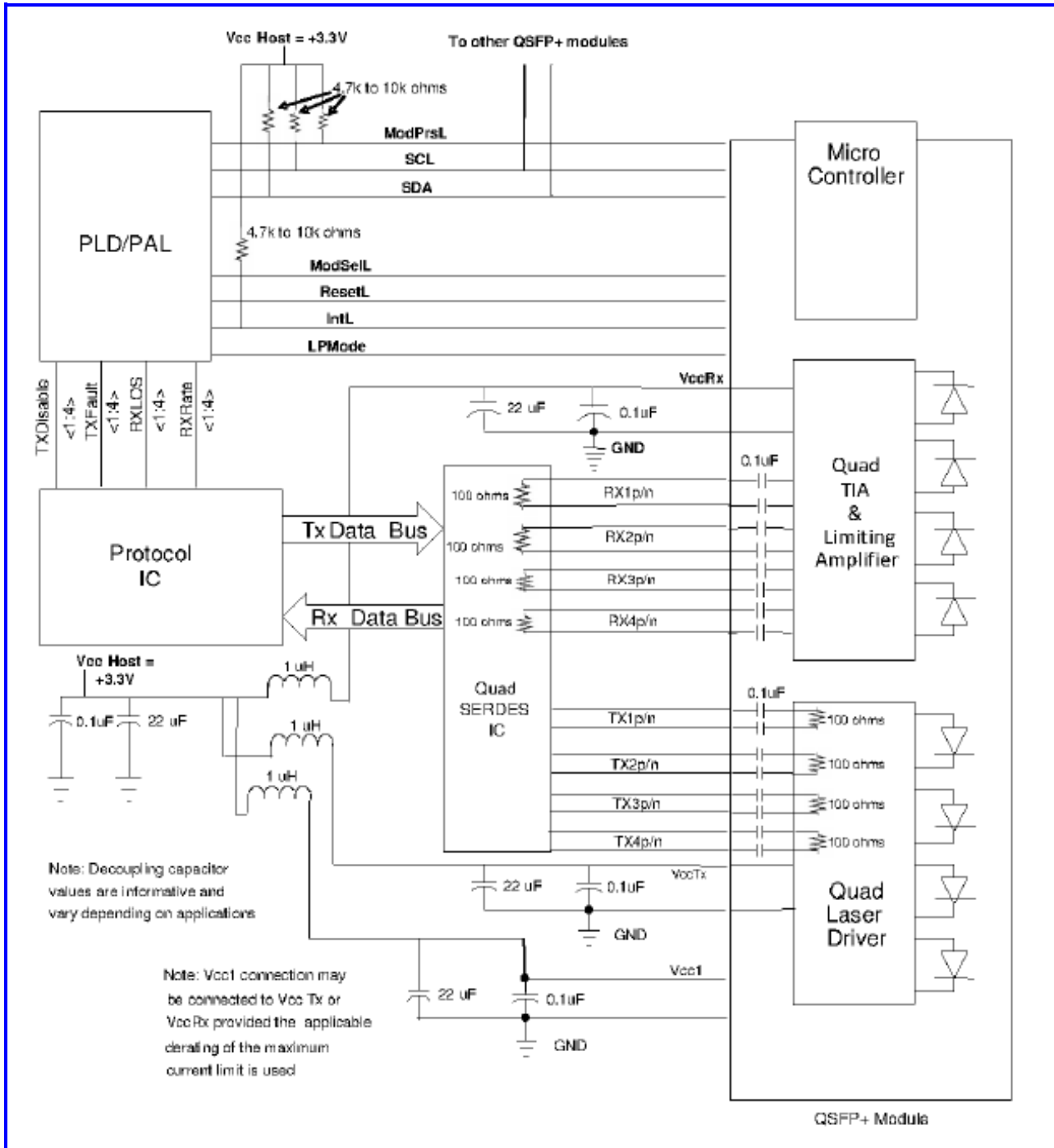
Host board power supply circuit



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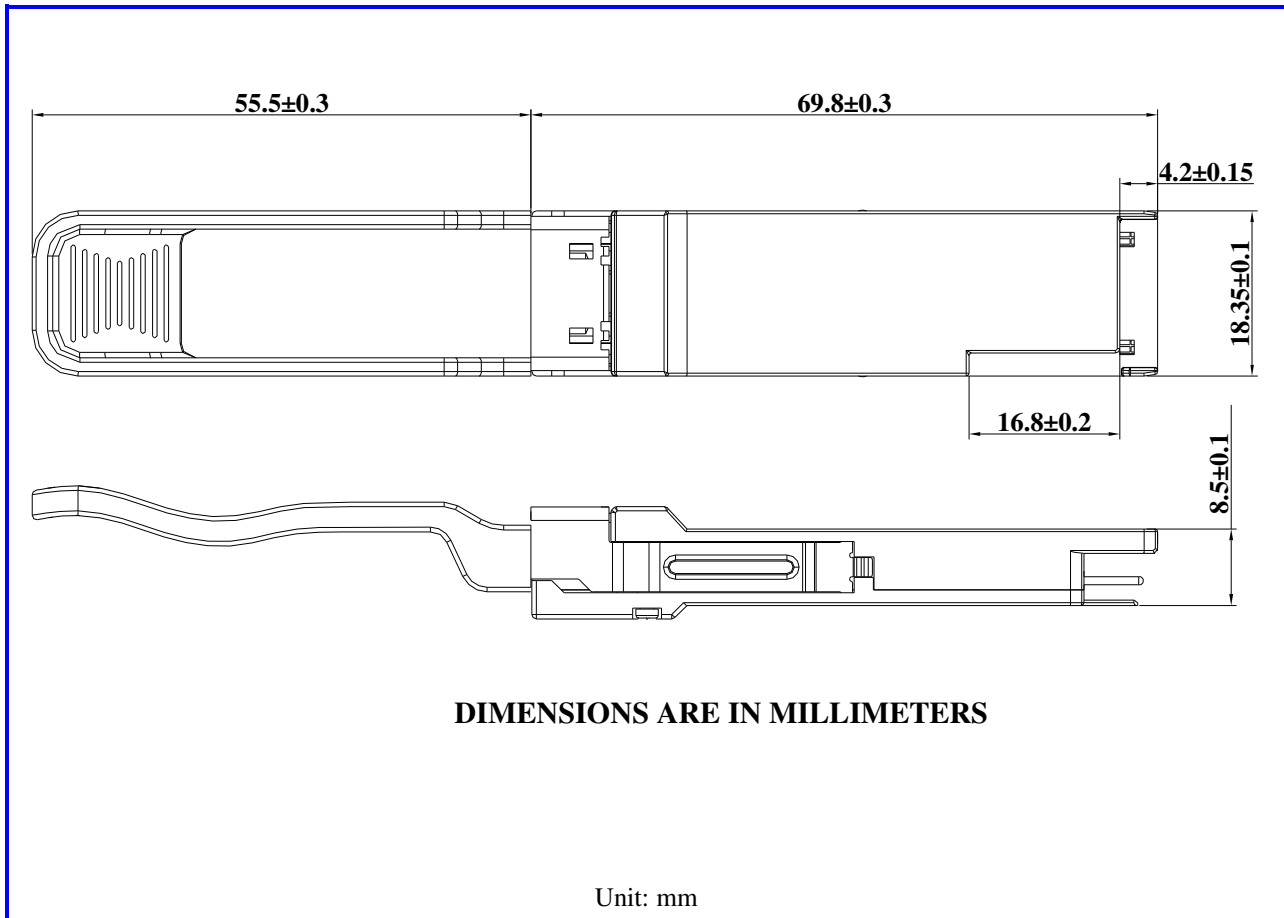
Recommended Interface circuit



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Dimensions





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Memory Map

