



RAYSTAR

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RFC35BR-AIW-DNN

SPECIFICATION

CUSTOMER:

APPROVED BY	
PCB VERSION	
DATE	

FOR CUSTOMER USE ONLY

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

Release DATE:

TFT Display Inspection Specification: <https://www.raystar-optronics.com/download/products.htm>

Precaution in use of TFT module: <https://www.raystar-optronics.com/download/declaration.htm>

Revision History

VERSION	DATE	REVISED PAGE NO.	Note
0 A	2018/07/12 2020/06/12		First issue Modify AC Characteristics

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1.Module Classification Information

R	F	C	35	BR	-	A	I	W	-	D	N	N
1	2	3	4	5	-	6	7	8	-	9	10	11

Item	Description	
1	R : Raystar Optonics Inc.	
2	Display Type : F→TFT Type, J→ Custom TFT	
3	Solution: A: 128x160 B:320x234 C:320x240 D:480x234 E:480x272 F:800x480 G:640x480 H:1024x600 I:320x480 J:240x320 K:1280x800 L:240x400 M:1024x768 N:128x128 O:480x800 P:640x320 Q:800x600 S:480x128 T:800x320	
4	Display Size : 3.5" TFT	
5	Version Code.	
6	Model Type: A : TFT LCD E : TFT+FR+CONTROL BOARD J : TFT+FR+A/D BOARD N : TFT+FR+A/D BOARD+CONTROL BOARD S : TFT+FR+POWER BOARD (DC TO DC) 1 : TFT+CONTROL BOARD	6 : TFT+FR H : TFT+D/V BOARD I : TFT+FR+D/V BOARD B : TFT+POWER BD
7	Polarizer Type, Temperature range, View direction	I→Transmissive, W. T, 6:00 ; C→Transmissive, N. T, 6:00 L→Transmissive, W.T,12:00 ; F→Transmissive, N.T,12:00 Y→Transmissive,W.T, IPS TFT ; A→Transmissive, N.T, IPS TFT Z→Transmissive, W.T, O-TFT R→Transmissive, Super W.T, O-TFT N→Transmissive, Super W.T, 6:00; Q→Transmissive, Super W.T, 12:00 V→Transmissive, Super W.T, VA TFT
8	Backlight	W : LED, White H : LED, High Light White F : CCFL, White
9	Driver Method	D: Digital A: Analog L : LVDS M:MIPI
10	Interface	N : without control board A : 8Bit B : 16Bit S:SPI Interface R: RS232 U:USB I: I2C
11	TS	N : Without TS S : resistive touch panel C : capacitive touch panel capacitive touch panel (G-F-F) G : capacitive touch panel(G-G)

2.Summary

TFT 3.5" is a TN transmissive type color active matrix TFT liquid crystal display that uses amorphous silicon TFT as switching devices. This module is composed of a TFT_LCD module. It is usually designed for industrial application and this module follows RoHS,

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3.General Specifications

- Size: 3.5 inch
- Dot Matrix: 320 x RGBx240(TFT) dots
- Module dimension: 76.84(W) x 63.84(H) x 3.27(D) mm
- Active area: 70.08 x 52.56 mm
- Dot pitch: 0.073 x 0.219 mm
- LCD type: TFT, Normally White, Transmissive
- View Direction: 12 o'clock
- Gray Scale Inversion Direction: 6 o'clock
- Interface: 8-bit/16-bit CPU or option other mode (build in controller)
- Aspect Ratio: 4:3
- Backlight Type: LED, Normally White
- IC: SSD2119
- With /Without TP: Without TP
- Surface: Anti-Glare

*Color tone slight changed by temperature and driving voltage.

4.Interface

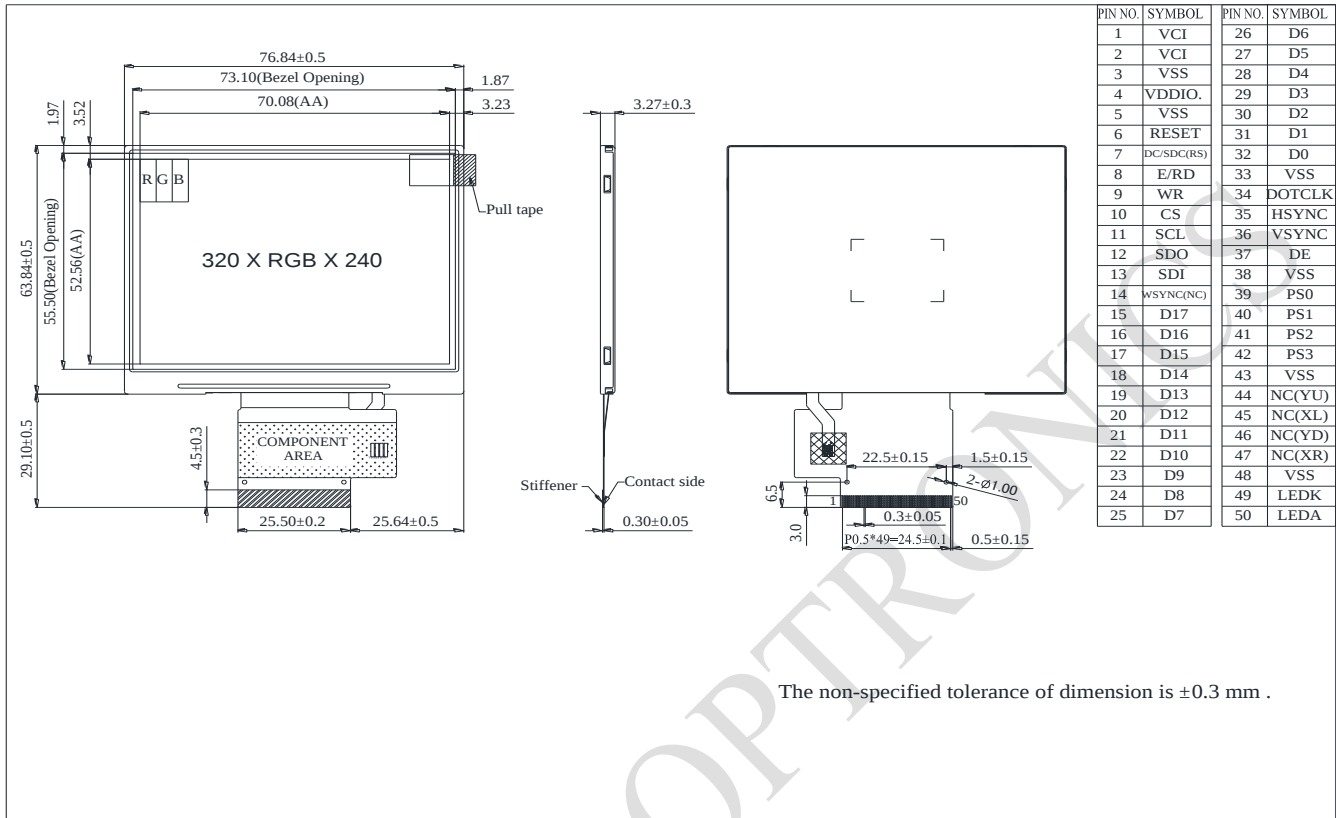
4.1. LCM PIN Definition

No.	Symbol	Description
1	VCI	Booster input voltage pin
2	VCI	Booster input voltage pin
3	VSS	Ground
4	VDDIO	Voltage input pin for logic
5	VSS	Ground
6	RESET	Reset Signal pin ("Low" is enable)
7	DC/SDC	Data or Command select PIN.
8	E/RD	6800 system: E(enable signal) 8080 system : RD(read strobe signal) Serial mode: Not use and should be connected to VDDIO or VSS
9	WR	6800 system : RW (indicates read cycle when high ,write cycle when low) 8080 system : WR (write strobe signal)
10	CS	Chip select
11	SCL	Serial Clock.
12	SD0	Serial Data output
13	SDI	Serial Data Input
14	WSYNC	Ram write synchronization output. Leave it OPEN when not used.
15~32	D17~D0	Data bus
33	VSS	Ground
34	DOTCLK	Dot-clock signal and oscillator source
35	HSYNC	Line Synchronous Signal
36	VSYNC	Frame Synchronous Signal
37	DE	Display enable pin for controller
38	VSS	Ground
39	PS0	Interface select PIN
40	PS1	
41	PS2	
42	PS3	
43	VSS	Ground
44~47	NC	NC

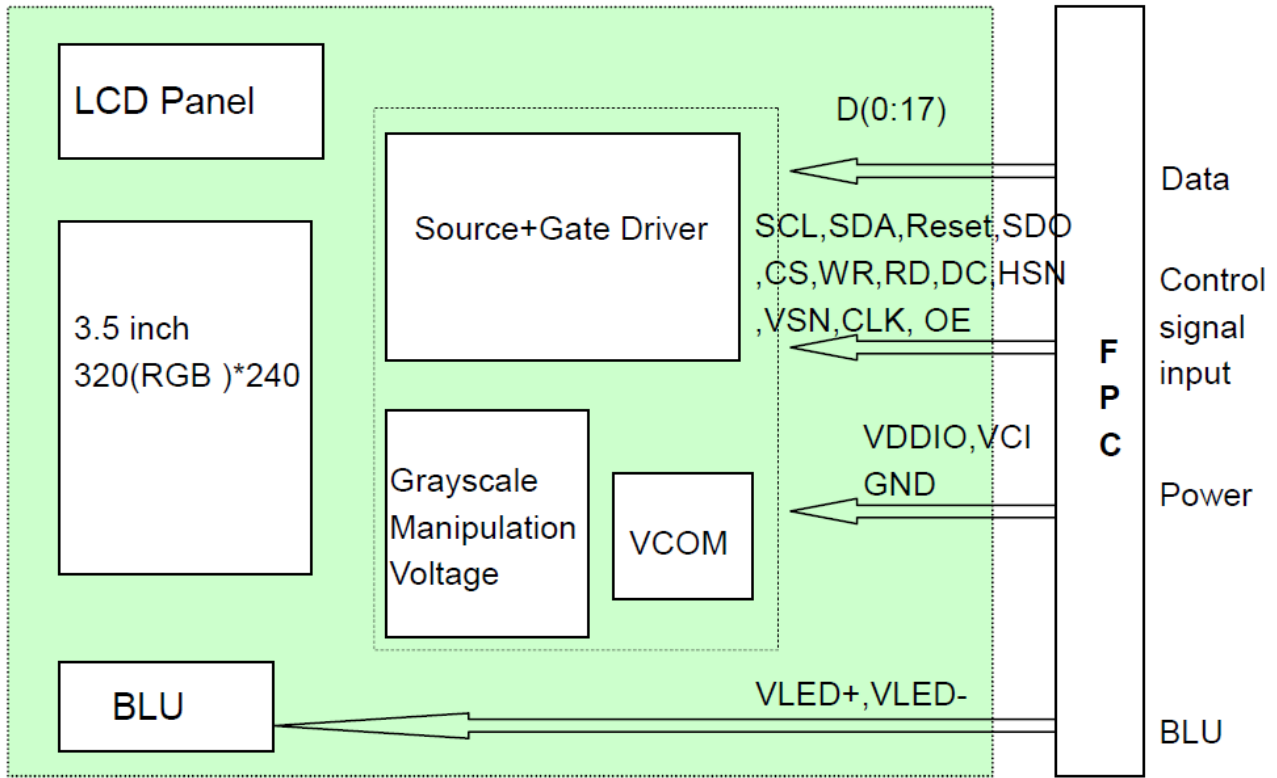
48	VSS	Ground
49	LEDK	Backlight LED Cathode
50	LEDA	Backlight LED Anode.

PS3	PS2	PS1	PS0	Interface Mode	Data bus input
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]
0	0	0	1	8-bit 6800 parallel interface	D[17:10]
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]
0	0	1	1	8-bit 8080 parallel interface	D[17:10]
0	1	0	0	9-bit generic D[9:16] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally	
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI	
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI	
0	1	1	1	6-bit generic D[8:3] (262k colour) + 3-wire SPI	
1	0	0	0	18-bits 6800 parallel interface	D[17:0]
1	0	0	1	9-bits 6800 parallel interface	D[17:9]
1	0	1	0	18-bit 8080 parallel interface	D[17:0]
1	0	1	1	9-bit 8080 parallel interface	D[17:9]
1	1	1	0	3-wire SPI	
1	1	1	1	4-wire SPI	

5. Contour Drawing



6. Block Diagram



7. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	°C
Storage Temperature	TST	-30	—	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

- Temp. $\leq 60^{\circ}\text{C}$, 90% RH MAX. Temp. $> 60^{\circ}\text{C}$, Absolute humidity shall be less than 90% RH at 60°C

8. Electrical Characteristics

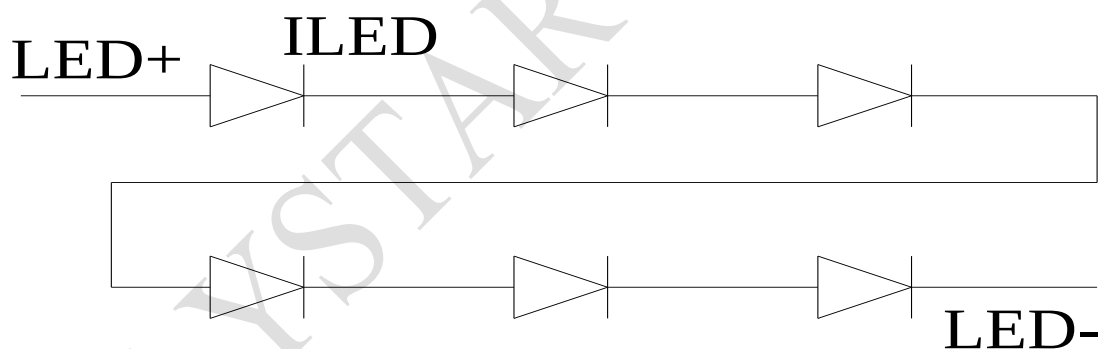
8.1. Operating conditions:

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Power supply voltage	VCI	2.5	3.3	3.6	V	
Power supply pin of IO pins	VDDIO	1.4	3.3	3.6	V	
Current consumption	IVCI+IVDDIO	-	6	-	mA	
Dot clock	DCK	-	5.5	8.2	MHz	

8.2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		-	20	-	mA	
Power Consumption		348	384	408	mW	
LED voltage	LED+	17.4	19.2	20.4	V	Note 1
LED Life Time		-	50,000	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



Note 2 : $T_a = 25^\circ\text{C}$

Note 3 : Brightness to be decreased to 50% of the initial value

Note 4 : The single LED lamp case

9.AC Characteristics

9.1. Parallel 6800-series Interface Timing Characteristics

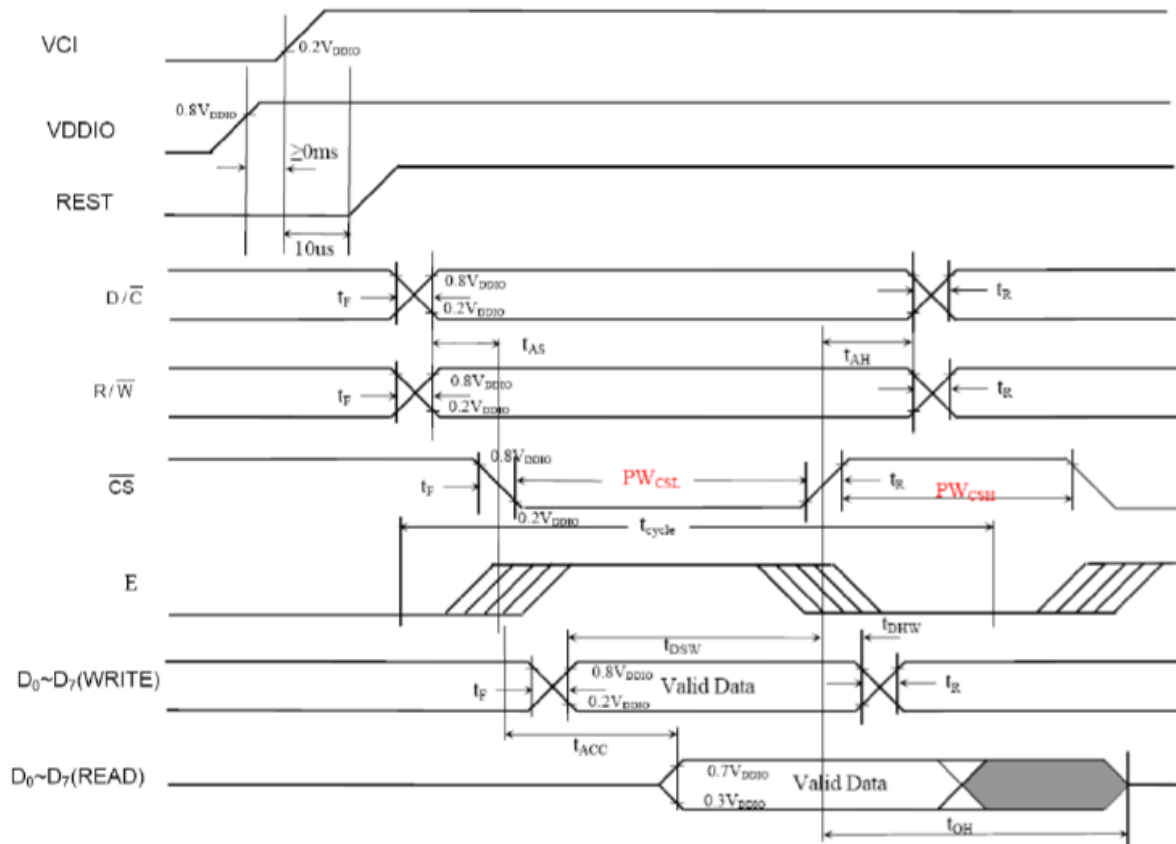
(TA = -40 to 85 °C, VDDIO = 1.4V to 2.4)

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock cycle time (write cycle)	75	-	-	ns
tcycle	Clock cycle time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	1000	-	-	ns
tAS	Address setup time (R/W)	0	-	-	ns
tAH	Address hold time (R/W)	0	-	-	ns
tDSW	Data setup time(D0~D7,WRITE)	5	-	-	ns
tDHW	Data hold time(D0~D7,WRITE)	5	-	-	ns
tACC	Data access time(D0~D7,READ)	250	-	-	ns
tOH	Output hold time(D0~D7,READ)	100	-	-	ns
PWCSL	Pulse width/CS low(write cycle)	40	-	-	ns
PWCSH	Pulse width/CS high(write cycle)	25	-	-	ns
PWCSL	Pulse width/CS low(read cycle)	500	-	-	ns
PWCSH	Pulse width/CS high(read cycle)	500	-	-	ns
tR	Rise time(/CS)	-	-	15	ns
tF	Fall time(/CS)	-	-	15	ns

(TA = -40 to 85 °C, VDDIO = 2.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock cycle time (write cycle)	75	-	-	ns
tcycle	Clock cycle time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
tAS	Address setup time (R/W)	0	-	-	ns
tAH	Address hold time (R/W)	0	-	-	ns
tDSW	Data setup time(D0~D7,WRITE)	5	-	-	ns
tDHW	Data hold time(D0~D7,WRITE)	5	-	-	ns
tACC	Data access time(D0~D7,READ)	200	-	-	ns
tOH	Output hold time(D0~D7,READ)	100	-	-	ns
PWCSL	Pulse width/CS low(write cycle)	40	-	-	ns
PWCSH	Pulse width/CS high(write cycle)	25	-	-	ns
PWCSL	Pulse width/CS low(read cycle)	225	-	-	ns
PWCSH	Pulse width/CS high(read cycle)	225	-	-	ns
tR	Rise time(/CS)	-	-	15	ns
tF	Fall time(/CS)	-	-	15	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

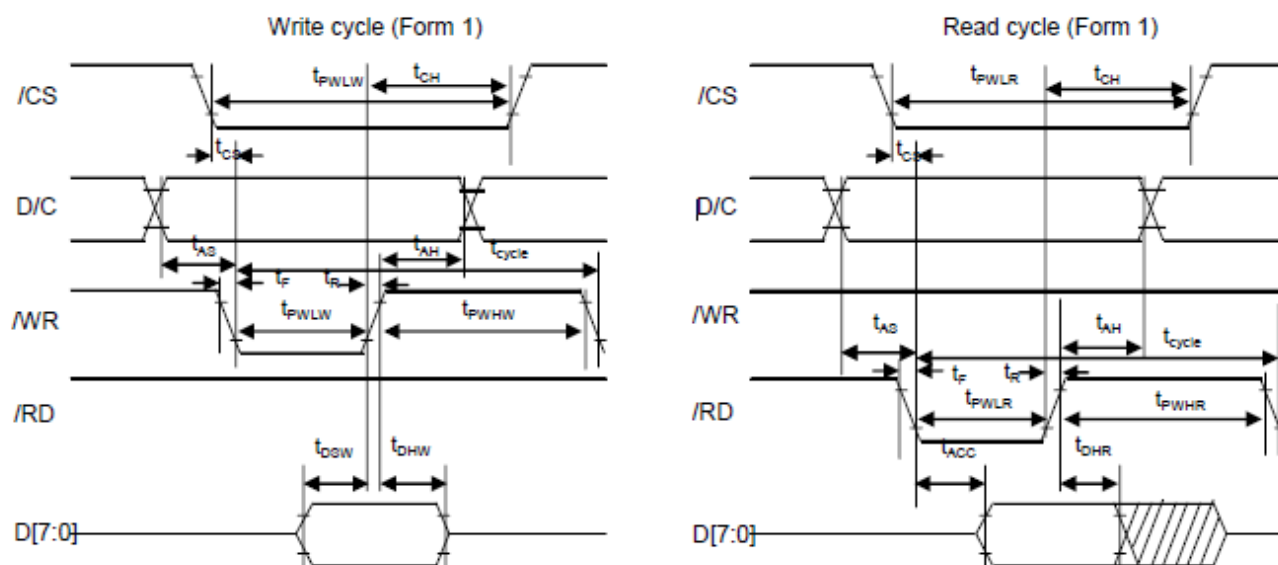
Parallel 6800-series interface timing characteristics


9.2. Parallel 8080 Timing Characteristics

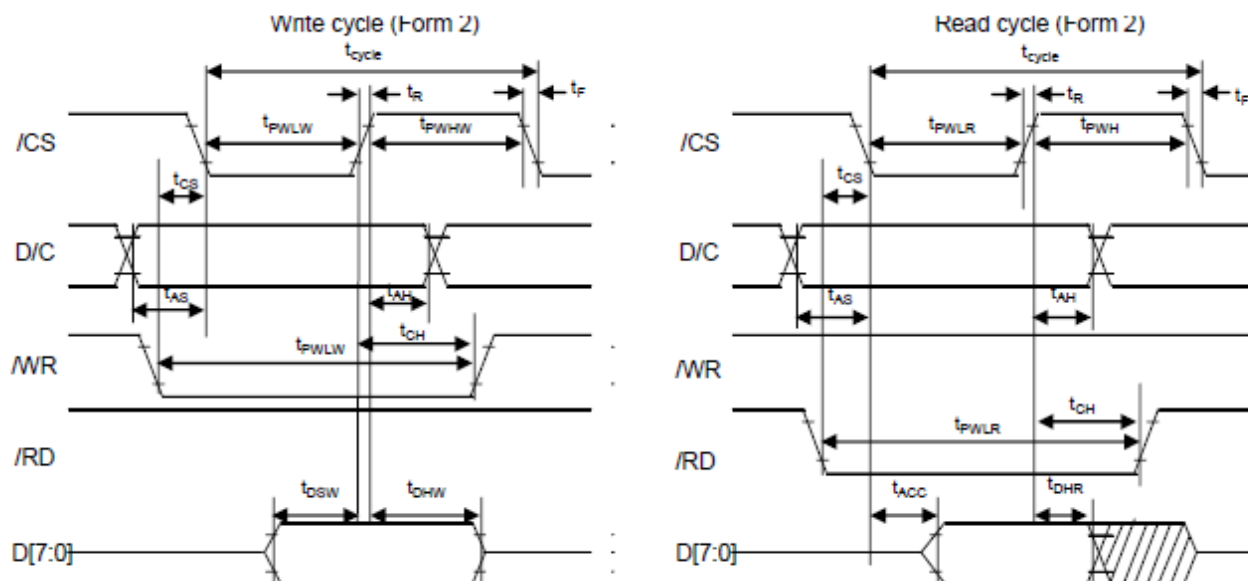
Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock cycle time (write cycle)	100	-	-	ns
t _{AS}	Address setup time	10	-	-	ns
t _{AH}	Address hold time	0	-	-	ns
t _{CS}	Chip select time	0			ns
t _{CH}	Chip select hold time	0			ns
t _{DSW}	Write Data setup time	10	-	-	ns
t _{DHW}	Write Data hold time	10	-	-	ns
t _{DHR}	Read Data hold time	100			ns
t _{ACC}	Access time(RAM)	250	-	-	ns
	Access time(command)	250			ns
t _{PWLR}	Chip select low pulse width(read RAM)	500	-	-	ns
t _{PWLR}	Chip select low pulse width(read command)	500			ns
t _{PWLW}	Chip select low pulse width(write)	50			ns
t _{PWHR}	Chip select high pulse width(read)	500	-	-	ns
t _{PWHW}	Chip select high pulse width(write)	50			ns
t _R	Rise time	-	-	15	ns
t _F	Fall time	-	-	15	ns

Note: all timings are based on 20% to 80% of $V_{DDIO}-V_{SS}$

8080-series parallel interface characteristics (Form 1: /CS low pulse width > W/ R low pulse width)



8080-series parallel interface characteristics (Form 2: /CS low pulse width < W/ R low pulse width)

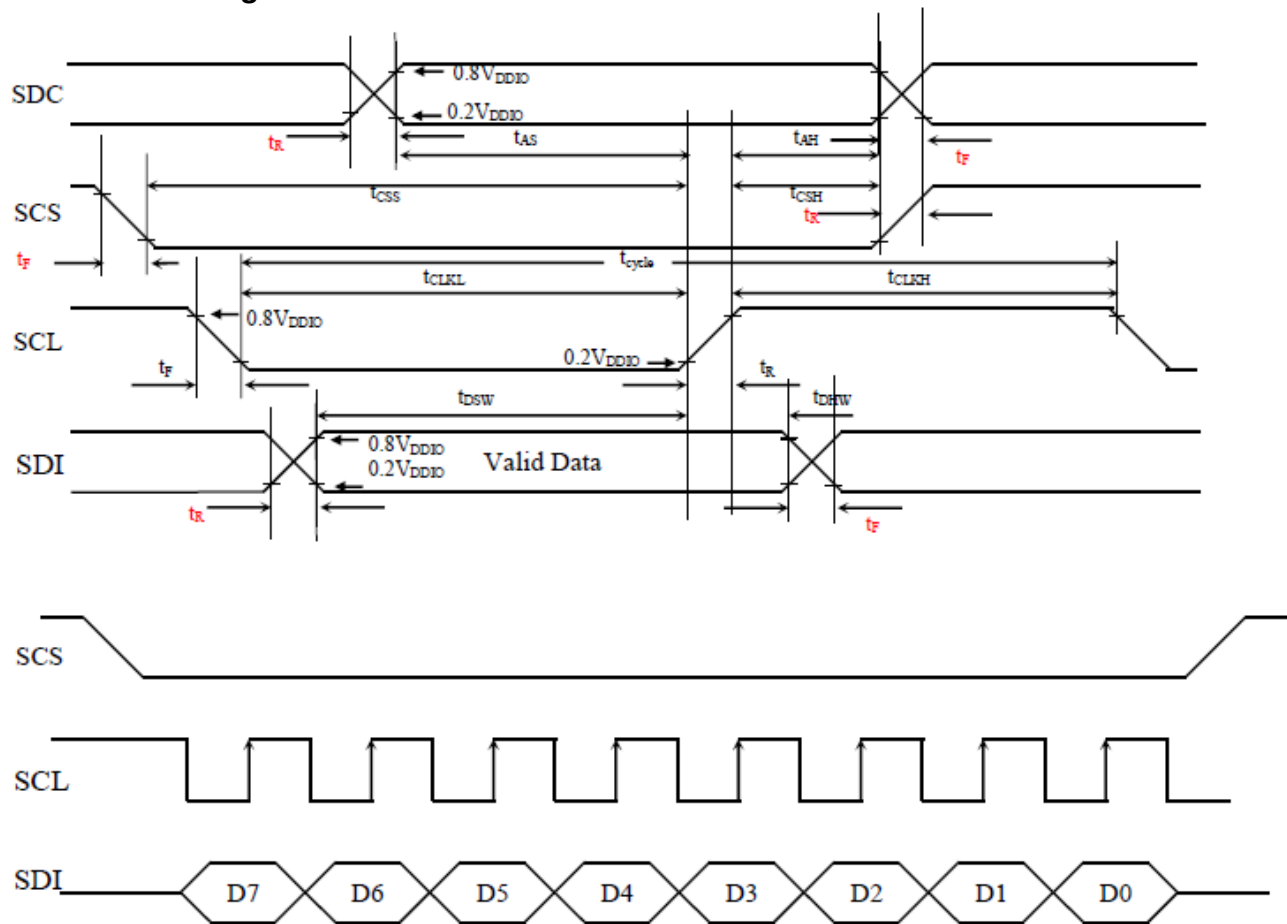


9.3. Serial Timing Characteristics

(Ta=-40 to 85°C, VDDIO = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock cycle time	77	-	-	ns
f _{CLK}	Serial clock cycle time SPI clock tolerance =+/- 2 ppm	-	-	15	MHz
t _{AS}	Register select setup time	4	-	-	ns
t _{AH}	Register select hold time	5	-	-	ns
t _{CSS}	Chip select setup time	2			ns
t _{CSH}	Chip select hold time	10			ns
t _{DSW}	Write Data setup time	5	-	-	ns
t _{DHW}	Write Data hold time	10	-	-	ns
t _{CLKL}	Clock low time	38			ns
t _{CLKH}	Clock high time	38	-	-	ns
t _R	Rise time	-	-	15	ns
t _F	Fall time	-	-	15	ns

4 wire serial timing characteristics



9.4. RGB Timing Characteristics

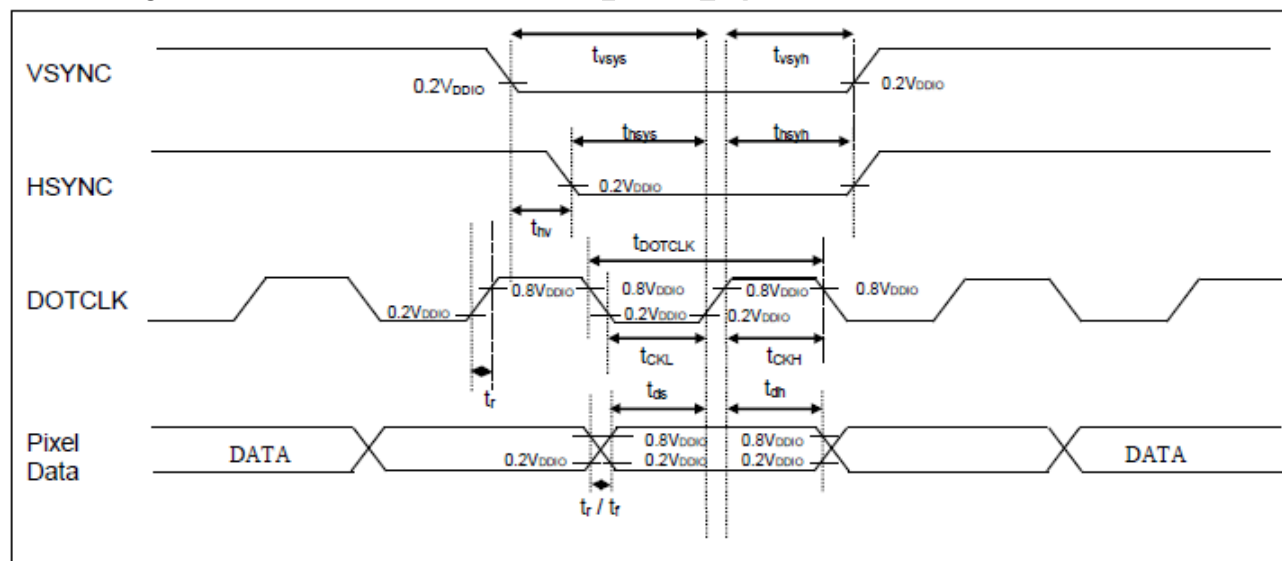
($T_a = -40$ to 85°C , $V_{DDIO} = 1.4\text{V}$ to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
fDOTCLK	DOTCLK frequency (70Hz frame rate)	1	5.5	8.2	MHZ
tDOTCLK	DOTCLK period	122	182	1000	ns
tVSYS	Vertical sync setup time	20	-	-	ns
tVSYH	Vertical sync hold time	20	-	-	ns
tHSYS	Horizontal sync setup time	20	-	-	ns
tHSYH	Horizontal sync hold time	20	-	-	ns
tHV	Phase difference of sync signal falling edge	0	-	HFP-1	t_{DOTCLK}
tCLK	DOTCLK low period	61	-	-	ns
tCKH	DOTCLK high period	61	-	-	ns
tDS	Data setup time	25	-	-	ns
tDH	Data hold time	25	-	-	ns

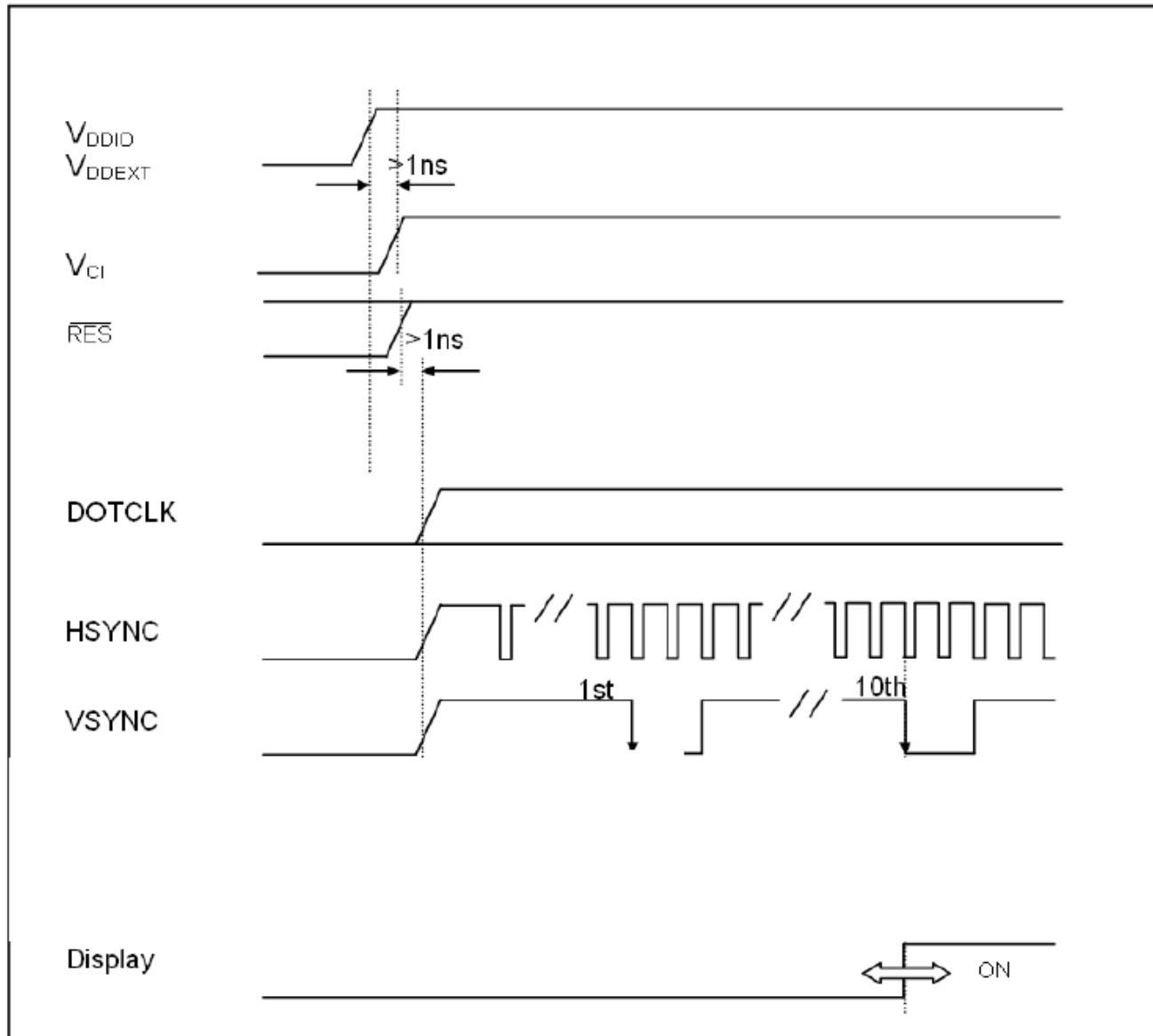
Note: External clock source must be provided to DOTCLK pin of SSD2119M1. The driver will not operate in absence of the clocking signal.

*HFP: Horizontal Front Porch setting in customers' setup

RGB timing characteristics

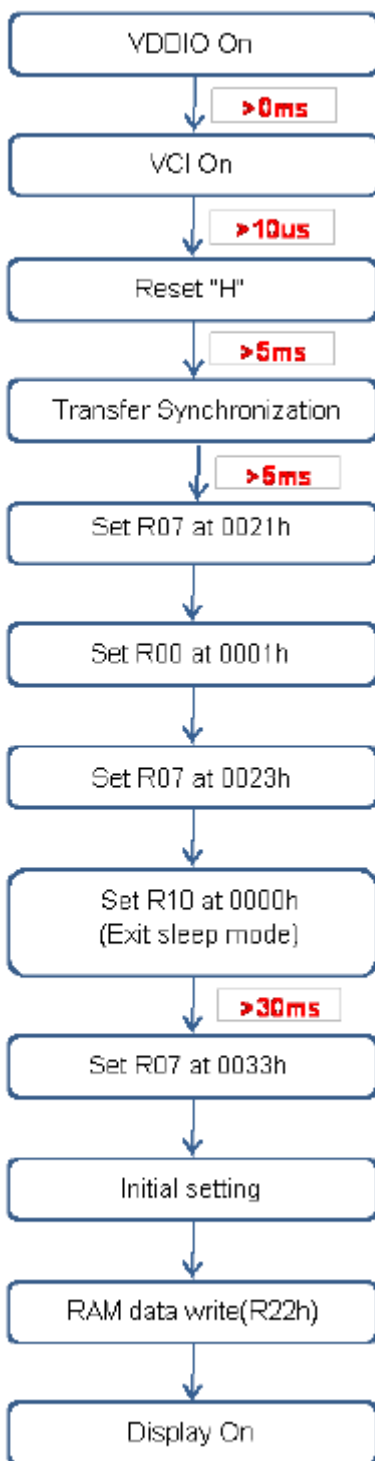


9.5. Power Up Sequence for RGB mode



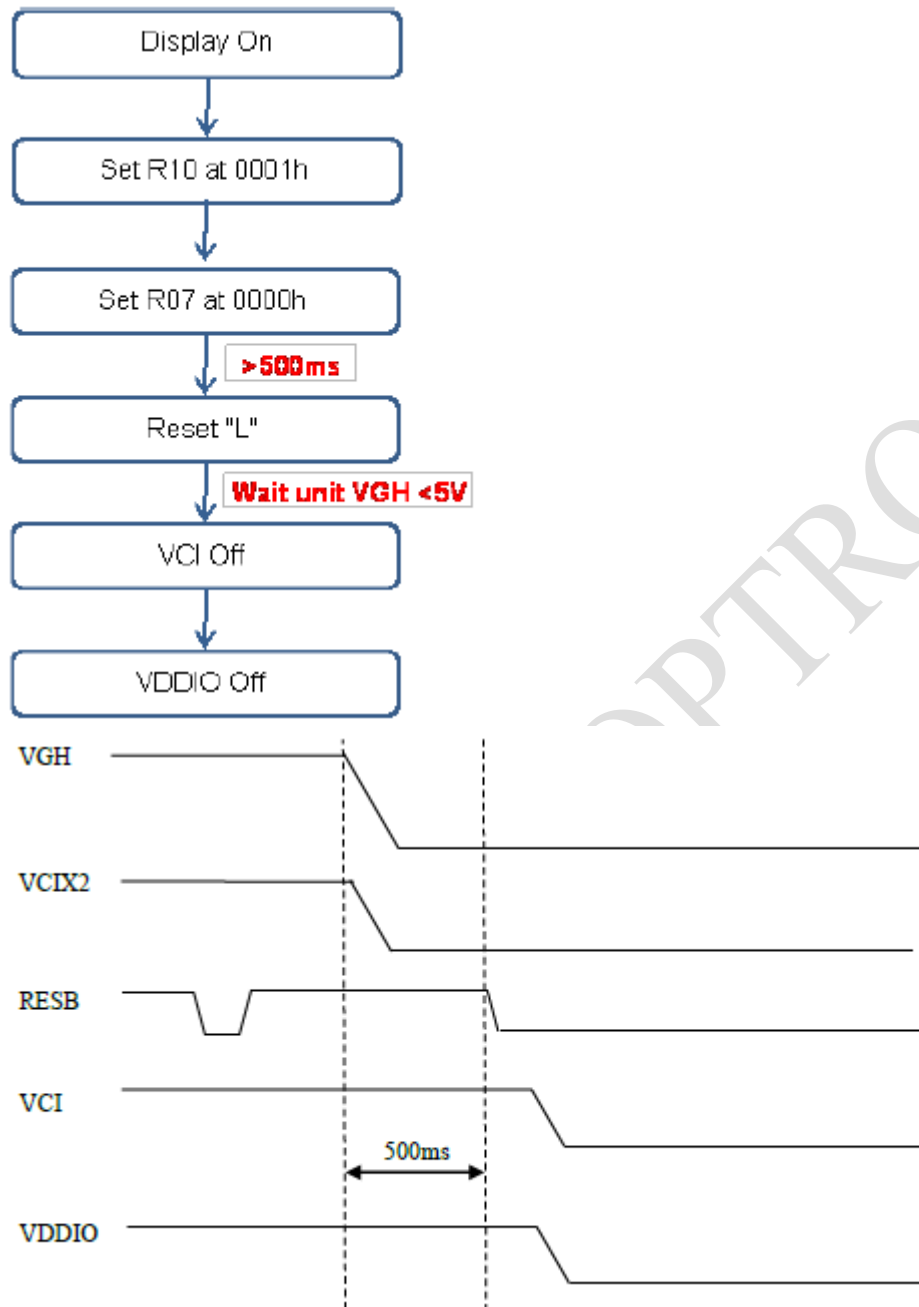
9.6. Display on sequence

Note: To prevent potential damage to the device, all capacitors must be discharged to below 0.5V before the driver is removed from, or before the driver is attached to those components.



9.7. Display off sequence

Note: To prevent potential damage to the device, all capacitors must be discharged to below 0.5V before the driver is removed from, or before the driver is attached to those components.



Note:

1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the OTP programming voltage should be turned off and cap discharged before VCI/VDDIO are turned off.

10. Optical Characteristics

Item	Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time	Tr	$\theta=0^\circ$ 、 $\phi=0^\circ$	-	10	-	ms	Note 3,5
	Tf		-	15	-	ms	
Contrast ratio	CR	At optimized viewing angle	200	300	-	-	Note 4,5
Color Chromaticity	White	$\theta=0^\circ$ 、 $\phi=0^\circ$	0.26	0.31	0.36	-	Note 2,6,7
	Wy		0.28	0.33	0.38	-	
Viewing angle (Gray Scale Inversion Direction)	Hor.	θ_R	-	60	-	Deg.	Note 1
		θ_L	-	60	-		
	Ver.	ϕ_T	-	50	-		
		ϕ_B	-	60	-		
Brightness	-	-	350	400	-	cd/m ²	Center of display

Ta=25±2℃, IL=20mA

Note 1: Definition of viewing angle range

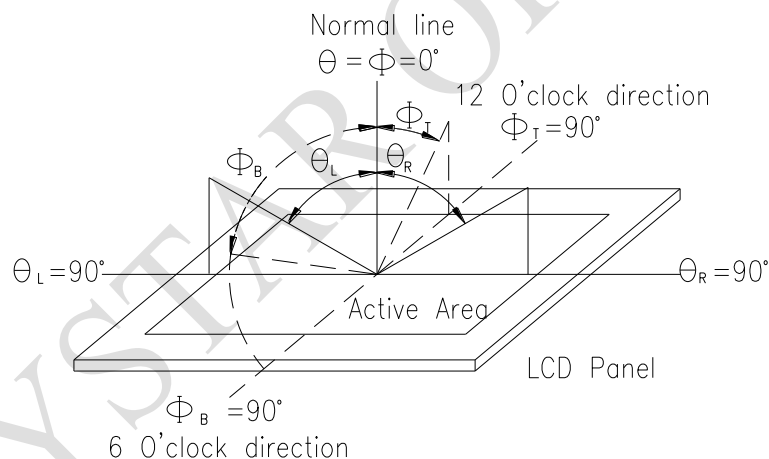


Fig. 10.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

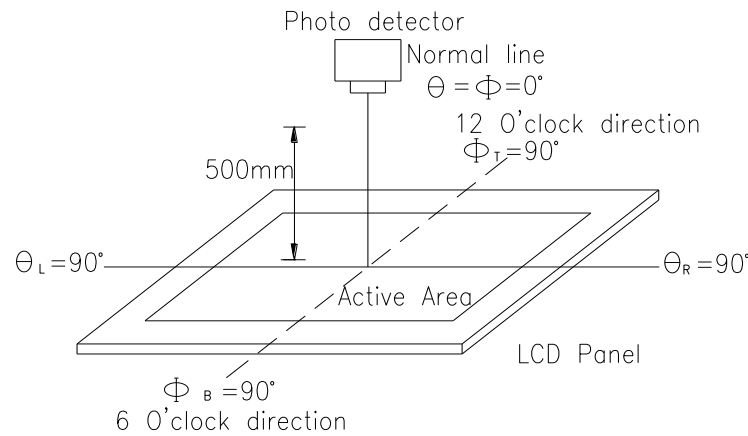
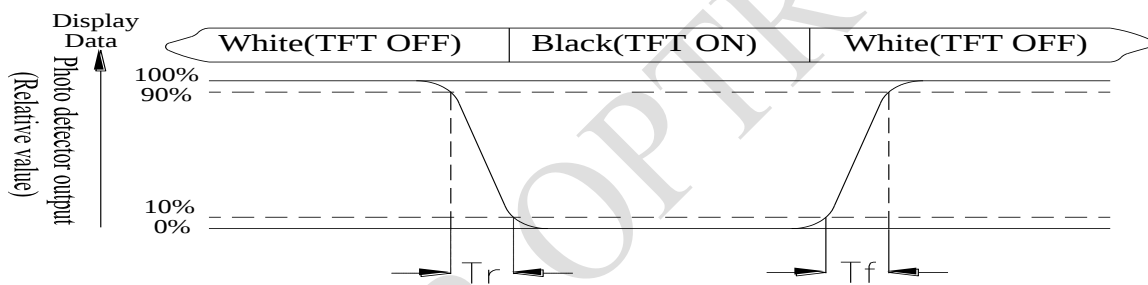


Fig. 10.2. Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, T_r , is the time between photo detector output intensity changed from 90% to 10%. And fall time, T_f , is the time between photo detector output intensity changed from 10% to 90%



Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White $V_i = V_{i50} \pm 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

“ $\pm$ ” means that the analog input signal swings in phase with VCOM signal.

“ $\pm$ ” means that the analog input signal swings out of phase with VCOM signal.

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

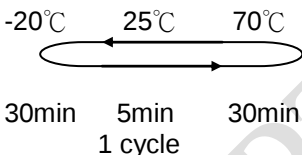
Note 6: Definition of color chromaticity (CIE 1931)

Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

11. Reliability

Content of Reliability Test (Wide temperature, -20°C~70°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max	60°C,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation 	-20°C/70°C 10 cycles	—
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 3 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact) ,±800v(air), RS=330Ω CS=150pF 10 times	—

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

LCM Sample Estimate Feedback Sheet		
Module Number : _____		
1 、 Panel Specification :		
1. Panel Type :	☐ Pass	☐ NG , _____
2. View Direction :	☐ Pass	☐ NG , _____
3. Numbers of Dots :	☐ Pass	☐ NG , _____
4. View Area :	☐ Pass	☐ NG , _____
5. Active Area :	☐ Pass	☐ NG , _____
6. Operating Temperature :	☐ Pass	☐ NG , _____
7. Storage Temperature :	☐ Pass	☐ NG , _____
8. Others : _____		
2 、 Mechanical Specification :		
1. PCB Size :	☐ Pass	☐ NG , _____
2. Frame Size :	☐ Pass	☐ NG , _____
3. Material of Frame :	☐ Pass	☐ NG , _____
4. Connector Position :	☐ Pass	☐ NG , _____
5. Fix Hole Position :	☐ Pass	☐ NG , _____
6. Backlight Position :	☐ Pass	☐ NG , _____
7. Thickness of PCB :	☐ Pass	☐ NG , _____
8. Height of Frame to PCB :	☐ Pass	☐ NG , _____
9. Height of Module :	☐ Pass	☐ NG , _____
10. Others :	☐ Pass	☐ NG , _____
3 、 Relative Hole Size :		
1. Pitch of Connector :	☐ Pass	☐ NG , _____
2. Hole size of Connector :	☐ Pass	☐ NG , _____
3. Mounting Hole size :	☐ Pass	☐ NG , _____
4. Mounting Hole Type :	☐ Pass	☐ NG , _____
5. Others :	☐ Pass	☐ NG , _____
4 、 Backlight Specification :		
1. B/L Type :	☐ Pass	☐ NG , _____
2. B/L Color :	☐ Pass	☐ NG , _____
3. B/L Driving Voltage (Reference for LED Type) : ☐ Pass ☐ NG , _____		
4. B/L Driving Current :	☐ Pass	☐ NG , _____
5. Brightness of B/L :	☐ Pass	☐ NG , _____
6. B/L Solder Method :	☐ Pass	☐ NG , _____
7. Others :	☐ Pass	☐ NG , _____

>> Go to page 2 <<

Module Number : _____

5 、 Electronic Characteristics of Module :

1.Input Voltage :	☐ Pass	☐ NG , _____
2.Supply Current :	☐ Pass	☐ NG , _____
3.Driving Voltage for LCD :	☐ Pass	☐ NG , _____
4.Contrast for LCD :	☐ Pass	☐ NG , _____
5.B/L Driving Method :	☐ Pass	☐ NG , _____
6.Negative Voltage Output :	☐ Pass	☐ NG , _____
7.Interface Function :	☐ Pass	☐ NG , _____
8.LCD Uniformity :	☐ Pass	☐ NG , _____
9.ESD test :	☐ Pass	☐ NG , _____
10.Others :	☐ Pass	☐ NG , _____

6 、 Summary :
Sales signature : _____

Customer Signature : _____

Date : / /