Ver 1.0

BQ7V Series FPGA

Datasheet

Part Number: BQ7VX330TBG1761 / BQ7VX690TBG1761 / BQ7VX690TBG1927

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	20220121		Initial Release.	

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1. Product Description

1.1 Features

- **Fully compatible with Virtex7 series of Xilinx and higher security**
  - Optimized for highest system performance
  - Speed grade same with Virtex7 series "-1M"
  - Solve the "StarBleed" vulnerability at the hardware level, provide higher security for users
- **Configurable Logic Block（CLB）**
  - Real 6-input look-up tables (LUTs)
  - Memory capability within the LUT
  - Register and shift register functionality
- **Clock Management Tile (CMT)**
  - High-speed buffers and routing for low-skew clock distribution
  - Frequency synthesis and phase shifting
  - Low-jitter clock generation and jitter filtering
- **Block RAM**
  - Dual-port 36 Kb block RAM with port widths of up to 72
  - Programmable FIFO logic
  - Built-in optional error correction circuitry
- **Digital Signal Processing Slice (DSP)**
  - 25 × 18 two's complement multiplier/48-bit accumulator
  - Power saving pre-adder to optimize symmetrical filter applications
  - Optional pipelining, optional ALU, and dedicated buses for cascading
- **Input/Output（IOB）**
  - High-performance SelectIO technology with support for DDR3
  - High range (HR) I/O [1], from 1.2V to 3.3V
  - High performance (HP) I/O, from 1.2V to 1.8V
  - High-frequency decoupling capacitors for enhanced signal integrity
  - Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation
- **Low-Power Gigabit Transceivers（GTH）**
  - capable of 8.5 Gb/s line rates
  - Low-power mode to optimize chip-to-chip interfaces
- **Integrated Interface Blocks for PCI Express Designs**
  - Compliant to the PCI Express Base Specification 3.0 with Endpoint and Root Port capability
- **Configuration**
  - High-speed SPI and BPI Flash configuration
  - 256-bit AES encryption with HMAC/ SHA-256 authentication
  - Partial reconfiguration
- **XADC(Analog-to-Digital Converter)**
  - 12-bit 1 MSPS analog-to-digital converters (ADCs)
  - Up to 17 flexible and user-configurable analog inputs
  - On-chip temperature and power supply voltage sensors
  - Continuous JTAG access to ADC measurements
- **28 nm CMOS Process Technology**
- **1.0V Core Voltage**
- **Reliability**
  - temperature range: –55℃ to +125℃
  - ESD (human body model): 2000V for regular I/O and power, 1500V for GTH Transceivers.

Notes:

1. BQ7VX690T does not include HR.

1.2 General Description

The BQ7V Series FPGA is a new generation of high performance SRAM FPGA. In addition to the advanced, high-performance logic fabric, BQ7V FPGAs contain many hard-IP system level blocks, including powerful 36-Kbit block RAM/FIFOs, 25 x 18 DSP slices, SelectIO technology with built-in digitally-controlled impedance, ChipSync source-synchronous interface blocks, system monitor functionality, enhanced clock management tiles with integrated mixed-mode clock manager and phase-locked loop clock generators, and advanced configuration options. Additional platform dependent features include power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, and integrated blocks for PCI Express. Most importantly, BQ7V FPGAs provide higher security for users by solving the “StarBleed” vulnerability at the hardware level. These features allow advanced logic designers to build high levels of performance and functionality into their FPGA-based systems. Built on a 28-nm CMOS process technology, BQ7V FPGAs are a programmable alternative to custom ASIC technology. The most advanced system designs require the programmable strength of FPGAs. BQ7V FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities.

The BQ7V series FPGA currently includes three products BQ7VX330TBG1761, BQ7VX690TBG1761 and BQ7VX690TBG1927. The details are as follows：

Device	CLB		DSP slice	BRAM MAX (Kb)	CMT	PCIe	GTH	XADC	User IO	Package
	slice	Distributed RAM (Kb)								
BQ7VX330TBG1761	51000	4388	1120	27000	14	2	28	1	700	PBGA1761
BQ7VX690TBG1761	108300	10888	3600	52920	20	3	36	1	850	PBGA1761
BQ7VX690TBG1927	108300	10888	3600	52920	20	3	80	1	600	PBGA1927

2. DC Characteristics

2.1 Absolute Maximum Ratings

a) Internal supply voltage（V_{CCINT}）：-0.5V～1.1V

b) Auxiliary supply voltage（V_{CCAUX}）：-0.5V～2.0V

c) Auxiliary supply voltage（V_{CCAUX_IO}）：-0.5V～2.06V

d) Supply voltage for the block RAM memories（V_{CCBRAM}）：-0.5V～1.1V

e) Output drivers supply voltage（V_{CCO}）：-0.5V～3.6V（3.3V HR I/O banks）
-0.5V～2.0V（1.8V HP I/O banks）

f) Key memory battery backup supply（V_{CCBATT}）：-0.5V～2.0V

g) Input reference voltage（V_{REF}）：-0.5 V～2.0 V

h) I/O input voltage（V_{IN}）：
-0.40V～VCCO +0.55V（3.3V HR I/O banks）
-0.55V～VCCO +0.55V（1.8V HP I/O banks）
-0.40V～2.625V （when VCCO=3.3V for VREF and differential I/O standards except TMDS_33）

i) Analog supply voltage for the GTH transmitter and receiver circuits（$V_{MGTAVCC}$）：-0.5V～1.1V

j) Analog supply voltage for the GTH transmitter and receiver termination circuits（$V_{MGTAVTT}$）：-0.5V～1.32V

k) Auxiliary analog Quad PLL (QPLL) voltage supply for the GTH transceivers（$V_{MGTVCCAUX}$）：-0.5V～1.935V

l) GTH transceiver reference clock absolute input voltage（$V_{MGTREFCLK}$）：-0.5V～1.32V

m) Analog supply voltage for the resistor calibration circuit of the GTH transceiver column（$V_{MGTAVTTRCAL}$）：-0.5V～1.32V

n) Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage（V_{IN}）：-0.5V～1.26V

o) DC input current for receiver input pins DC coupled：

$I_{DCIN-FLOAT}$ =14mA（RX termination = floating）

$I_{DCIN-MGTAVTT}$ =12mA（RX termination =$V_{MGTAVTT}$）

$I_{DCIN-GND}$ =6.5mA（RX termination = GND）

p) DC output current for transmitter pins DC coupled：

$I_{DCOUT-FLOAT}$ =14mA（RX termination = floating）

$I_{DCOUT-MGTAVTT}$ =12mA（RX termination =$V_{MGTAVTT}$）

q) XADC supply relative to GNDADC（V_{CCADC}）：-0.5V～2.0V

r) XADC reference input relative to GNDADC（V_{REFP}）：-0.5V～2.0V

s) Storage temperature（T_{STG}） ：-65℃～150℃

t) Maximum soldering temperature（T_{SOL}）：220℃

u) Maximum junction temperature（T_J）：+125°C

v) Junction-to-case thermal resistance（θ_{JC}）：1℃/W

2.2 Recommended Operating Conditions

a) Internal supply voltage（V_{CCINT}）：0.97V～1.03V

b) Auxiliary supply voltage（V_{CCAUX}）：1.71V～1.89V

c) Auxiliary supply voltage（V_{CCAUX_IO}）：

1.71V～1.89V（Auxiliary supply voltage when set to 1.8V）

1.94V～2.06V（Auxiliary supply voltage when set to 2.0V）

d) Block RAM supply voltage（V_{CCBRAM}）：0.97V～1.03V

e) Supply voltage（V_{CCO}）：1.14V～3.465V（3.3V HR I/O banks）

1.14V～1.89V（1.8V HP I/O banks）

f) I/O input voltage（V_{IN}）：-0.20V～V_{CCO} +0.2V

-0.20V～2.625V（when VCCO = 3.3V for VREF and differential I/O standards except TMDS_33）

g) Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode（I_{IN}）：10mA

h) Battery voltage（V_{CCBATT}）：1.0V～1.89V

i) Analog supply voltage for the GTH transceiver QPLL frequency range（$V_{MGTAVCC}$）：1.02V～1.08V(Under 6.6 Gbps), 1.05V～1.08V(Over 6.6 Gbps)

j) Analog supply voltage for the GTH transmitter and receiver termination circuits（$V_{MGTAVTT}$）：1.17V～1.23V

k) Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers（$V_{MGTVCCAUX}$）：1.75V～1.85V

l) Analog supply voltage for the resistor calibration circuit of the GTH transceiver column（$V_{MGTAVTTRCAL}$）：1.17V～1.23V

m) XADC supply relative to GNDADC（V_{CCADC}）：1.71V～1.89V

n) Externally supplied reference voltage（V_{REFP}）：1.20V～1.30V

o) Junction temperature（TJ）：-55° C～ +125° C

3. Pinout Information and Package

3.1 BQ7VX330TBG1761-PBGA1761

As shown in Figure 3-1, the BQ7VX330TBG1761 device is available in the PBGA1761 packages. Actual column count is 1760.

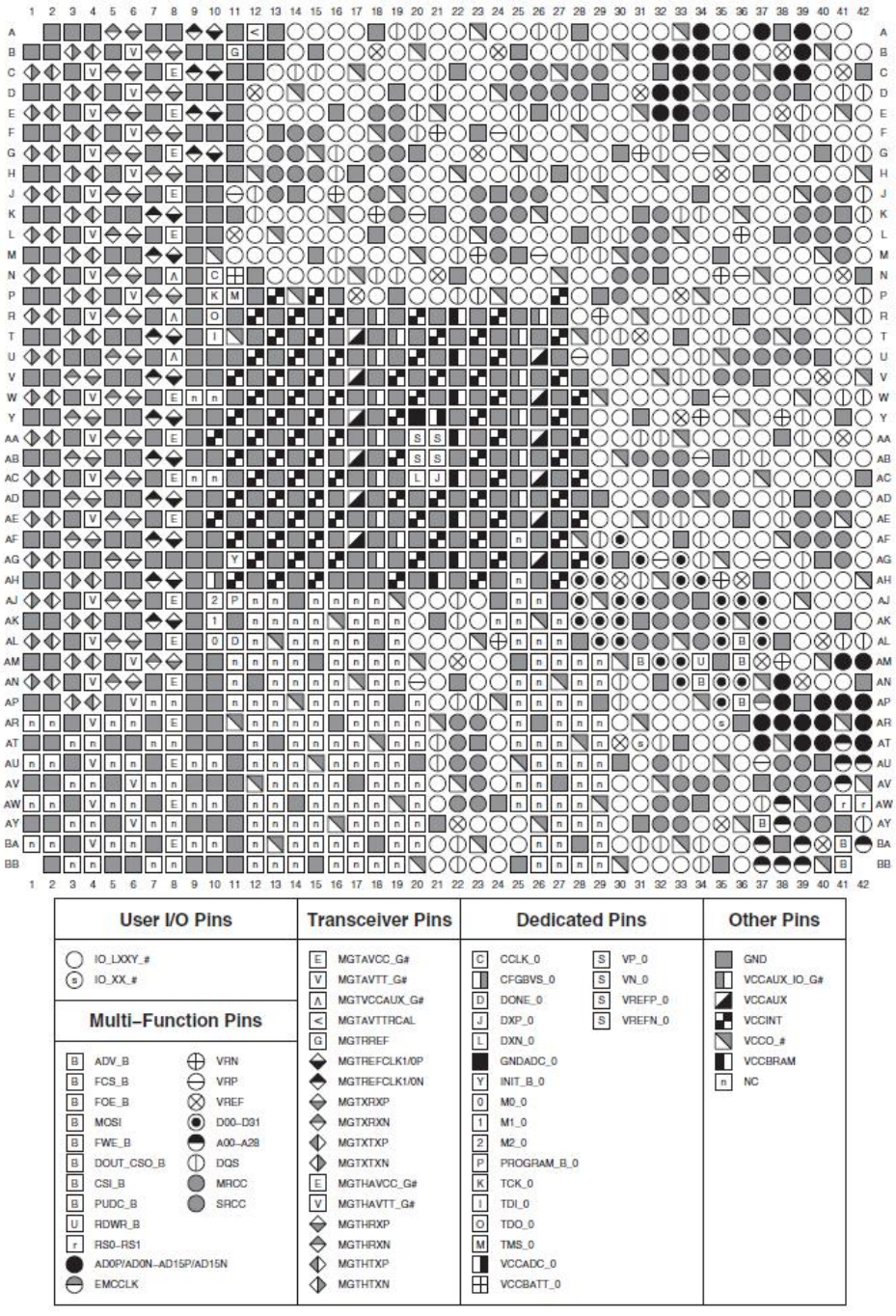
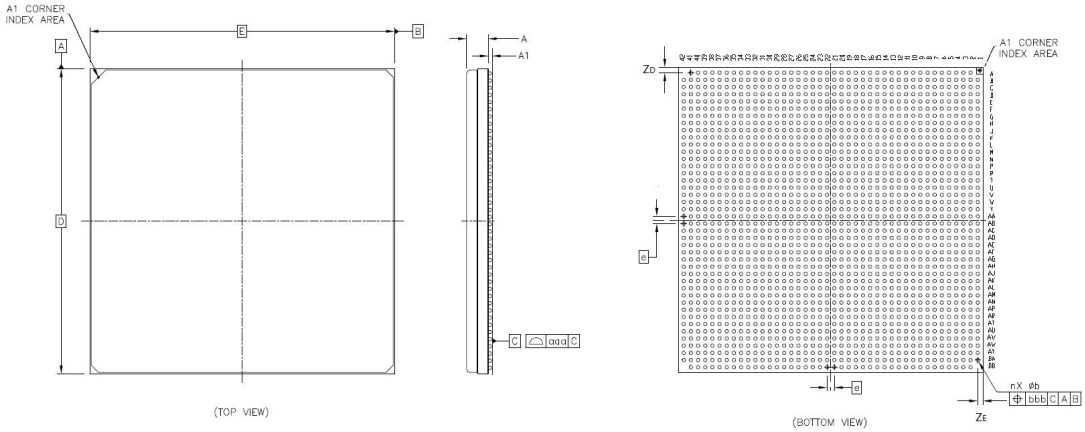


Figure 3-1 BQ7VX330TBG1761-PBGA1761 Pinout Diagram

Figure 3-2 shows the package specifications for BQ7VX330TBG1761-PBGA1761.



symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	4.10
A1	0.4	——	0.6
D/E	42.00	——	43.00
Z_D/Z_E	0.5	——	1.00
e	——	1.00	——
Ø b	0.5	——	0.7
aaa	——	——	0.20
bbb	——	——	0.30

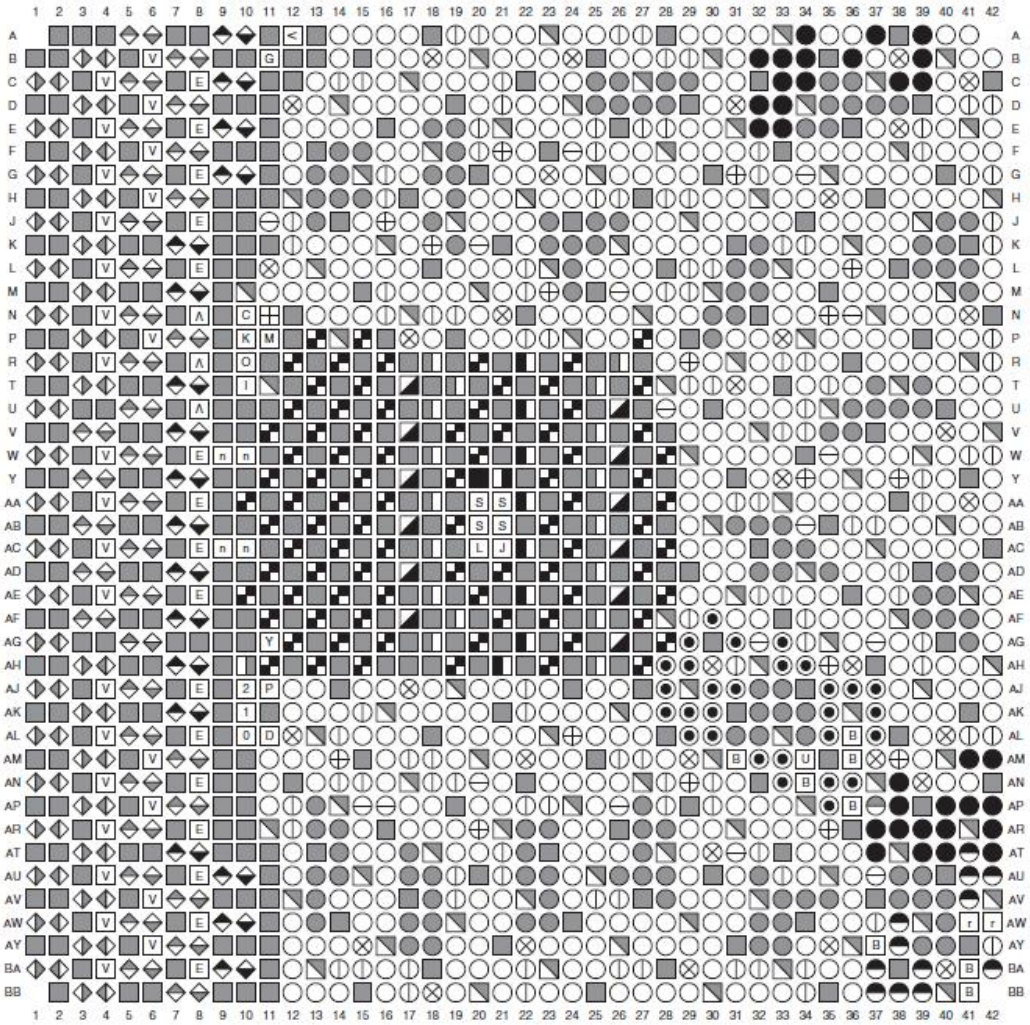
Figure 3-2 Flip-Chip Package Specifications for BQ7VX330T BG1761-PBGA1761

BQ7VX330TBG1761-PBGA1761 pinout list is shown in Appendix II Table 1.

3.2 BQ7VX690TBG1761-PBGA1761

As shown in Figure 3-3, the BQ7VX690TBG1761 device is available in the PBGA1761 packages.

Actual column count is 1760.



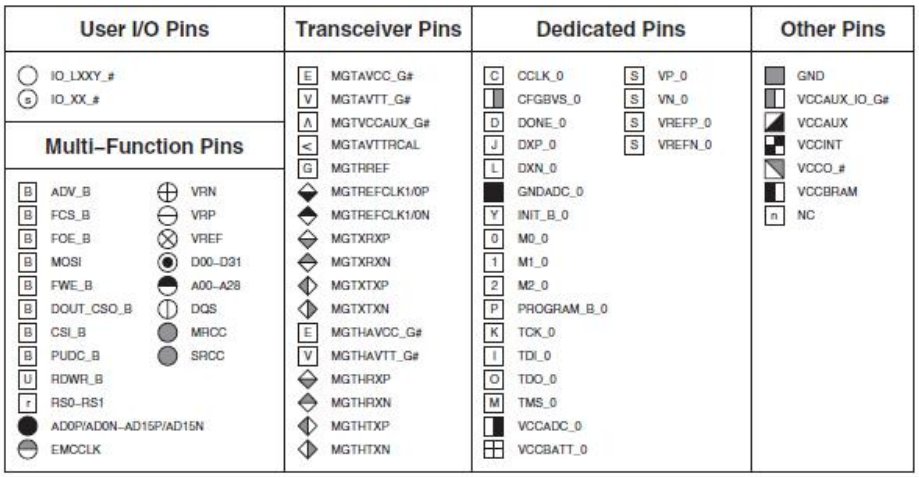
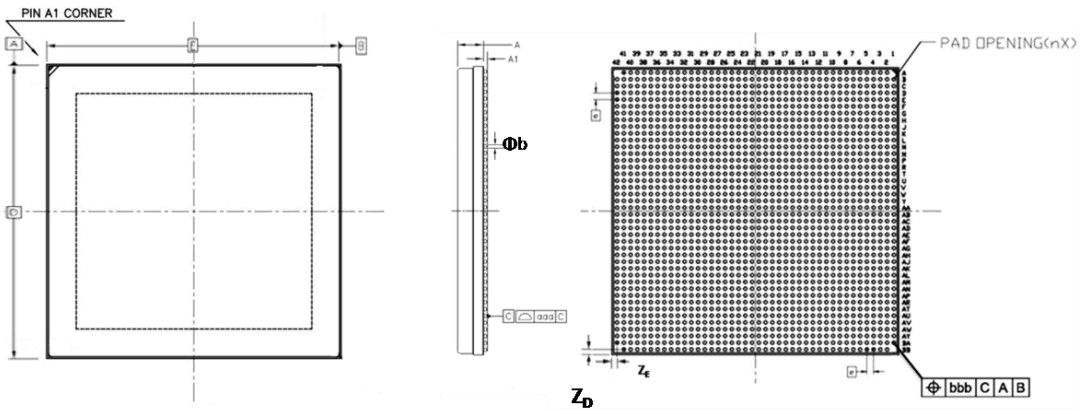


Figure 3-3 BQ7VX690TBG1761-PBGA1761 Pinout Diagram

Figure 3-4 shows the package specifications for BQ7VX690TBG1761-PBGA1761.



symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.68	——	4.00
A1	0.4	——	0.6
D/E	42.00	——	43.00
ZD/ZE	0.5	——	1.00
e	——	1.00	——
Ø b	0.5	——	0.7
aaa	——	——	0.20
bbb	——	——	0.30

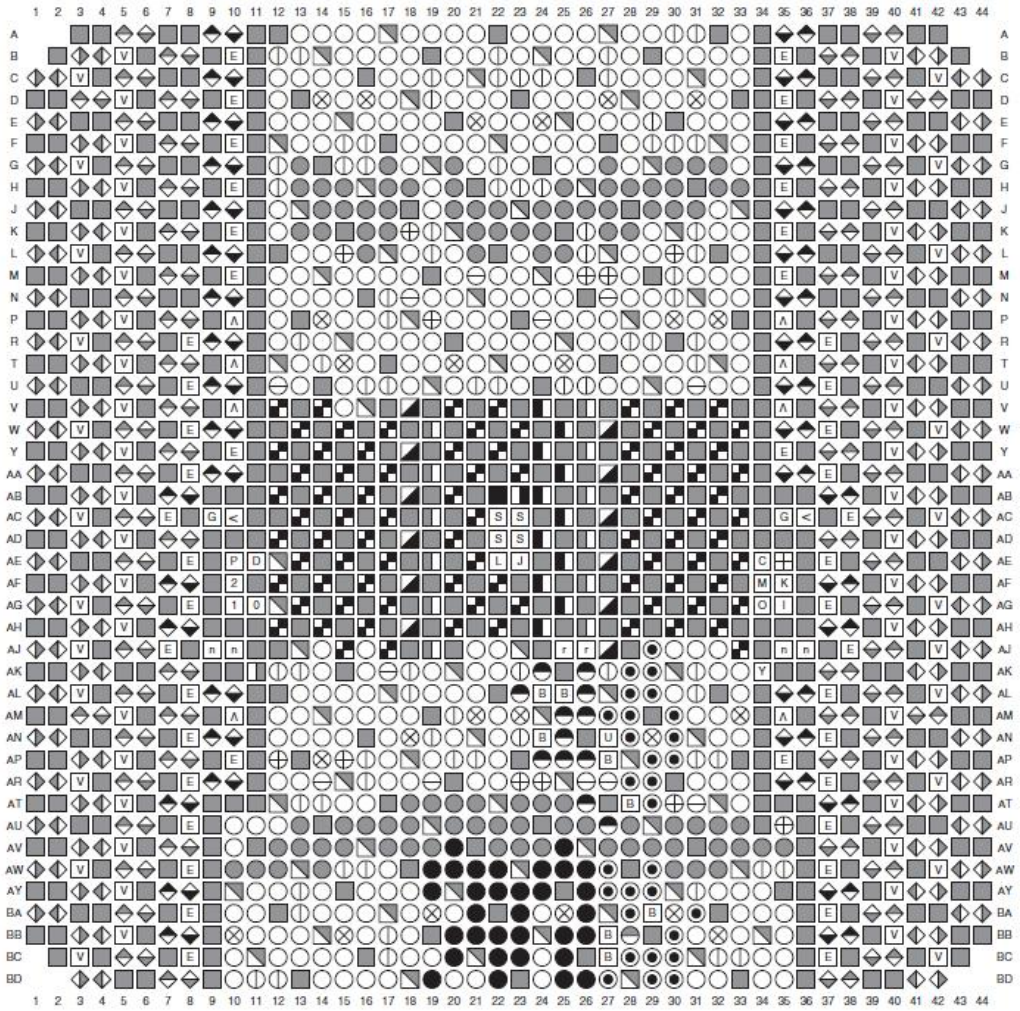
Figure 3-4 Flip-Chip Package Specifications for BQ7VX690TBG1761-PBGA1761

BQ7VX690T-BG1761PBGA1761 pinout list is shown in Appendix II Table 2.

3.3 BQ7VX690TBG1927-PBGA1927

As shown in Figure 3-5, the BQ7VX690TBG1927 device is available in the PBGA1927packages.

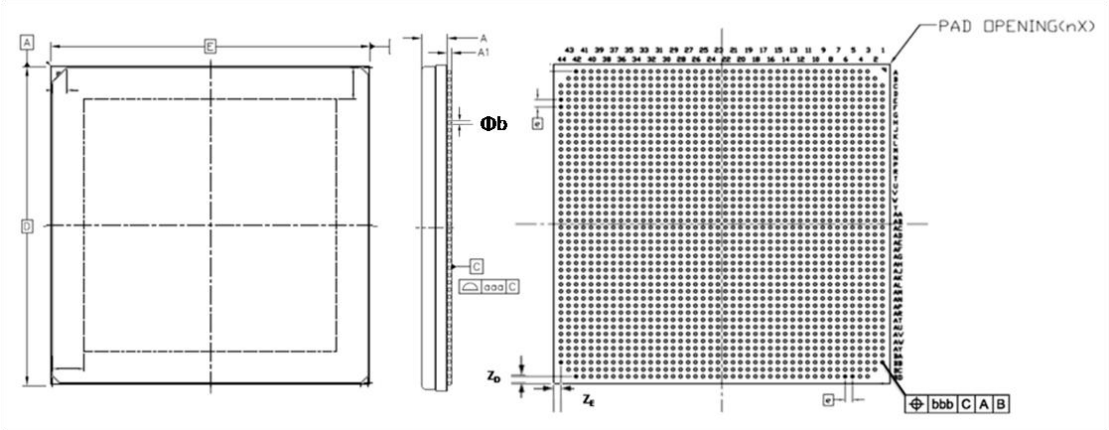
Actual column count is 1924.



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi-Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

Figure 3-5 BQ7VX690TBG1927-PBGA1927 Pinout Diagram

Figure 3-6 shows the package specifications for BQ7VX690TBG1927-PBGA1927.



symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.23	——	3.55
A1	0.4	——	0.6
D/E	44.6	——	45.4
ZD/ZE	0.5	——	1.50
e	——	1.00	——
Ø b	0.5	——	0.7
aaa	——	——	0.20
bbb	——	——	0.30

Figure 3-6 Flip-Chip Package Specifications for BQ7VX690TBG1927-PBGA1927

BQ7VX690TBG1927-PBGA1927 pinout list is shown in Appendix II Table 3.

4. Architecture Features

This section briefly describes BQ7V Series features.

4.1 Input/Output Blocks (SelectIO)

IOBs of BQ7V series FPGAs are programmable and include two types of SelectIO module according to the requirements of different application scenarios: high-performance (HP) and high-range (HR) I/O banks. The HP I/O banks are designed to meet the performance requirements of high-speed memory and other chip-to-chip interfaces with voltages up to 1.8V. The HR I/O banks are designed to support a wider range of I/O standards with voltages up to 3.3V.

Supported Features in the HR and HP I/O Banks：

Feature	HP I/O Banks	HR I/O Banks
3.3V I/O standards	N/A	Supported
2.5V I/O standards	N/A	Supported
1.8V I/O standards	Supported	Supported
1.5V I/O standards	Supported	Supported
1.35V I/O standards	Supported	Supported
1.2V I/O standards	Supported	Supported
LVDS signaling	Supported	Supported
24 mA drive option for LVCMOS18 and LVTTL outputs	N/A	Supported
VCCAUX_IO supply rail	Supported	N/A
Digitally-controlled impedance (DCI) and DCI cascading	Supported	N/A
Internal VREF	Supported	Supported
Internal differential termination (DIFF_TERM)	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	N/A
IDELAYCTRL	Supported	Supported
ISERDES	Supported	Supported
OSERDES	Supported	Supported
ZHOLD_DELAY	N/A	Supported

BQ7V series FPGAs contain following basic I/O logic resources:

- Combinatorial input/output
- 3-state output control
- Registered input/output
- Registered 3-state output control
- Double-Data-Rate (DDR) input/output
- DDR output 3-state control
- IDELAY provides users control of an adjustable, fine-resolution delay taps
- ODELAY provides users control of an adjustable, fine-resolution delay taps

- SAME_EDGE output DDR mode
- SAME_EDGE and SAME_EDGE_PIPELINED input DDR mode

The SelectIO input, output, and 3-state drivers are contained in the input/output buffer (IOB). The HP banks have separate IDELAY and ODELAY blocks. The HR banks have the same logic elements as the HP banks except for the ODELAY block.

More details about SelectIO can be found in Xilinx's official manual UG471: SelectIO Resources.

4.2 Configurable Logic Block(CLB)

A configurable logic block(CLB) of a BQ7V series FPGA is composed of two slices. Each slice contains and is equivalent to:

- Four function generators
- Eight storage elements
- Arithmetic logic gate
- Large multiplexer
- Fast Carry Forward Chain

The function generator can be configured as 6-input LUT or as 5-input with dual-output LUT. The SLICEM in some CLBs can be configured as a 32-bit shift register (or two 16-bit registers) or 64-bit distributed RAM. In addition, the four storage elements can be configured as edge-triggered D-type flip-flops or level-sensitive latches. Each CLB has an internal fast carry chain function and can be connected to a switch matrix that accesses common wiring resources.

A CLB contains two slices, the two slices are located in two independent columns. They have independent carry chains and are not connected to each other. The lower Slice of the CLB is Slice0, and the upper Slice is Slice1 as shown in Figure 4-1.

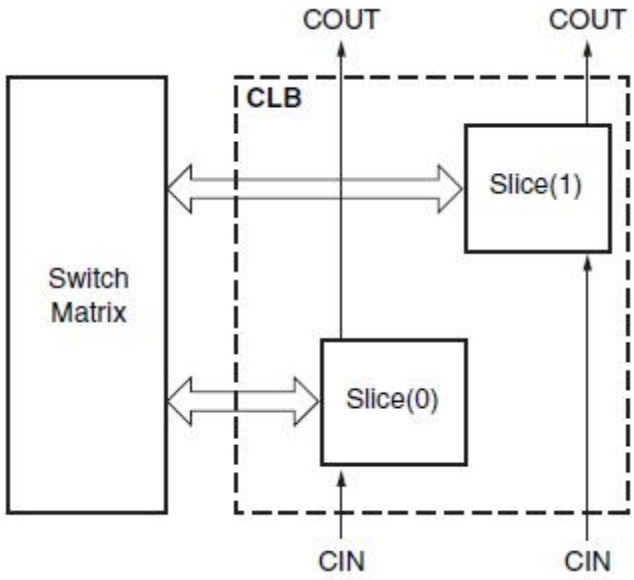


Figure 4-1 Slice in CLB

More details about CLB refer to Xilinx user guide UG474: 7 Series FPGAs Configurable Logic Block User Guide

4.3 Global Clocking

The BQ7V series FPGAs clocking resources manage complex and simple clocking requirements with dedicated global and regional I/O and clocking resources. The clock management tiles (CMT) provide clock frequency synthesis, deskew, and jitter filtering functionality.

The CMT includes a mixed-mode clock manager (MMCM) and a phase-locked loop (PLL). The CMT diagram (Figure 4-2) shows a high-level view of the connection between the various clock input sources and the MMCM/PLL.

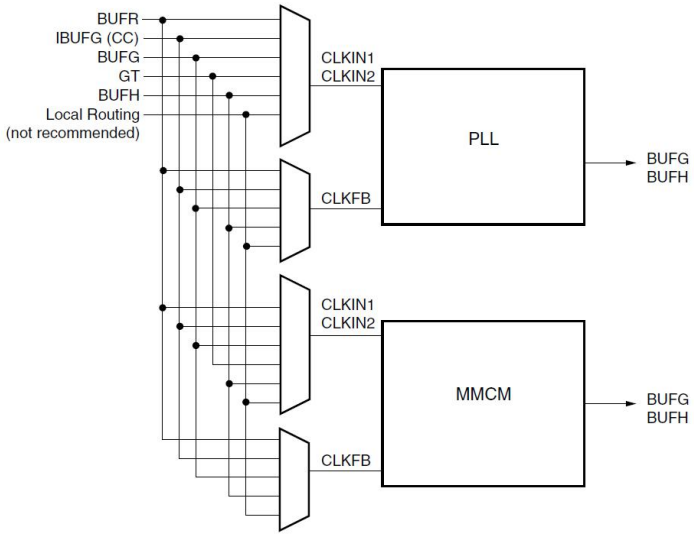


Figure 4-2 Block Diagram of the 7 Series FPGAs CMT

Figure 4-3 shows PLL primitives, detailed PLL block diagram, MMCM primitives and detailed MMCM block diagram. The PLL contains a subset of the MMCM functions. The MMCM supports following additional features:

- Direct HPC to BUFR or BUFIO using CLKOUT[0:3]
- Inverted clock outputs (CLKOUT[0:3]B)
- CLKOUT6
- CLKOUT4_CASCADE
- Fractional divide for CLKOUT0_DIVIDE_F
- Fractional multiply for CLKFBOUT_MULT_F
- Fine phase shifting
- Dynamic phase shifting

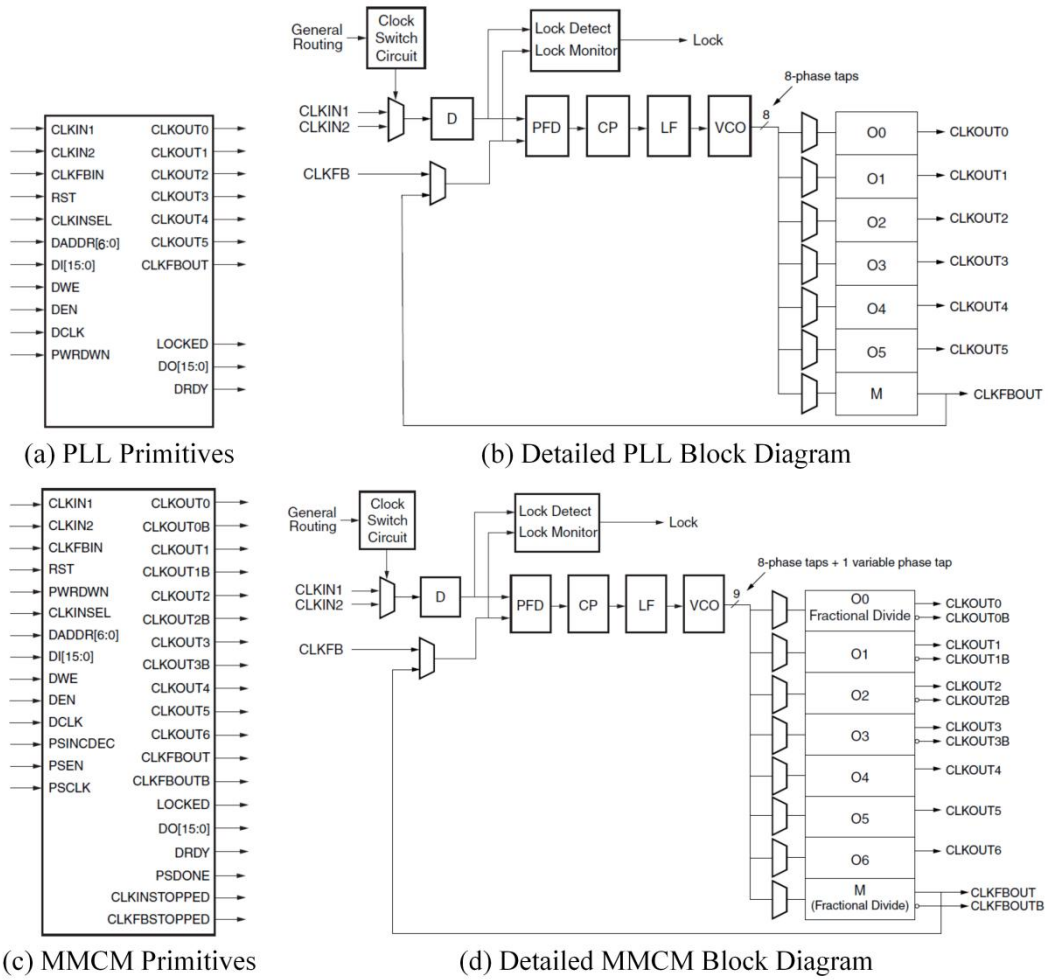


Figure 4-3 PLL Primitives, Detailed PLL Block Diagram, MMCM Primitives and Detailed MMCM Block Diagram

More details about clocking resources can be found in Xilinx's official manual UG472: 7 Series FPGAs Clocking Resources.

4.4 Block RAM

The block RAM stores up to 36 Kbits of data and can be configured as either two independent 18 Kb RAMs, or one 36 Kb RAM. Each 36 Kb block RAM can be configured as a 64K x 1 (when cascaded with an adjacent 36 Kb block RAM), 32K x 1, 16K x 2, 8K x 4, 4K x 9, 2K x 18, 1K x 36, or 512 x 72 in simple dual-port mode. Each 18 Kb block RAM can be configured as a 16K x 1, 8K x 2, 4K x 4, 2K x 9, 1K x 18 or512 x 36 in simple dual-port mode. Power gating is enabled on every 18Kb block which is not instantiated in the design to save power.

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate)

operation increments the internal addresses and provides four handshaking flags: full, empty, almost full, and almost empty. The almost full and almost empty flags are freely programmable.

More details about BRAM refer to Xilinx User Guide UG473：7 Series FPGAs Memory Resources.

4.5 DSP Slice

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. BQ7V series FPGAs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 × 18 bit two's complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

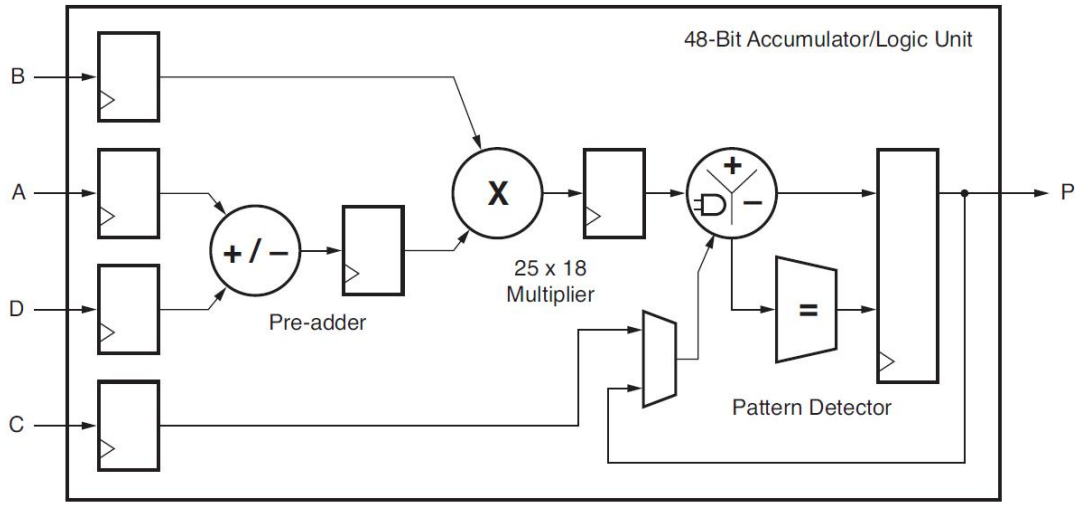


Figure 4-4 Basic Function Diagram of DSP48E1 Slice

More details about DSP refer to Xilinx User Guide UG479: 7 Series DSP48E1 Slice.

4.6 Integrated Block for PCI Express Designs

BQ7V series FPGA include Integrated Block for PCI Express. Highlights of the integrated blocks for PCI Express include：

- Compliant to the PCI Express Base Specification 3.0 with Endpoint and Root Port capability
- Supports Gen1 (2.5 Gb/s), Gen2 (5 Gb/s), and Gen3 (8 Gb/s)

- Advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC (ECRC) Advanced Error

Integrated Block for PCI Express can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 3.0. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom FPGA-to-FPGA communication via the PCI Express protocol. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. The integrated block consists of the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol. Figure 4-5 illustrates the interface block diagram.

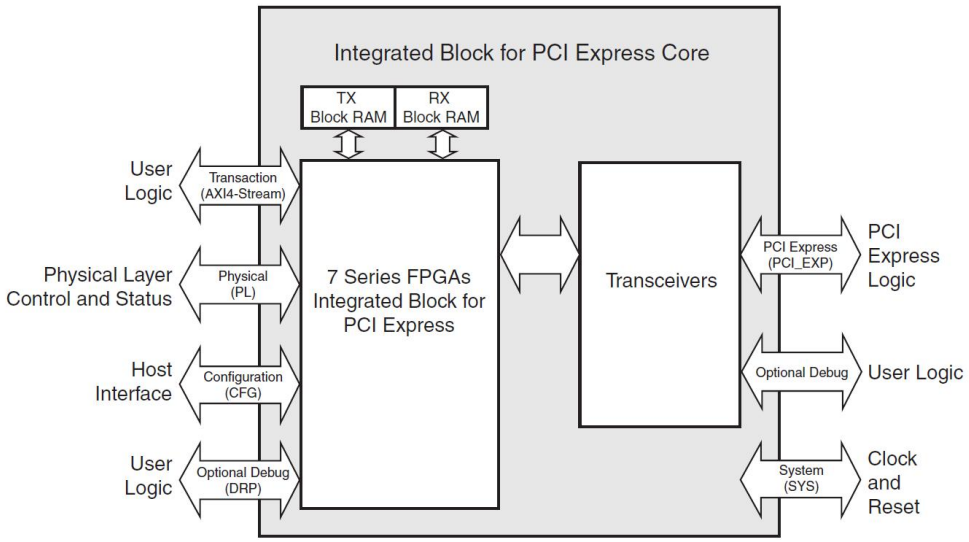


Figure 4-5 Gen3 Integrated Block for PCI Express

More design details refer to Xilinx PG023：Virtex-7 FPGA Gen3 Integrated Block for PCI Express v4.3.

4.7 Boundary Scan

Boundary-Scan instructions and associated data registers support a standard methodology for accessing and configuring BQ7V devices, complying with IEEE standards 1149.1 and 1532.

4.8 RocketIO GTH Transceivers

The GTH transceivers are a low-power and high-efficient four-channel transceivers ,supporting line rates from 500 Mb/s to 8.5 Gb/s. The GTH transceiver supports a variety of high-speed serial communication protocols, including:

- PCI Express Revision 1.1/2.0
- Interlaken
- 10 Gb Attachment Unit Interface (XAUI), Reduced Pin Extended Attachment Unit Interface (RXAUI)
- Common Packet Radio Interface (CPRI)/Open Base Station Architecture Initiative (OBSAI)
- OC-48
- OTU-1

- Serial RapidIO（SRIO）
- Serial Advanced Technology Attachment (SATA)/Serial Attached SCSI (SAS)
- Serial Digital Interface (SDI)

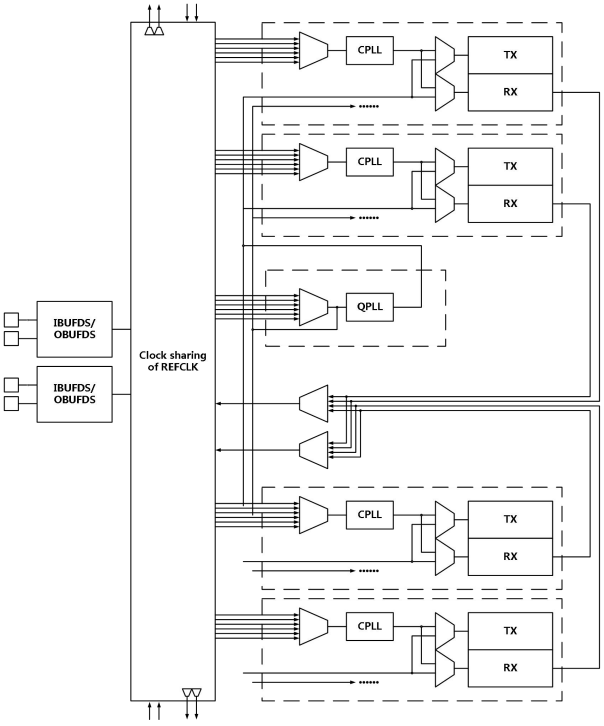


Figure 4-6 Overall Structure of GTH

The overall structure of the GTH lower-power four-channel high-speed serial transceiver is illustrated in Figure 4-6, including four channels and LC VCO phase-locked loop (QPLL). Each high-speed serial transceiver channel contains a transmit (TX) data channel and a receive (RX) data channel, together for realizing data transmit and reception. The channel is embedded with a channel phase-locked loop (CPLL) to realize the internal clock of a single channel management. The QPLL provides high-frequency and low-jitter reference clocks for four-channels.

The overall structure of GTH transceiver consists of two parts: the shared part and the data path. The shared part includes the QPLL, band-gap reference source, and terminal impedance calibration module. The data path part includes the transmit data path and the receiver data path. The transmit data path performs channel coding on the input parallel data. After PISO and pre-emphasis processing, it is output as a high-speed differential serial signal. In the receiving data path, the high-speed differential serial signal is converted into parallel data after signal equalization processing, clock and data recovery. After channel decoding, clock correction, channel alignment and other operations, it is transmitted to the FPGA internal logic in parallel data.

More details about rocketIO GTX transceivers can be found in Xilinx’s official manual UG476: 7 Series FPGAs GTX/GTH Transceivers.

4.9 XADC

The XADC is available in all BQ7V series FPGA devices. The XADC includes a dual 12-bit (for temperature range -40℃-100℃, 10-bit when temperature range is -55℃-125℃), 1 Mega sample per second(MSPS) ADC and on-chip sensors. By combining XADC with programmable logic, it is possible to craft customized analog interfaces for a wide range of applications. Most commonly used XADC functions are: 1) Sets up a predefined operating mode and a number of channels, the XADC automatically selects the channel for conversion and stores the results in the status registers based on the setting; 2) The XADC provides a digital averaging function that allows a user to average up to 256 individual measurements to produce a reading. Averaging the sensor measurements helps generate a noise-free measurement; 3) The XADC can be set to automatically generate alarm outputs when the defined operating ranges for the FPGA supply voltages and temperature are exceeded.

Figure 4-7 shows a block diagram of the XADC. The XADC is built around a dual 12-bit(for temperature range -40 ℃ -100℃, 10-bit when temperature range is -55 ℃ -125 ℃), 1MSPS Analog-to-Digital Converter (ADC). When combined with a number of on-chip sensors, the XADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures. Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 users-electable analog inputs, known as auxiliary analog inputs (VAUXP[15:0], VAUXN[15:0]). Apart from a single dedicated analog input pair (VP/VN), the external analog inputs use dual-purpose I/O.

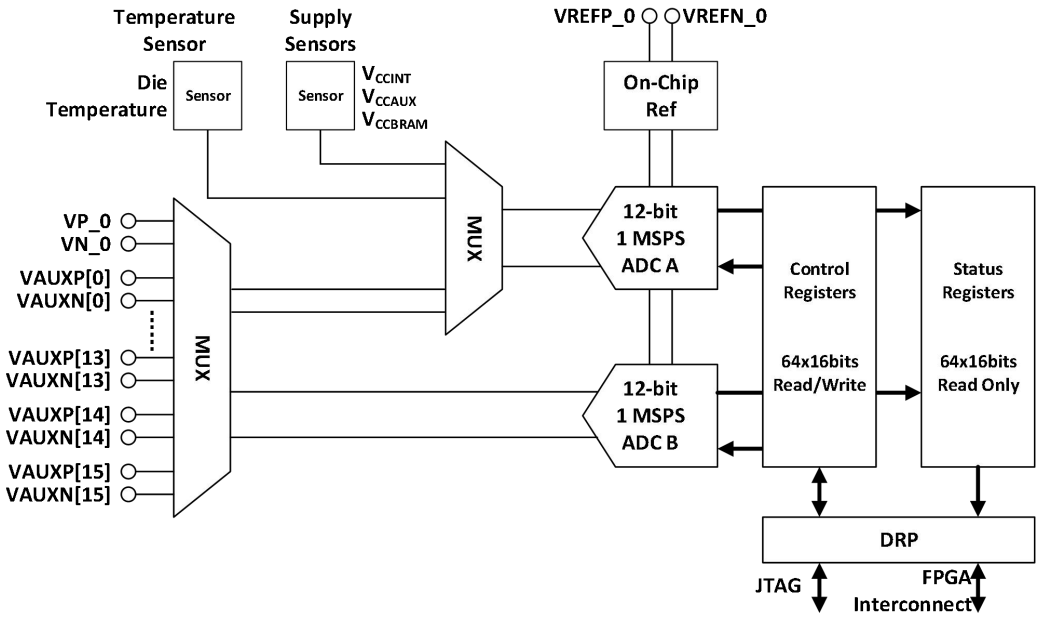


Figure 4-7 XADC Block Diagram

The XADC accommodates both unipolar and bipolar signals. The ADC conversion data is stored in dedicated registers called status registers. These registers are accessible via the FPGA interconnect using a 16-bit synchronous read and write port called the Dynamic Reconfiguration Port (DRP). ADC conversion data is also accessible via the JTAG TAP. In the latter case, users are not required to instantiate the XADC. If the XADC is not instantiated in a design, the device operates in a predefined mode (called default mode) that monitors on-chip temperature and supply voltages.

Control registers are used to configure the XADC operation. All XADC functionality is controlled through these registers. These control registers are initialized using the XADC attributes when the XADC is instantiated in a design. The configuration registers can be modified through the DRP after the FPGA has been configured.

The read-only status registers contain the results of an analog-to-digital conversion of the on-chip sensors and external analog channels. The status registers also store the maximum and minimum measurements recorded for the on-chip sensors from the device power-up or the last user reset of the XADC. At the end of an ADC conversion when the measurement is written to the status registers EOC (End of Conversion) or EOS (End of Sequence) signals transition to active High.

When the die temperature exceeds a factory set limit of 125°C or a user-defined threshold in Control Register, the Over-Temperature alarm logic output (OT) becomes active. The OT signal resets when the FPGA temperature has fallen below 70°C or a user-programmable limit in Control Register. When the automatic power-down feature is enabled, the OT signal can be used to trigger a device power down. When OT goes High, the FPGA enters power down mode which initiates a configuration shutdown sequence, disabling the device and asserts GHIGH to prevent any contention. When OT is de-asserted, GHIGH is de-asserted and the start-up sequence is initiated releasing all global resources.

For more details on XADC see UG480: Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide.

4.10 Configuration

BQ7V devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode

- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE-1532 and -1149)
- SPI mode (Serial Peripheral Interface standard Flash)
- BPI-up modes (Byte-wide Peripheral interface standard x8 or x16 NOR Flash)

In addition, BQ7V devices also support the following configuration options:

- Partial reconfiguration
- Built-in SEU detection and correction
- Built-in MultiBoot and safe-update capability
- 256-bit AES encryption with HMAC/SHA-256 authentication
- Parallel configuration bus width auto-detection

The configuration banks voltage select pin (CFGBVS) determines the I/O voltage operating range and voltage tolerance for the dedicated configuration bank0. If the VCCO_0 supply for bank 0 is supplied with 2.5V or 3.3V, then the CFGBVS pin must be tied High. Tie CFGBVS to Low, only if the VCCO_0 for bank0 is less than or equal to 1.8V.

For detailed information on usage of Configuration, see ug470. BQ7V have five configuration interfaces. Each configuration interface corresponds to one or more configuration modes and bus width, shown in Table 4-1.

Table 4-1 BQ7V Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1,2,4	Output
Master BPI	010	8,16	Output
Master SelectMAP	100	8,16	Output
JTAG	101	1	Not Applicable
Slave SelectMAP	110	8,16,32	Input
Slave Serial	111	1	Input

4.10.1 Serial Configuration Interface

In serial configuration modes, the FPGA is configured by loading one configuration bit per CCLK

cycle:

- In Master Serial mode, CCLK is an output.
- In Slave Serial mode, CCLK is an input.

Figure 4-8 shows the basic BQ7V serial configuration interface. There are four methods of configuring an FPGA in serial mode:

- Master serial configuration
- Slave serial configuration
- Serial daisy-chain configuration
- Ganged serial configuration

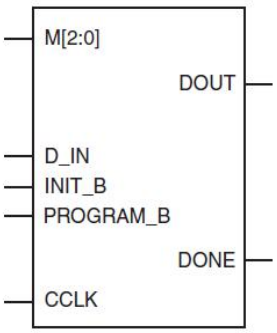


Figure 4-8 BQ7V FPGA Serial Configuration Interface

Table 4-2 BQ7V FPGA Serial Configuration Interface Pins

Pin Name	Direction	Type	Description
M[2:0]	Input	Dedicated	M[2:0] determine the configuration mode M[2:0] = 000：Master Serial Configuration； M[2:0] = 111：Slave Serial Configuration。
CCLK	Input or Output	Dedicated	CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode.
DIN	Input	Multi-function	DIN is the serial data input pin. By default, data from DIN is captured on the rising edge of CCLK.
DONE	Bidirectional	Dedicated	A High signal on the DONE pin indicates completion of the configuration sequence.
INIT_B	Bidirectional (open-drain)	Dedicated	Active-Low FPGA initialization pin or configuration error signal. Upon completing the FPGA initialization process, INIT_B is released to high-Z at which time an external resistor is expected to pull INIT_B High.

PROGRAM_B	Input	Dedicated	Active-Low reset to configuration logic
DOUT	Output	Multi-function	DOUT is the data output for a serial configuration daisy-chain.
PUDC_B	Input	Multi-function	Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. PUDC_B must be tied either directly, or via a ≤1 kΩ to VCCO_14 or GND. ***Caution!*** Do not allow this pin to float before and during configuration.

Slave Serial Configuration

Slave serial configuration is typically used for devices in a serial daisy chain or when configuring a single device from an external microprocessor or CPLD (See Figure 4-9). Design considerations are similar to Master serial configuration except for the direction of CCLK. CCLK must be driven from an external clock source.

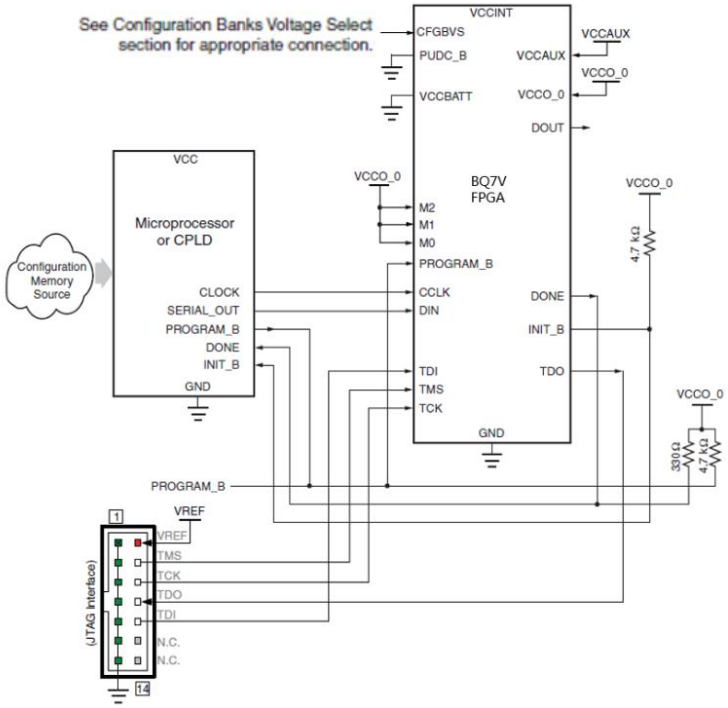


Figure 4-9 Slave Serial Mode Configuration Example

Master Serial Configuration

The Master Serial configuration mode is the same as the Slave Serial configuration mode, except that the FPGA generates the CCLK. That is, the CCLK is an output in Master serial mode.

Serial Daisy Chains

Multiple BQ7V devices can be configured from a single configuration source by arranging the devices in a serial daisy chain. In a serial daisy chain, devices receive their configuration data through

their D_IN pin, passing configuration data along to downstream devices through their DOUT pin. The device closest to the configuration data source is considered the most upstream device, while the device furthest from the configuration data source is considered the most downstream device.

In a serial daisy chain, the configuration clock is typically provided by the most upstream device in Master serial mode. All other devices are set for Slave serial mode. Figure 4-10 illustrates this configuration.

Another alternative is to use SPI mode for the first device. The daisy chain data is still sent out through DOUT in SPI mode.

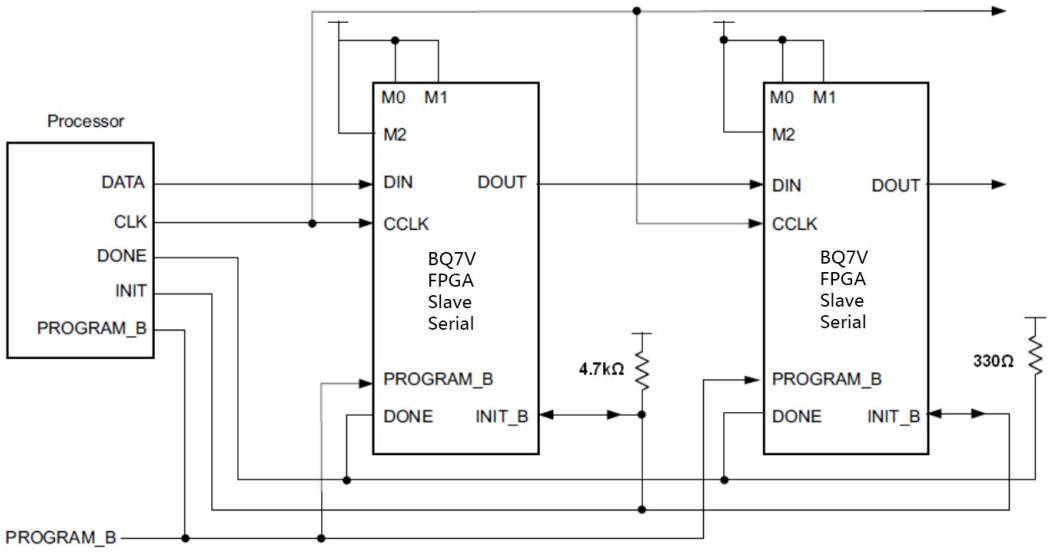


Figure 4-10 Master/Slave Serial Mode Daisy Chain Configuration

The first device in a serial daisy chain is the last to be configured. CRC only checks the data for the current device, not for any others in the chain.

It is important that all DONE pins in a Slave serial daisy chain be connected. Only the first device in the serial daisy chain should have the DONE active pull-up driver enabled. Enabling the DONE driver on downstream devices causes contention on the DONE signal.

Mixed Serial Daisy Chains

BQ7V devices can be daisy-chained with BMTI BQ2V、BQR2V、BQ5V、BQR5V and the Xilinx Virtex/Spartan families. There are three important design considerations when designing a mixed serial daisy chain:

- Many older FPGA devices cannot accept as fast a CCLK frequency as a BQ7V device can generate. Select a configuration CCLK speed supported by all devices in the chain.
- BQ7V devices should always be at the beginning of the serial daisy chain, with older family

devices located at the end of the chain.

- All BMTI device families have similar BitGen options. The guidelines provided for BQ7V BitGen options should be applied to all BMTI devices in a serial daisy chain.
- The number of configuration bits that a device can pass through its DOUT pin is limited. This limit varies for different families (Table 4-2). The sum of the bitstream lengths for all downstream devices must not exceed the number in Table 4-3 for each family.

Table 4-3 Maximum Number of Configuration Bits, Various Device Families

Architecture	Maximum DOUT Bits
BQ2V、BQR2V、BQ5V、BQR5V	4,294,967,264

Ganged Serial Configuration

More than one device can be configured simultaneously from the same bitstream using a ganged serial configuration setup (Figure 4-11). In this arrangement, the serial configuration pins are tied together such that each device sees the same signal transitions. One device is typically set for Master serial mode (to drive CCLK) while the others are set for Slave serial mode. For ganged serial configuration, all devices must be identical. Configuration can be driven from a configuration PROM or from an external configuration controller.

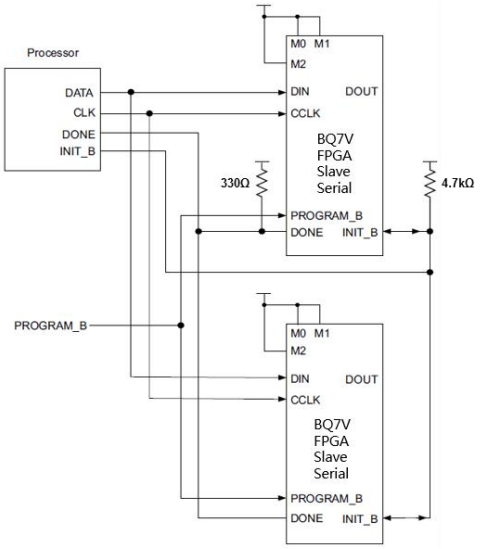


Figure 4-11 Ganged Serial Configuration

4.10.2 SelectMAP Configuration Interface

The SelectMAP configuration interface (Figure 4-12) provides an 8-bit, 16-bit, or 32-bit bidirectional data bus interface to the BQ7V configuration logic which can be used for both configuration and

readback. The bus width of SelectMAP is automatically detected. CCLK is an output in Master SelectMAP mode; in Slave SelectMAP mode, CCLK is an input.

There are four methods of configuring an FPGA in SelectMAP mode:

- Single device Master SelectMAP
- Single device Slave SelectMAP
- Multiple device SelectMAP bus
- Multiple device ganged SelectMAP

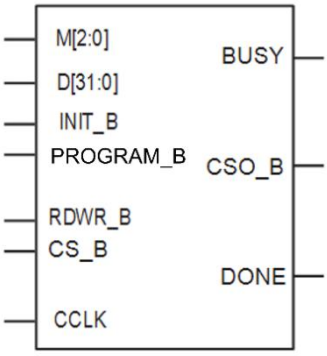


Figure 4-12 BQ7V Device SelectMAP Configuration Interface

Table 4-4 describes the SelectMAP configuration interface.

Table 4-4 BQ7V Device SelectMAP Configuration Interface Pins

Pin Name	Type	Dedicated or Dual-Purpose	Description
M[2:0]	Input	Dedicated	Mode pins - determine configuration mode
CCLK	Input and Output	Dedicated	Configuration clock source for all configuration modes except JTAG
D[31:0]	Three-State Bidirectional	Dual-Purpose	Configuration and readback data bus, clocked on the rising edge of CCLK.
DONE	Bidirectional, Open-Drain or active	Dedicated	Active-High signal indicating configuration is complete: 0= FPGA not configured 1= FPGA configured
INIT_B	Input or Output, Open-Drain	Dedicated	Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration. After the Mode pins are sampled, INIT_B is an open-drain, active-Low output indicating whether a CRC error occurred during configuration: 0= CRC error 1= No CRC error

			When the SEU detection function is enabled, INIT_B is optionally driven Low when a read back CRC error is detected.
PROGRAM_B	Input	Dedicated	Active-Low asynchronous full-chip reset.
CSI_B	Input	Dedicated	Active-Low chip select to enable the SelectMAP data bus (see "SelectMAP Data Loading"): 0= SelectMAP data bus enabled 1= SelectMAP data bus disabled
RDWR_B	Input	Dedicated	Determines the direction of the D[x:0] data bus (see "SelectMAP Data Loading"): 0= inputs 1= outputs RDWR_B input can only be changed while CS_B is deasserted, otherwise an ABORT occurs (see "SelectMAP ABORT").
CSO_B	Output	Dual-Purpose	Parallel daisy chain active-Low chip select output. Not used in single FPGA applications.
RS[1:0]	Output	Dual-Purpose	RS0 and RS1 are high-Z during configuration. However, the FPGA can drive the RS0 and RS1 pins under two possible conditions. When the ConfigFallback option is enabled, the FPGA drives RS0 and RS1 Low during the fallback configuration process that follows a detected configuration error. When a user-invoked MultiBoot configuration is initiated, the FPGA can drive the RS0 and RS1 pins to a user-defined state during the MultiBoot configuration process. If fallback is disabled (default) and if MultiBoot is not used, or if SPI mode is used, then RS0 and RS1 are high-Z and can be left unconnected.
PUDC_B	Input	Multi-function	Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. PUDC_B must be tied either directly, or via a ≤1 kΩ to VCCO_14 or GND. ***Caution!*** Do not allow this pin to float before and during configuration.

Single Device SelectMAP Configuration

For custom applications where a microprocessor or CPLD is used to configure a single BQ7V FPGA device, either Master SelectMAP mode (use CCLK from the FPGA) or Slave SelectMAP mode can be used (Figure 4-13). Slave SelectMAP mode is preferred.

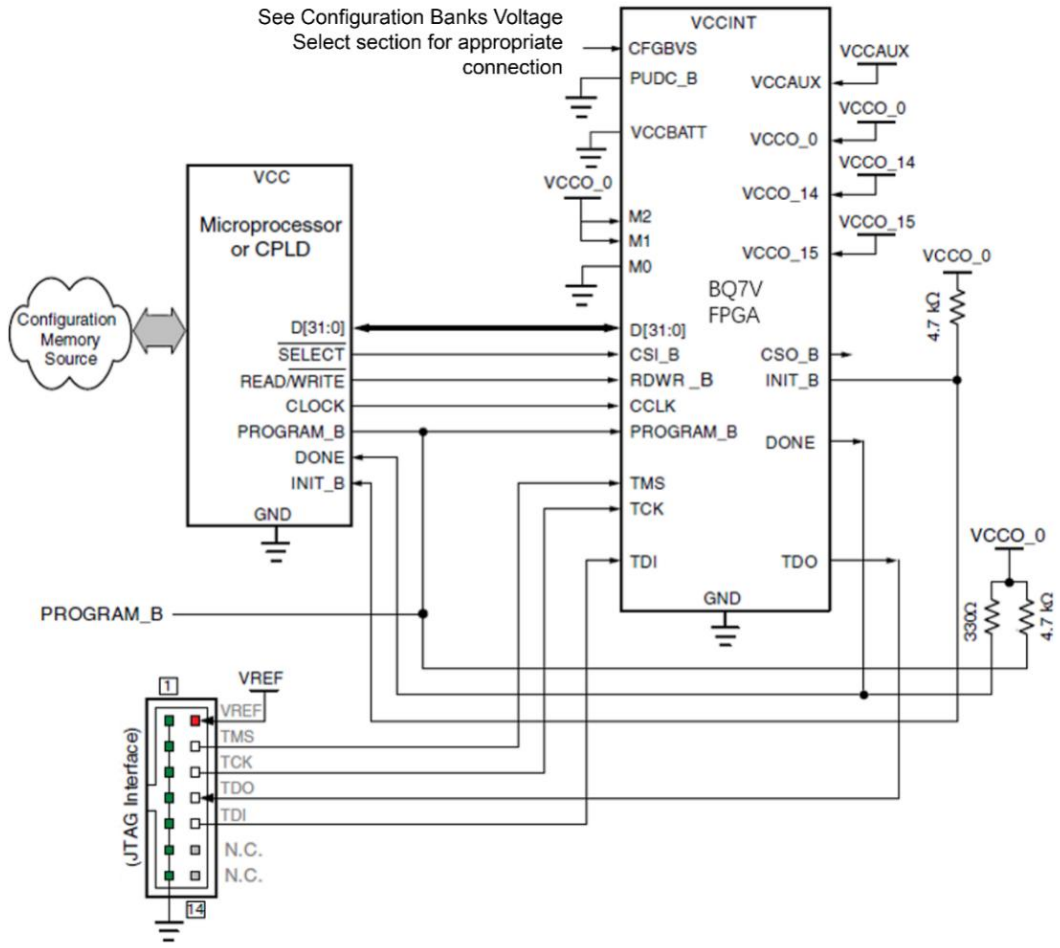


Figure 4-13 Single Slave Device SelectMAP Configuration from Microprocessor or CPLD Example

Multiple Device SelectMAP Configuration

Multiple BQ7V devices in Slave SelectMAP mode can be connected on a common SelectMAP bus (Figure 4-14). In a SelectMAP bus, the DATA, CCLK, RDWR_B, BUSY, PROGRAM_B, DONE, and INIT_B pins share a common connection between all of the devices. To allow each device to be accessed individually, the CSI_B (Chip Select) inputs must not be tied together. External control of the CSI_B signal is required and is usually provided by a microprocessor or CPLD.

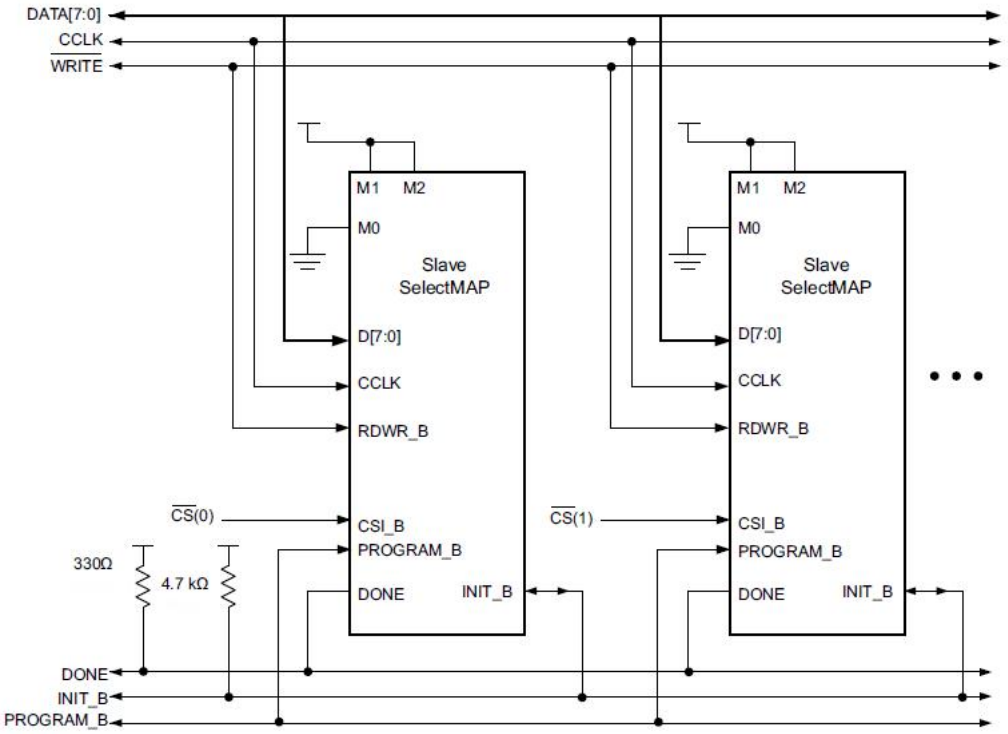


Figure 4-14 Multiple Slave Device Configuration on an 8-Bit SelectMAP Bus

Parallel Daisy Chain

BQ7V FPGA configuration supports parallel daisy-chain. Figure 4-15 shows an example schematic of the leading device in BPI mode. The leading device can also be in Master or Slave SelectMAP modes. The D, CCLK, RDWR_B, PROGRAM_B, DONE, and INIT_B pins share a common connection between all of the devices. The CSI_B pins are daisy chained.

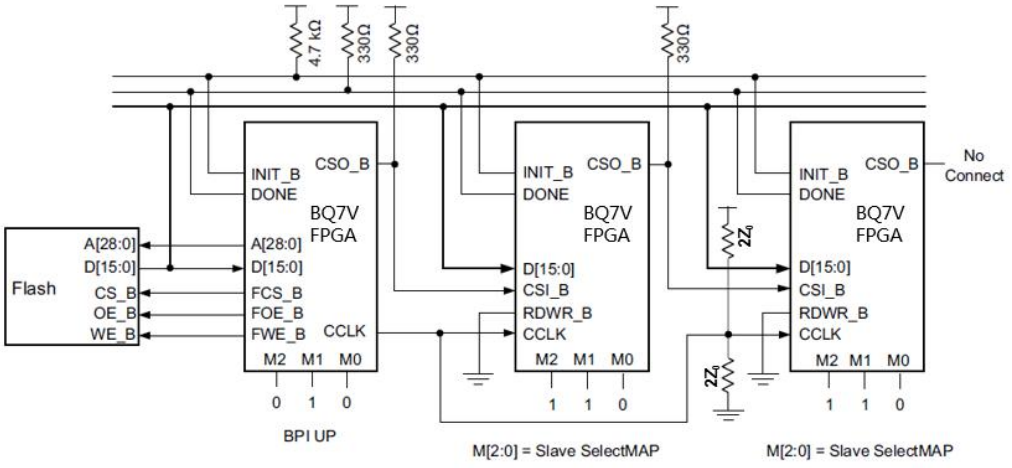


Figure 4-15 Parallel Daisy Chain

Within Figure 4-15, Z_0 is the characteristic impedance of CCLK transmission line.

Ganged SelectMAP

It is also possible to configure multiple devices simultaneously with the same configuration bitstream by using a ganged SelectMAP configuration. In a ganged SelectMAP arrangement, the CSI_B pins of two or more devices are connected together (or tied to ground), causing all devices to recognize data presented on the D pins. All devices can be set for Slave SelectMAP mode if an external oscillator is available, or one device can be designated as the Master device, as illustrated in Figure 4-16.

An external pull-up resistor is required on the common DONE signal. Designers must carefully focus on signal integrity due to the increased fanout. Signal integrity simulation is recommended.

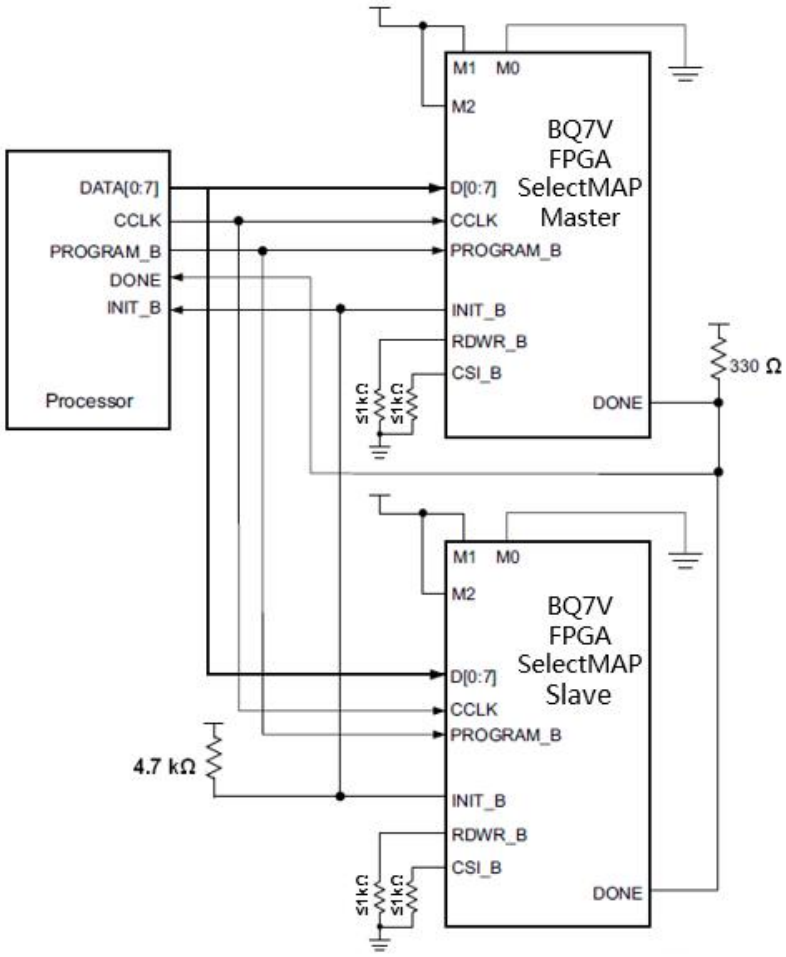


Figure 4-16 Ganged x8 SelectMAP Configuration

SelectMAP Data Loading

The SelectMAP interface allows for either continuous or non-continuous data loading. Data loading is controlled by the CSI_B, RDWR_B, CCLK, and BUSY signals.

CSI_B

The Chip Select input (CSI_B) enables the SelectMAP bus. When CSI_B is High, the 7 series device ignores the SelectMAP interface, neither registering any inputs nor driving any outputs. The D[31:0] pins are placed in a High-Z state, and RDWR_B is ignored.

- If CSI_B = 0, the device's SelectMAP interface is enabled.
- If CSI_B = 1, the device's SelectMAP interface is disabled.

If only one device is being configured through the SelectMAP and readback is not required, the CSI_B signal can be tied to ground.

RDWR_B

RDWR_B is an input to the BQ7V device that controls whether the data pins are inputs or outputs:

- If RDWR_B = 0, the data pins are inputs (writing to the FPGA).
- If RDWR_B = 1, the data pins are outputs (reading from the FPGA).

For configuration, RDWR_B must be set for write control (RDWR_B = 0). For readback, RDWR_B must be set for read control (RDWR_B = 1) while CSI_B is asserted.

Changing the value of RDWR_B from High to Low while CSI_B is Low also triggers an ABORT, and the configuration I/O changes from output to input asynchronously with no ABORT status readback. If readback is not needed, RDWR_B can be tied to ground or used for debugging with SelectMAP ABORT.

CCLK

All activity on the SelectMAP data bus is synchronous to CCLK. When RDWR_B is set for write control (RDWR_B = 0, Configuration), the FPGA samples the SelectMAP data pins on rising CCLK edges. When RDWR_B is set for read control (RDWR_B = 1, Readback), the FPGA updates the SelectMAP data pins on rising CCLK edges.

In Slave SelectMAP mode, configuration can be paused by stopping CCLK.

SelectMAP ABORT

In monolithic devices an ABORT is an interruption in the SelectMAP configuration or readback sequence occurring when the state of RDWR_B changes while CSI_B is asserted as sampled by CCLK. During a configuration ABORT, internal status is driven onto the D[04:07] pins over the next four CCLK cycles. The other D pins are always High. After the ABORT sequence finishes, the user can

resynchronize the configuration logic and resume configuration.

ABORT Status Word

During the configuration ABORT sequence, the device drives a status word onto the D[00:07] pins. The status bits do not bit-swap. The other data pins are always High. The key for the status word is given in Table 4-5.

Table 4-5 ABORT Status Word

Bit Number	Status Bit Name	Meaning
D07	CFGERR_B	Configuration error (active Low) 0 = A configuration error has occurred. 1 = No configuration error.
D06	DALIGN	Sync word received (active High) 0 = No sync word received. 1 = Sync word received by interface logic.
D05	RIP	Readback in progress (active High) 0 = No readback in progress. 1 = A readback is in progress.
D04	IN_ABORT_B	ABORT in progress (active Low) 0 = Abort is in progress. 1 = No abort in progress.
D03-D02	RSVD	Reserved
D01-D00	11	Fixed to ones.

There are two ways to resume configuration or readback after an ABORT:

- The device can be resynchronized after the ABORT completes.
- The device can be reset by pulsing PROGRAM_B Low at any time.

4.10.3 SPI Configuration Interface

In SPI serial Flash mode, M[2:0]=001. The BQ7V FPGA configures itself from an attached industry-standard SPI serial Flash PROM. Although SPI is a standard four-wire interface, various available SPI Flash memories use different read commands and protocol. Besides M[2:0], FS[2:0] pins are sampled by the INIT_B rising edge to determine the type of read commands used by SPI Flash. For BQ7V FPGA configurations, the default address always starts from 0. Figure 4-17 shows the SPI related configuration pins, and the standard connection between BQ7V devices and SPI Flash.

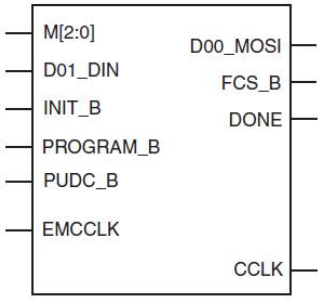


Figure 4-17 BQ7V Device SPI Configuration Interface

Table 4-6 describes the SPI configuration interface pins.

Table 4-6: BQ7V Device SPI Configuration Interface Pins

Pin Name	Type	Dedicated or Dual-Purpose	Description
M[2:0]	Input	Dedicated	Mode pins – 001for SPI
D01_DIN	Bidirectional	Dual-Purpose	DIN is the serial data input pin. By default, data from DIN is captured on the rising edge of CCLK.
CCLK	Output	Dedicated	Configuration clock output (to SPI).
D00_MOSI	Bidirectional	Dual-Purpose	FPGA (master) SPI mode output for sending commands to the SPI (slave) flash device.
DONE	Bidirectional	Dedicated	A High signal on the DONE pin indicates completion of the configuration sequence.
INIT_B	Input or Output, Open-Drain	Dedicated	Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration. After the Mode pins are sampled, INIT_B is an open-drain active Low output indicating whether a CRC error occurred during configuration: 0= CRC error 1= No CRC error When the SEU detection function is enabled, INIT_B is optionally driven Low when read back CRC error is detected.
PROGRAM_B	Input	Dedicated	Active-Low asynchronous full-chip reset
FCS_B	Output	Dual-Purpose	Active-Low chip select output, clocked by the CCLK falling edge.
EMCCLK	Input	Dual-Purpose	Optional external clock input for running the configuration logic in a master mode (versus the internal configuration oscillator).
PUDC_B	Input	Multi-function	Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after

			power-up and during configuration. PUDC_B must be tied either directly, or via a ≤1 kΩ to VCCO_14 or GND. ***Caution!*** Do not allow this pin to float before and during configuration.

Figure 4-18 shows the connections for a SPI configuration with a x1 or x2 data width. These connections are the same because the x2 mode uses the D00_MOSI pin as a dual-purpose Data In/Out pin. Daisy-chained configuration mode is only available in SPI.

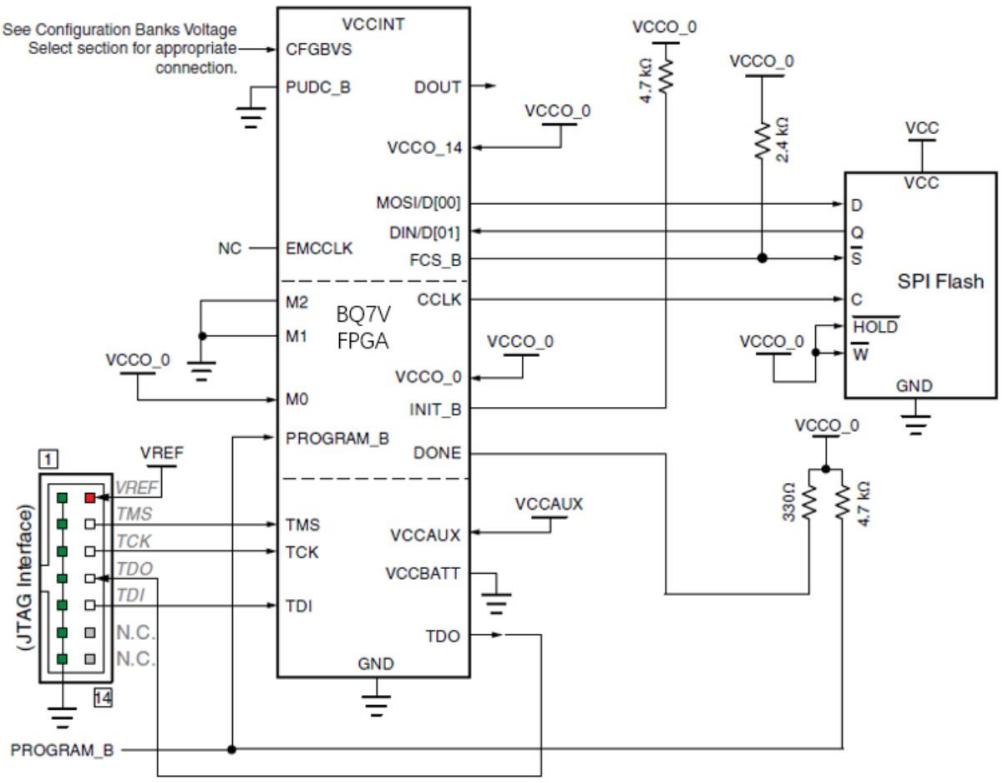


Figure 4-18 SPI x1/x2 Configuration Interface

BQ7V FPGA supports a x4 quad SPI master configuration width as shown in Figure 4-19.

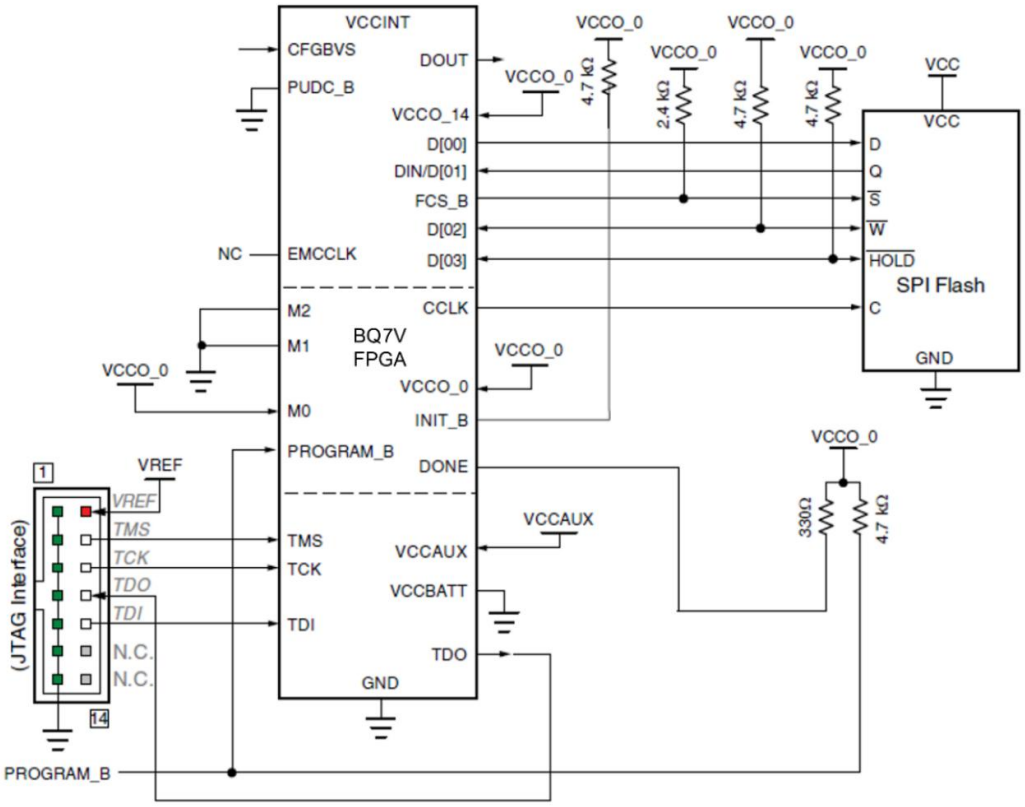


Figure 4-19 SPI x4 Configuration Interface

When configuration starts, the FPGA clocks data is imported on the rising edge. This continues until the FPGA reads the command in the early part of the bitstream that instructs it to change to the falling edge. This occurs before the command to change to external clocking or the command to change the master clock frequency. The falling edge clocking option is enabled by setting the option spi_fall_edge.

SPI Serial Daisy Chain

In a serial daisy chain application, the leading device can be in SPI mode and all downstream devices in Slave Serial mode. In this case, all configuration bitstreams can be stored inside one SPI device. The bitstream format for master and slave serial daisy chains is exactly the same.

4.10.4 Byte Peripheral Interface Parallel Flash Mode

In BPI (M[2:0]=100) mode, the BQ7V FPGA configures itself from an industry-standard parallel NOR Flash PROM, as illustrated in Figure 4-20. BPI configuration mode has two BPI flash read modes available: asynchronous and synchronous. Bus widths of x8 and x16 are supported.

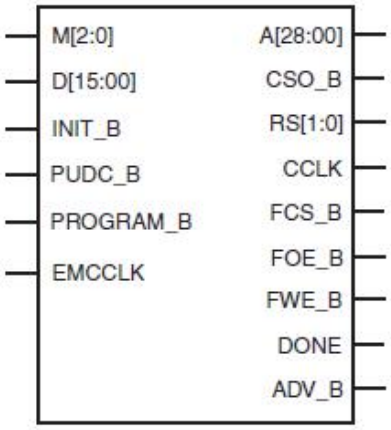


Figure 4-20 BQ7V BPI Configuration Interface

Asynchronous Read Mode Support

In the Master BPI configuration mode, the BQ7V FPGAs use the BPI flash asynchronous read mode by default to read bitstream data. After power-up, the Mode pins, M[2:0], are sampled when the FPGA's INIT_B output goes High. The Mode pins must be defined at the valid logic levels (Master BPI Configuration mode M[2:0] = 010) at this time. The PUDC_B pin must remain at a constant logic level throughout the FPGA configuration. After the Master BPI configuration mode is determined, the FPGA drives the flash control signals (FWE_B High, FOE_B Low, and FCS_B Low). Although the CCLK output is not connected to the BPI flash device for BPI flash asynchronous read mode, the FPGA outputs an address after the rising edge of CCLK, and the data is still sampled on the next rising edge of CCLK. The timing parameters related to BPI use the CCLK pin as a reference. In the Master BPI mode, the address starts at 0 and increments by 1 until the DONE pin is asserted. If the address reaches the maximum value (29'h1FFFFFF) and configuration is not done (DONE is not asserted), an error flag is raised in the status register, and fallback reconfiguration starts.

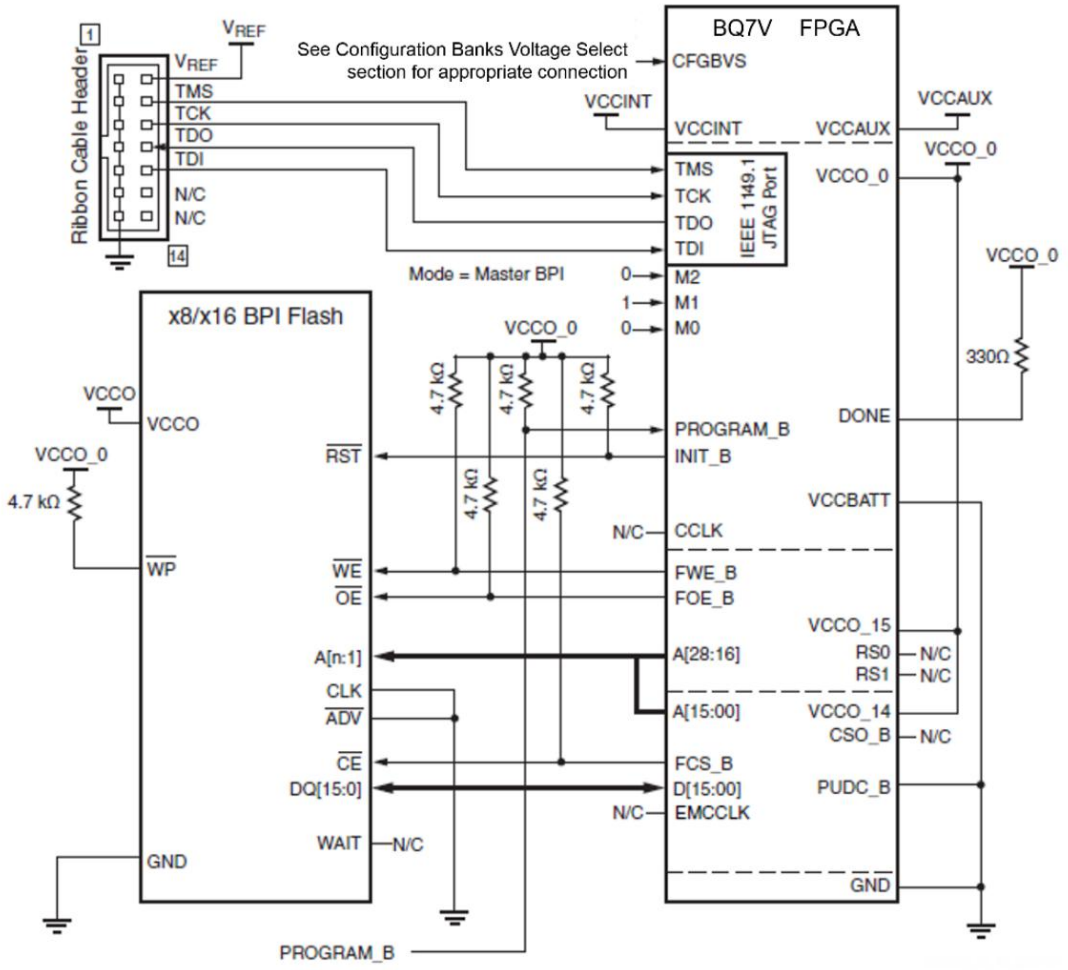


Figure 4-21 BQ7V BPI Asynchronous Configuration

Synchronous Read Mode Support

The BQ7V FPGA Master BPI configuration mode with synchronous read is the fastest direct flash configuration option without the need for customized external control logic. The FPGA starts in asynchronous read mode, using the default CCLK frequency, and the bitstream header determines if the read mode continues asynchronously or if it switches to the faster synchronous read mode. Bitstream commands initiate the switch from asynchronous read to synchronous read if the BPI_ sync_ mode option is set. There are two available settings for the option: Type1 or Type2. Type1 is used to set the G18F flash family synchronous and latency bits and Type2 is used to set the P30/P33. The switch to synchronous mode is done by the FPGA controller, which performs an asynchronous write to the BPI flash configuration register to set the device into synchronous mode and initiate a bitstream reread. To support the synchronous read mode, the FPGA CCLK output is connected to the BPI flash device, and the ADV_B FPGA signal must be connected to the flash ADV signal.

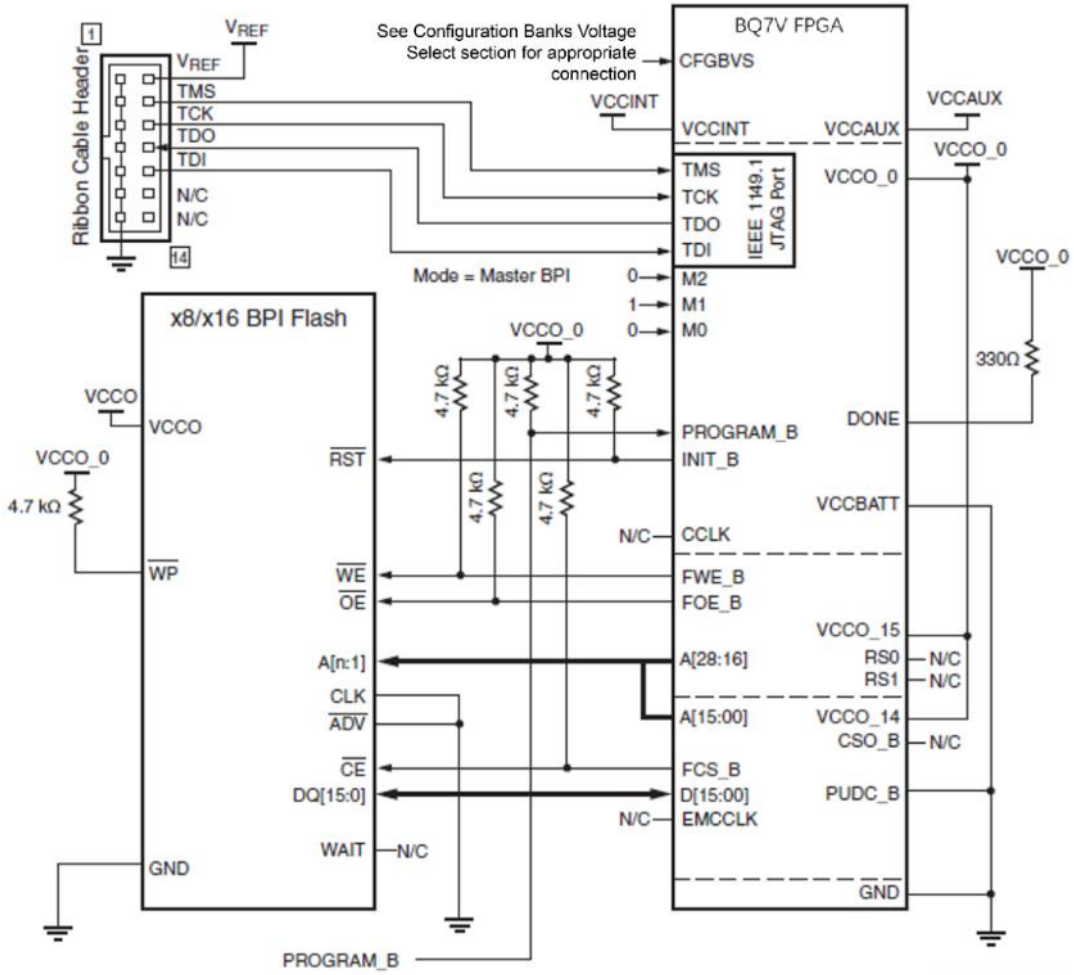


Figure 4-22 BQ7V BPI Synchronous Configuration

Page Mode Support

Many NOR Flash devices support asynchronous page reads. The first access to a page usually takes the longest time (~100 ns), subsequent accesses to the same page take less time (~25 ns). The following parameters are bitstream programmable in BQ7V devices to take advantage of page reads and maximize the CCLK frequency:

- Page sizes of 1 (default), 4, or 8.
- If the actual Flash page size is larger than 8, the value of 8 should be used to maximize the efficiency.
- First access CCLK cycles of 1 (default), 2, 3, or 4. CCLK cycles must be 1 if the page size is 1.
- CCLK frequency

For more details on configuration, see UG470. 7 Series FPGAs Configuration User Guide.

5. Electrical Characteristics

Table 5-1 DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	MAX	Units
IREF	VREF leakage current per pin		15	μA
IL	Input or output leakage current per pin (sample-tested)		15	μA
IRPU	Pad pull-up (when selected) @ VIN = 0V, VCCO = 3.3V	90	330	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 2.5V	68	250	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 1.8V	34	220	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 1.5V	23	150	μA
	Pad pull-up (when selected) @ VIN = 0V, VCCO = 1.2V	12	120	μA
IRPD	Pad pull-down (when selected) @ VIN = 3.3V	68	330	μA
	Pad pull-down (when selected) @ VIN = 1.8V	45	180	μA

Table 5-2 SelectIO DC Input and Output Levels

I/O Standard	VIL		VIH		VOL	VOH	lOL	lOH
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	8(1)	-8(2)
HSTL_I_12	- 0.300	VREF-0.080	VREF + 0.080	VCCO + 0.300	25% VCCO	75% VCCO	6.3(3)	-6.3(4)
HSTL_I_18	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	8(1)	-8(2)
HSTL_II	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	16(1)	-16(2)
HSTL_II_18	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	0.400	VCCO-0.400	16(1)	-16(2)
HSUL_12	- 0.300	VREF-0.130	VREF+ 0.130	VCCO + 0.300	20% VCCO	80% VCCO	0.1(1)	-0.1(2)
LVCMOS12	- 0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.400	VCCO-0.400	12(5)	-12(16)
LVCMOS15,	- 0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.450	VCCO-0.450	16(1)	-16(2)
LVCMOS18	- 0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.400	VCCO-0.400	24(5)	-24(6)

SSTL12	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	VCCO/2 - 0.150	VCCO/2 + 0.150	14.25 (3)	-14.25 (4)
SSTL135	- 0.300	VREF-0.090	VREF + 0.090	VCCO + 0.300	VCCO/2 - 0.150	VCCO/2 + 0.150	13.0(1)	-13.0(2)
SSTL15	- 0.300	VREF-0.100	VREF + 0.100	VCCO + 0.300	VCCO/2 - 0.175	VCCO/2 + 0.175	13.0(1)	-13.0(2)
SSTL18_I	-0.300	VREF-0.125	VREF + 0.125	VCCO +0.300	VCCO/2 - 0.470	VCCO/2 + 0.470	8(1)	-8(2)
SSTL18_II	-0.300	VREF-0.125	VREF+ 0.125	VCCO +0.300	VCCO/2 - 0.600	VCCO/2 + 0.600	13.4(1)	-13.4(2)

(1)Test VOL in HP-I/O and HR-I/O, Supported drive current(positive).

(2)Test VOH in HP-I/O and HR-I/O, Supported drive current(negative).

(3)Test VOL only in HP-I/O , Supported drive current(positive).

(4)Test VOH only in HP-I/O, Supported drive current(negative).

(5)Test VOL only in HR-I/O, Supported drive current(positive).

(6)Test VOH only in HR-I/O, Supported drive current(negative).

Table 5-3 Differential IO DC Input and Output Levels

Symbol	DC Parameter	Conditions	Min	Max	Units
VOH	Output High voltage	LVDS are only supported in in HP I/O banks		1.675	V
VOL	Output Low voltage		0.825		V
VODIFF	Differential output voltage		247	600	mV
VOCM	Output common-mode voltage		1.000	1.425	V
VIDIFF	Differential input voltage		100	600	mV
VICM	Input common-mode voltage		0.300	1.425	V
VOH	Output High voltage	LVDS_25 are only supported in in HR I/O banks		1.675	V
VOL	Output Low voltage		0.700		V
VODIFF	Differential output voltage		247	600	mV
VOCM	Output common-mode voltage		1.000	1.425	V
VIDIFF	Differential input voltage		100	600	mV
VICM	Input common-mode voltage		0.300	1.500	V

Table 5-4 MMCM Switching Characteristics

Symbol	Description	Min	M MAX	Units

MMCM_FINMIN	MMCM Minimum input clock frequency	10		MHz
MMCM_FINMAX	MMCM Maximum input clock frequency		800	MHz
MMCM_FOUTMIN	MMCM minimum output frequency	4.69		MHz
MMCM_FOUTMAX	MMCM maximum output frequency		800	MHz
MMCM_FVCOTMIN	MMCM minimum VCO frequency	600		MHz
MMCM_FVCOTMAX	MMCM maximum VCO frequency		1200	MHz
MMCM_FPFDMIN	Minimum frequency at the phase frequency detector	10		MHz
MMCM_FPFDMAX	Maximum frequency at the phase frequency detector		450	MHz

Table 5-5 PLL Switching Characteristics

Symbol	Description	Min	MAX	Units
PLL_FINMIN	PLL Minimum input clock frequency	19		MHz
PLL_FINMAX	PLL Maximum input clock frequency		800	MHz
PLL_FOUTMIN	PLL minimum output frequency	6.25		MHz
PLL_FOUTMAX	PLL maximum output frequency		800	MHz
PLL_FVCOTMIN	PLL minimum VCO frequency	800		MHz
PLL_FVCOTMAX	PLL maximum VCO frequency		1600	MHz
PLL_FPFDMIN	Minimum frequency at the phase frequency detector	19		MHz
PLL_FPFDMAX	Maximum frequency at the phase frequency detector		450	MHz

Table 5-6 GTH Transceiver DC Specifications

Symbol	Description	Conditions	Min	MAX	Units
DVPPIN	Differential mode input voltage (DC coupled)	>10.3125 Gb/s	150	1250	mV
		6.6 Gb/s - 10.3125 Gb/s	150	1250	mV
		< 6.6 Gb/s	150	1250	mV
VCMIN	Common mode input voltage	2/3 VMGTAVTT			mV
DVPPOUT	Differential mode output voltage	Transmitter output swing is set to 4'b1010	800		mV
VCMOUTDC	Common mode output voltage:	DC coupled		VMGTAVTT-200	mV
VIDIFF	Differential clock input voltage		350	2000	mV

Table 5-7 GTH Transceiver AC Specifications

Symbol	Description	Conditions	Min	MAX	Units
FGTHMAX	Maximum GTH transceiver data rate			8.5	Gbps
FGTHMIN	Minimum GTH transceiver data rate		0.5		Gbps
FGCLK	Reference clock frequency range		60	820	MHz

6. Typical Applications

The application fields of BQ7V series FPGA include: communication transmission field, mainly used for high-speed interface circuit design of communication equipment, to complete high-speed data transceiver and exchange; high performance digital signal and image processing field, to achieve a variety of more complex mathematical algorithms, using FPGA internal resources to make it into the actual processing circuit; SOPC and other control processing fields, mainly use FPGA platform to build embedded system, and then carry out embedded system software development.

A typical kind of hardware system application of BQ7V series FPGA is shown in Figure 6-1. The system includes a BQ7V series FPGA, a PROM configuration memory, DDR3 data storage, PCIE circuit, SFP optical fiber communication interface, RS232/ RS485 interface, GTH and universal I/O extended interface, etc.

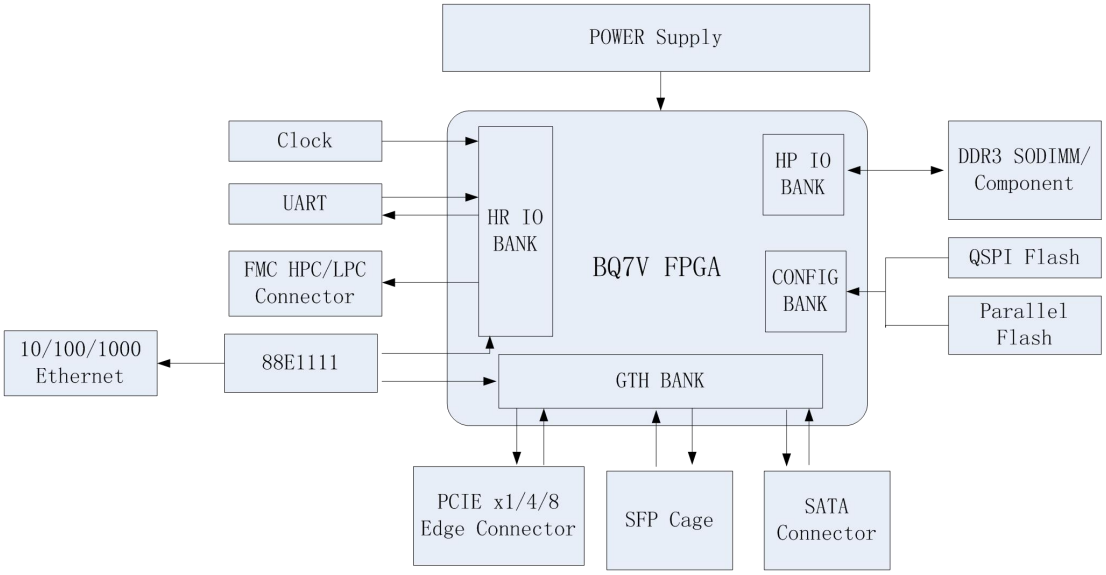


Figure 6-1 Typical Hardware Application

7. Notes for Application

7.1 Product Introduction of Application

BQ7VX330TBG1761, BQ7VX690TBG1761, BQ7VX690TBG1927 and XILINX XQ7VX330T, XQ7VX690T are consistent in circuit structure, various electrical parameters, design process and development tools. BQ7VX330TBG1761, BQ7VX690TBG1761 and BQ7VX690TBG1927 have no special requirements. Xilinx Vivado development environment is recommended as development tools.

7.2 Attention Matters

a. The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO}. To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence;

b. The recommended power-on sequence to achieve minimum current draw for the GTH transceivers is V_{CCINT}, $V_{MGTAVCC}$,$V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

c. It's suggested that the actual frequency of the device should not exceed 80% of the maximum constraint frequency that can be passed, so as to keep sufficient design margin;

d. Maximum data transmission rate of PCI Express is not higher than 8.5Gbps.

e. Recommended analog supply voltage for the GTH transceiver QPLL frequency range （VMGTAVCC）: 1.02V～1.08V(Under 6.6Gbps), 1.05V～1.08V(Over 6.6Gbps).

7.3 Product Protection

The packaging of the product is made of non-corrosive material, which can conduct electricity or be coated or impregnated with antistatic material, and has sufficient antistatic ability.

Under the condition of avoiding the direct influence of rain and snow, the packing boxes which contain the product can be transported by any means of transportation. But don't put them with acid, alkaline or other corrosive objects.

The storage environment of the packaged products shall meet the requirements in Section 8.1 of Q/W 657A — 2007(temperature: 15℃~25℃, humidity: 25%~65%), without acid, alkaline or other corrosive gases, with good ventilation and corresponding anti-static measures.

7.3.1 Product Packaging

The device packaging shall at least meet the following requirements:

a. Made of non-corrosive material;

b. Strong enough to withstand the shock during handling;

c. Coated or impregnated with antistatic materials and has sufficient antistatic capacity;
d. Can firmly support the installed device in a certain position;
e. Can keep the lead of the device from deformation;
f. No sharp edges or corners;
g. Can safely and easily remove, check and replace the device;
h. Generally, do not use polyvinyl chloride, neoprene rubber, vinyl resin or polysulfide materials. It's advisable to use materials with low exhaust index and low dust particle shedding.

7.3.2 Transport and Storage

During transportation and storage, the device shall at least meet the following requirements:

a. Transportation: Under the condition of avoiding the direct influence of rain and snow, the packing boxes which contain the products can be transported by any means of transportation. But don't put them with acid, alkaline and other corrosive objects.
b. Storage: Packaged products shall be stored in a well-ventilated warehouse with ambient temperature of 16℃~28℃, relative humidity not greater than 30%~70%, and without acid, alkaline or other corrosive gases.

Appendix I Soldering Suggestion

Reflow soldering curve is shown as Figure 1.

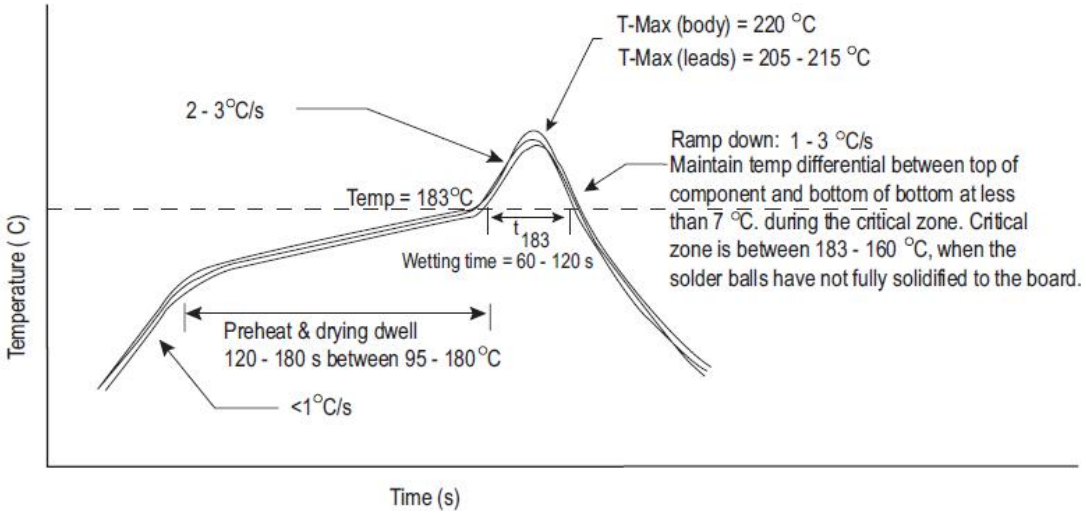


Figure 1 Reflow soldering curve

Appendix II Pinout Information and Package

Table 1 BQ7VX330TBG1761-PBGA1761 Pinout

Bank	**Pin name**	**Pin**	**I/O Type**
0	DXN_0	AC20	CONFIG
0	VCCADC_0	Y21	CONFIG
0	GNDADC_0	Y20	CONFIG
0	DXP_0	AC21	CONFIG
0	VREFN_0	AA20	CONFIG
0	VREFP_0	AB21	CONFIG
0	VP_0	AA21	CONFIG
0	VN_0	AB20	CONFIG
0	VCCBATT_0	N11	CONFIG
0	CCLK_0	N10	CONFIG
0	TCK_0	P10	CONFIG
0	TMS_0	P11	CONFIG
0	TDO_0	R10	CONFIG
0	TDI_0	T10	CONFIG
0	INIT_B_0	AG11	CONFIG
0	PROGRAM_B_0	AJ11	CONFIG
0	CFGBVS_0	AH10	CONFIG
0	DONE_0	AL11	CONFIG
0	M2_0	AJ10	CONFIG
0	M0_0	AL10	CONFIG
0	M1_0	AK10	CONFIG

Bank	Pin name	Pin	I/O Type
NA	NC	AN29	NA
NA	NC	AY27	NA
NA	NC	AY28	NA
NA	NC	AU29	NA
NA	NC	AV29	NA
NA	NC	BA26	NA
NA	NC	BA27	NA
NA	NC	BB28	NA
NA	NC	BB29	NA
NA	NC	BB26	NA
NA	NC	BB27	NA
NA	NC	AY29	NA
NA	NC	BA29	NA
NA	NC	AW25	NA
NA	NC	AW26	NA
NA	NC	AR29	NA
NA	NC	AT29	NA
NA	NC	AV25	NA
NA	NC	AV26	NA
NA	NC	AW27	NA
NA	NC	AW28	NA
NA	NC	AU28	NA
NA	NC	AV28	NA
NA	NC	AU26	NA
NA	NC	AU27	NA
NA	NC	AR27	NA
NA	NC	AT27	NA
NA	NC	AP27	NA
NA	NC	AR28	NA
NA	NC	AN28	NA
NA	NC	AP28	NA
NA	NC	AT25	NA
NA	NC	AT26	NA
NA	NC	AP25	NA
NA	NC	AR25	NA
NA	NC	AN25	NA
NA	NC	AN26	NA
NA	NC	AM28	NA
NA	NC	AM29	NA
NA	NC	AK27	NA

Bank	Pin name	Pin	I/O Type
NA	NC	AL27	NA
NA	NC	AM26	NA
NA	NC	AM27	NA
NA	NC	AK24	NA
NA	NC	AK25	NA
NA	NC	AL25	NA
NA	NC	AL26	NA
NA	NC	AJ25	NA
NA	NC	AJ26	NA
NA	NC	AP26	NA
13	IO_0_13	AR35	HR
13	IO_L1P_T0_13	AY34	HR
13	IO_L1N_T0_13	BA35	HR
13	IO_L2P_T0_13	AV36	HR
13	IO_L2N_T0_13	AW36	HR
13	IO_L3P_T0_DQS_13	BA34	HR
13	IO_L3N_T0_DQS_13	BB34	HR
13	IO_L4P_T0_13	BA36	HR
13	IO_L4N_T0_13	BB36	HR
13	IO_L5P_T0_13	BB32	HR
13	IO_L5N_T0_13	BB33	HR
13	IO_L6P_T0_13	AW35	HR
13	IO_L6N_T0_VREF_13	AY35	HR
13	IO_L7P_T1_13	AT34	HR
13	IO_L7N_T1_13	AU34	HR
13	IO_L8P_T1_13	AT36	HR
13	IO_L8N_T1_13	AU36	HR
13	IO_L9P_T1_DQS_13	AT32	HR
13	IO_L9N_T1_DQS_13	AU33	HR
13	IO_L10P_T1_13	AR34	HR
13	IO_L10N_T1_13	AT35	HR
13	IO_L11P_T1_SRCC_13	AU32	HR
13	IO_L11N_T1_SRCC_13	AV33	HR
13	IO_L12P_T1_MRCC_13	AW32	HR
13	IO_L12N_T1_MRCC_13	AW33	HR
13	IO_L13P_T2_MRCC_13	AV34	HR
13	IO_L13N_T2_MRCC_13	AV35	HR
13	IO_L14P_T2_SRCC_13	AY32	HR
13	IO_L14N_T2_SRCC_13	AY33	HR
13	IO_L15P_T2_DQS_13	BA31	HR

Bank	Pin name	Pin	I/O Type
13	IO_L15N_T2_DQS_13	BA32	HR
13	IO_L16P_T2_13	AW30	HR
13	IO_L16N_T2_13	AY30	HR
13	IO_L17P_T2_13	BA30	HR
13	IO_L17N_T2_13	BB31	HR
13	IO_L18P_T2_13	AV30	HR
13	IO_L18N_T2_13	AW31	HR
13	IO_L19P_T3_13	AR30	HR
13	IO_L19N_T3_VREF_13	AT30	HR
13	IO_L20P_T3_13	AU31	HR
13	IO_L20N_T3_13	AV31	HR
13	IO_L21P_T3_DQS_13	AN30	HR
13	IO_L21N_T3_DQS_13	AP30	HR
13	IO_L22P_T3_13	AP32	HR
13	IO_L22N_T3_13	AR32	HR
13	IO_L23P_T3_13	AN31	HR
13	IO_L23N_T3_13	AP31	HR
13	IO_L24P_T3_13	AP33	HR
13	IO_L24N_T3_13	AR33	HR
13	IO_25_13	AT31	HR
14	IO_0_VRN_14	AH35	HP
14	IO_L1P_T0_D00_MOSI_14	AM36	HP
14	IO_L1N_T0_D01_DIN_14	AN36	HP
14	IO_L2P_T0_D02_14	AJ36	HP
14	IO_L2N_T0_D03_14	AJ37	HP
14	IO_L3P_T0_DQS_PUDC_B_14	AP36	HP
14	IO_L3N_T0_DQS_EMCCLK_14	AP37	HP
14	IO_L4P_T0_D04_14	AK37	HP
14	IO_L4N_T0_D05_14	AL37	HP
14	IO_L5P_T0_D06_14	AN35	HP
14	IO_L5N_T0_D07_14	AP35	HP
14	IO_L6P_T0_FCS_B_14	AL36	HP
14	IO_L6N_T0_D08_VREF_14	AM37	HP
14	IO_L7P_T1_D09_14	AG33	HP
14	IO_L7N_T1_D10_14	AH33	HP
14	IO_L8P_T1_D11_14	AK35	HP
14	IO_L8N_T1_D12_14	AL35	HP
14	IO_L9P_T1_DQS_14	AH31	HP
14	IO_L9N_T1_DQS_D13_14	AJ31	HP
14	IO_L10P_T1_D14_14	AH34	HP

Bank	Pin name	Pin	I/O Type
14	IO_L10N_T1_D15_14	AJ35	HP
14	IO_L11P_T1_SRCC_14	AJ33	HP
14	IO_L11N_T1_SRCC_14	AK33	HP
14	IO_L12P_T1_MRCC_14	AK34	HP
14	IO_L12N_T1_MRCC_14	AL34	HP
14	IO_L13P_T2_MRCC_14	AJ32	HP
14	IO_L13N_T2_MRCC_14	AK32	HP
14	IO_L14P_T2_SRCC_14	AL31	HP
14	IO_L14N_T2_SRCC_14	AL32	HP
14	IO_L15P_T2_DQS_RDWR_B_14	AM34	HP
14	IO_L15N_T2_DQS_DOUT_CSO_B_14	AN34	HP
14	IO_L16P_T2_CSI_B_14	AM31	HP
14	IO_L16N_T2_A15_D31_14	AM32	HP
14	IO_L17P_T2_A14_D30_14	AM33	HP
14	IO_L17N_T2_A13_D29_14	AN33	HP
14	IO_L18P_T2_A12_D28_14	AL29	HP
14	IO_L18N_T2_A11_D27_14	AL30	HP
14	IO_L19P_T3_A10_D26_14	AH29	HP
14	IO_L19N_T3_A09_D25_VREF_14	AH30	HP
14	IO_L20P_T3_A08_D24_14	AJ30	HP
14	IO_L20N_T3_A07_D23_14	AK30	HP
14	IO_L21P_T3_DQS_14	AF29	HP
14	IO_L21N_T3_DQS_A06_D22_14	AG29	HP
14	IO_L22P_T3_A05_D21_14	AK28	HP
14	IO_L22N_T3_A04_D20_14	AK29	HP
14	IO_L23P_T3_A03_D19_14	AF30	HP
14	IO_L23N_T3_A02_D18_14	AG31	HP
14	IO_L24P_T3_A01_D17_14	AH28	HP
14	IO_L24N_T3_A00_D16_14	AJ28	HP
14	IO_25_VRP_14	AG32	HP
15	IO_0_VRN_15	AM38	HP
15	IO_L1P_T0_AD0P_15	AN38	HP
15	IO_L1N_T0_AD0N_15	AP38	HP
15	IO_L2P_T0_AD8P_15	AM41	HP
15	IO_L2N_T0_AD8N_15	AM42	HP
15	IO_L3P_T0_DQS_AD1P_15	AR38	HP
15	IO_L3N_T0_DQS_AD1N_15	AR39	HP
15	IO_L4P_T0_15	AN40	HP
15	IO_L4N_T0_15	AN41	HP
15	IO_L5P_T0_AD9P_15	AR37	HP

Bank	Pin name	Pin	I/O Type
15	IO_L5N_T0_AD9N_15	AT37	HP
15	IO_L6P_T0_15	AM39	HP
15	IO_L6N_T0_VREF_15	AN39	HP
15	IO_L7P_T1_AD2P_15	AP40	HP
15	IO_L7N_T1_AD2N_15	AR40	HP
15	IO_L8P_T1_AD10P_15	AP41	HP
15	IO_L8N_T1_AD10N_15	AP42	HP
15	IO_L9P_T1_DQS_AD3P_15	AT39	HP
15	IO_L9N_T1_DQS_AD3N_15	AT40	HP
15	IO_L10P_T1_AD11P_15	AR42	HP
15	IO_L10N_T1_AD11N_15	AT42	HP
15	IO_L11P_T1_SRCC_15	AU39	HP
15	IO_L11N_T1_SRCC_15	AV39	HP
15	IO_L12P_T1_MRCC_15	AU38	HP
15	IO_L12N_T1_MRCC_15	AV38	HP
15	IO_L13P_T2_MRCC_15	AV40	HP
15	IO_L13N_T2_MRCC_15	AW40	HP
15	IO_L14P_T2_SRCC_15	AY39	HP
15	IO_L14N_T2_SRCC_15	AY40	HP
15	IO_L15P_T2_DQS_15	AW37	HP
15	IO_L15N_T2_DQS_ADV_B_15	AY37	HP
15	IO_L16P_T2_A28_15	BA37	HP
15	IO_L16N_T2_A27_15	BB37	HP
15	IO_L17P_T2_A26_15	AW38	HP
15	IO_L17N_T2_A25_15	AY38	HP
15	IO_L18P_T2_A24_15	BB38	HP
15	IO_L18N_T2_A23_15	BB39	HP
15	IO_L19P_T3_A22_15	BA39	HP
15	IO_L19N_T3_A21_VREF_15	BA40	HP
15	IO_L20P_T3_A20_15	AT41	HP
15	IO_L20N_T3_A19_15	AU42	HP
15	IO_L21P_T3_DQS_15	AY42	HP
15	IO_L21N_T3_DQS_A18_15	BA42	HP
15	IO_L22P_T3_A17_15	AU41	HP
15	IO_L22N_T3_A16_15	AV41	HP
15	IO_L23P_T3_FOE_B_15	BA41	HP
15	IO_L23N_T3_FWE_B_15	BB41	HP
15	IO_L24P_T3_RS1_15	AW41	HP
15	IO_L24N_T3_RS0_15	AW42	HP
15	IO_25_VRP_15	AU37	HP

Bank	Pin name	Pin	I/O Type
16	IO_0_VRN_16	Y34	HP
16	IO_L1P_T0_16	AF35	HP
16	IO_L1N_T0_16	AF36	HP
16	IO_L2P_T0_16	AE37	HP
16	IO_L2N_T0_16	AF37	HP
16	IO_L3P_T0_DQS_16	AF34	HP
16	IO_L3N_T0_DQS_16	AG34	HP
16	IO_L4P_T0_16	AD36	HP
16	IO_L4N_T0_16	AD37	HP
16	IO_L5P_T0_16	AC35	HP
16	IO_L5N_T0_16	AC36	HP
16	IO_L6P_T0_16	AG36	HP
16	IO_L6N_T0_VREF_16	AH36	HP
16	IO_L7P_T1_16	Y37	HP
16	IO_L7N_T1_16	AA37	HP
16	IO_L8P_T1_16	Y35	HP
16	IO_L8N_T1_16	AA36	HP
16	IO_L9P_T1_DQS_16	AB36	HP
16	IO_L9N_T1_DQS_16	AB37	HP
16	IO_L10P_T1_16	AA34	HP
16	IO_L10N_T1_16	AA35	HP
16	IO_L11P_T1_SRCC_16	AB31	HP
16	IO_L11N_T1_SRCC_16	AB32	HP
16	IO_L12P_T1_MRCC_16	AB33	HP
16	IO_L12N_T1_MRCC_16	AC33	HP
16	IO_L13P_T2_MRCC_16	AD32	HP
16	IO_L13N_T2_MRCC_16	AD33	HP
16	IO_L14P_T2_SRCC_16	AC34	HP
16	IO_L14N_T2_SRCC_16	AD35	HP
16	IO_L15P_T2_DQS_16	AE32	HP
16	IO_L15N_T2_DQS_16	AE33	HP
16	IO_L16P_T2_16	AF31	HP
16	IO_L16N_T2_16	AF32	HP
16	IO_L17P_T2_16	AE34	HP
16	IO_L17N_T2_16	AE35	HP
16	IO_L18P_T2_16	AE29	HP
16	IO_L18N_T2_16	AE30	HP
16	IO_L19P_T3_16	Y32	HP
16	IO_L19N_T3_VREF_16	Y33	HP
16	IO_L20P_T3_16	AC31	HP

Bank	Pin name	Pin	I/O Type
16	IO_L20N_T3_16	AD31	HP
16	IO_L21P_T3_DQS_16	AA31	HP
16	IO_L21N_T3_DQS_16	AA32	HP
16	IO_L22P_T3_16	AC30	HP
16	IO_L22N_T3_16	AD30	HP
16	IO_L23P_T3_16	AA29	HP
16	IO_L23N_T3_16	AA30	HP
16	IO_L24P_T3_16	AB29	HP
16	IO_L24N_T3_16	AC29	HP
16	IO_25_VRP_16	AB34	HP
17	IO_0_VRN_17	Y38	HP
17	IO_L1P_T0_17	AB41	HP
17	IO_L1N_T0_17	AB42	HP
17	IO_L2P_T0_17	W40	HP
17	IO_L2N_T0_17	Y40	HP
17	IO_L3P_T0_DQS_17	Y39	HP
17	IO_L3N_T0_DQS_17	AA39	HP
17	IO_L4P_T0_17	Y42	HP
17	IO_L4N_T0_17	AA42	HP
17	IO_L5P_T0_17	AB38	HP
17	IO_L5N_T0_17	AB39	HP
17	IO_L6P_T0_17	AA40	HP
17	IO_L6N_T0_VREF_17	AA41	HP
17	IO_L7P_T1_17	AC38	HP
17	IO_L7N_T1_17	AC39	HP
17	IO_L8P_T1_17	AD42	HP
17	IO_L8N_T1_17	AE42	HP
17	IO_L9P_T1_DQS_17	AD38	HP
17	IO_L9N_T1_DQS_17	AE38	HP
17	IO_L10P_T1_17	AC40	HP
17	IO_L10N_T1_17	AC41	HP
17	IO_L11P_T1_SRCC_17	AE39	HP
17	IO_L11N_T1_SRCC_17	AE40	HP
17	IO_L12P_T1_MRCC_17	AD40	HP
17	IO_L12N_T1_MRCC_17	AD41	HP
17	IO_L13P_T2_MRCC_17	AF39	HP
17	IO_L13N_T2_MRCC_17	AF40	HP
17	IO_L14P_T2_SRCC_17	AF41	HP
17	IO_L14N_T2_SRCC_17	AG41	HP
17	IO_L15P_T2_DQS_17	AG39	HP

Bank	Pin name	Pin	I/O Type
17	IO_L15N_T2_DQS_17	AH39	HP
17	IO_L16P_T2_17	AF42	HP
17	IO_L16N_T2_17	AG42	HP
17	IO_L17P_T2_17	AG38	HP
17	IO_L17N_T2_17	AH38	HP
17	IO_L18P_T2_17	AJ38	HP
17	IO_L18N_T2_17	AK38	HP
17	IO_L19P_T3_17	AK40	HP
17	IO_L19N_T3_VREF_17	AL40	HP
17	IO_L20P_T3_17	AH40	HP
17	IO_L20N_T3_17	AH41	HP
17	IO_L21P_T3_DQS_17	AL41	HP
17	IO_L21N_T3_DQS_17	AL42	HP
17	IO_L22P_T3_17	AJ40	HP
17	IO_L22N_T3_17	AJ41	HP
17	IO_L23P_T3_17	AK39	HP
17	IO_L23N_T3_17	AL39	HP
17	IO_L24P_T3_17	AJ42	HP
17	IO_L24N_T3_17	AK42	HP
17	IO_25_VRP_17	AG37	HP
18	IO_0_VRN_18	N35	HP
18	IO_L1P_T0_18	T34	HP
18	IO_L1N_T0_18	R35	HP
18	IO_L2P_T0_18	N33	HP
18	IO_L2N_T0_18	N34	HP
18	IO_L3P_T0_DQS_18	R33	HP
18	IO_L3N_T0_DQS_18	R34	HP
18	IO_L4P_T0_18	P35	HP
18	IO_L4N_T0_18	P36	HP
18	IO_L5P_T0_18	T32	HP
18	IO_L5N_T0_18	R32	HP
18	IO_L6P_T0_18	P32	HP
18	IO_L6N_T0_VREF_18	P33	HP
18	IO_L7P_T1_18	T36	HP
18	IO_L7N_T1_18	R37	HP
18	IO_L8P_T1_18	P37	HP
18	IO_L8N_T1_18	P38	HP
18	IO_L9P_T1_DQS_18	U34	HP
18	IO_L9N_T1_DQS_18	T35	HP
18	IO_L10P_T1_18	R38	HP

Bank	Pin name	Pin	I/O Type
18	IO_L10N_T1_18	R39	HP
18	IO_L11P_T1_SRCC_18	U37	HP
18	IO_L11N_T1_SRCC_18	U38	HP
18	IO_L12P_T1_MRCC_18	U39	HP
18	IO_L12N_T1_MRCC_18	T39	HP
18	IO_L13P_T2_MRCC_18	U36	HP
18	IO_L13N_T2_MRCC_18	T37	HP
18	IO_L14P_T2_SRCC_18	V35	HP
18	IO_L14N_T2_SRCC_18	V36	HP
18	IO_L15P_T2_DQS_18	V33	HP
18	IO_L15N_T2_DQS_18	V34	HP
18	IO_L16P_T2_18	W36	HP
18	IO_L16N_T2_18	W37	HP
18	IO_L17P_T2_18	U32	HP
18	IO_L17N_T2_18	U33	HP
18	IO_L18P_T2_18	W32	HP
18	IO_L18N_T2_18	W33	HP
18	IO_L19P_T3_18	V39	HP
18	IO_L19N_T3_VREF_18	V40	HP
18	IO_L20P_T3_18	T40	HP
18	IO_L20N_T3_18	T41	HP
18	IO_L21P_T3_DQS_18	W41	HP
18	IO_L21N_T3_DQS_18	W42	HP
18	IO_L22P_T3_18	U41	HP
18	IO_L22N_T3_18	T42	HP
18	IO_L23P_T3_18	W38	HP
18	IO_L23N_T3_18	V38	HP
18	IO_L24P_T3_18	V41	HP
18	IO_L24N_T3_18	U42	HP
18	IO_25_VRP_18	W35	HP
19	IO_0_VRN_19	L36	HP
19	IO_L1P_T0_19	E40	HP
19	IO_L1N_T0_19	D40	HP
19	IO_L2P_T0_19	A40	HP
19	IO_L2N_T0_19	A41	HP
19	IO_L3P_T0_DQS_19	D41	HP
19	IO_L3N_T0_DQS_19	D42	HP
19	IO_L4P_T0_19	B41	HP
19	IO_L4N_T0_19	B42	HP
19	IO_L5P_T0_19	F42	HP

Bank	Pin name	Pin	I/O Type
19	IO_L5N_T0_19	E42	HP
19	IO_L6P_T0_19	C40	HP
19	IO_L6N_T0_VREF_19	C41	HP
19	IO_L7P_T1_19	H40	HP
19	IO_L7N_T1_19	H41	HP
19	IO_L8P_T1_19	H39	HP
19	IO_L8N_T1_19	G39	HP
19	IO_L9P_T1_DQS_19	G41	HP
19	IO_L9N_T1_DQS_19	G42	HP
19	IO_L10P_T1_19	F40	HP
19	IO_L10N_T1_19	F41	HP
19	IO_L11P_T1_SRCC_19	J40	HP
19	IO_L11N_T1_SRCC_19	J41	HP
19	IO_L12P_T1_MRCC_19	K39	HP
19	IO_L12N_T1_MRCC_19	K40	HP
19	IO_L13P_T2_MRCC_19	L39	HP
19	IO_L13N_T2_MRCC_19	L40	HP
19	IO_L14P_T2_SRCC_19	M41	HP
19	IO_L14N_T2_SRCC_19	L41	HP
19	IO_L15P_T2_DQS_19	K42	HP
19	IO_L15N_T2_DQS_19	J42	HP
19	IO_L16P_T2_19	M42	HP
19	IO_L16N_T2_19	L42	HP
19	IO_L17P_T2_19	K37	HP
19	IO_L17N_T2_19	K38	HP
19	IO_L18P_T2_19	M36	HP
19	IO_L18N_T2_19	L37	HP
19	IO_L19P_T3_19	P41	HP
19	IO_L19N_T3_VREF_19	N41	HP
19	IO_L20P_T3_19	M37	HP
19	IO_L20N_T3_19	M38	HP
19	IO_L21P_T3_DQS_19	R42	HP
19	IO_L21N_T3_DQS_19	P42	HP
19	IO_L22P_T3_19	N38	HP
19	IO_L22N_T3_19	M39	HP
19	IO_L23P_T3_19	R40	HP
19	IO_L23N_T3_19	P40	HP
19	IO_L24P_T3_19	N39	HP
19	IO_L24N_T3_19	N40	HP
19	IO_25_VRP_19	N36	HP

Bank	Pin name	Pin	I/O Type
NA	NC	AM14	NA
NA	NC	AJ16	NA
NA	NC	AJ15	NA
NA	NC	AK14	NA
NA	NC	AK13	NA
NA	NC	AK15	NA
NA	NC	AL14	NA
NA	NC	AJ13	NA
NA	NC	AJ12	NA
NA	NC	AL16	NA
NA	NC	AL15	NA
NA	NC	AK12	NA
NA	NC	AL12	NA
NA	NC	AM13	NA
NA	NC	AN13	NA
NA	NC	AM12	NA
NA	NC	AM11	NA
NA	NC	AN15	NA
NA	NC	AN14	NA
NA	NC	AN11	NA
NA	NC	AP11	NA
NA	NC	AR14	NA
NA	NC	AT14	NA
NA	NC	AP13	NA
NA	NC	AR13	NA
NA	NC	AU14	NA
NA	NC	AU13	NA
NA	NC	AV13	NA
NA	NC	AW13	NA
NA	NC	AP12	NA
NA	NC	AR12	NA
NA	NC	AR15	NA
NA	NC	AT15	NA
NA	NC	AT12	NA
NA	NC	AU12	NA
NA	NC	AV15	NA
NA	NC	AV14	NA
NA	NC	AW15	NA
NA	NC	AY15	NA
NA	NC	AW12	NA

Bank	Pin name	Pin	I/O Type
NA	NC	AY12	NA
NA	NC	BA15	NA
NA	NC	BA14	NA
NA	NC	AY14	NA
NA	NC	AY13	NA
NA	NC	BB14	NA
NA	NC	BB13	NA
NA	NC	BA12	NA
NA	NC	BB12	NA
NA	NC	AP15	NA
NA	NC	AR20	NA
NA	NC	AL19	NA
NA	NC	AM19	NA
NA	NC	AK17	NA
NA	NC	AL17	NA
NA	NC	AM18	NA
NA	NC	AM17	NA
NA	NC	AK19	NA
NA	NC	AK18	NA
NA	NC	AM16	NA
NA	NC	AN16	NA
NA	NC	AJ18	NA
NA	NC	AJ17	NA
NA	NC	AP18	NA
NA	NC	AP17	NA
NA	NC	AP20	NA
NA	NC	AR19	NA
NA	NC	AN19	NA
NA	NC	AN18	NA
NA	NC	AR18	NA
NA	NC	AR17	NA
NA	NC	AU18	NA
NA	NC	AV18	NA
NA	NC	AT17	NA
NA	NC	AU17	NA
NA	NC	AY18	NA
NA	NC	AY17	NA
NA	NC	AW18	NA
NA	NC	AW17	NA
NA	NC	AU19	NA

Bank	Pin name	Pin	I/O Type
NA	NC	AV19	NA
NA	NC	AT20	NA
NA	NC	AT19	NA
NA	NC	AV16	NA
NA	NC	AW16	NA
NA	NC	AT16	NA
NA	NC	AU16	NA
NA	NC	BB19	NA
NA	NC	BB18	NA
NA	NC	AV20	NA
NA	NC	AW20	NA
NA	NC	BA17	NA
NA	NC	BB17	NA
NA	NC	AY20	NA
NA	NC	BA20	NA
NA	NC	BA16	NA
NA	NC	BB16	NA
NA	NC	AY19	NA
NA	NC	BA19	NA
NA	NC	AP16	NA
33	IO_0_VRN_33	AL24	HP
33	IO_L1P_T0_33	AJ23	HP
33	IO_L1N_T0_33	AK23	HP
33	IO_L2P_T0_33	AK20	HP
33	IO_L2N_T0_33	AL20	HP
33	IO_L3P_T0_DQS_33	AJ22	HP
33	IO_L3N_T0_DQS_33	AK22	HP
33	IO_L4P_T0_33	AL21	HP
33	IO_L4N_T0_33	AM21	HP
33	IO_L5P_T0_33	AJ21	HP
33	IO_L5N_T0_33	AJ20	HP
33	IO_L6P_T0_33	AL22	HP
33	IO_L6N_T0_VREF_33	AM22	HP
33	IO_L7P_T1_33	AM24	HP
33	IO_L7N_T1_33	AN24	HP
33	IO_L8P_T1_33	AM23	HP
33	IO_L8N_T1_33	AN23	HP
33	IO_L9P_T1_DQS_33	AP23	HP
33	IO_L9N_T1_DQS_33	AP22	HP
33	IO_L10P_T1_33	AN21	HP

Bank	Pin name	Pin	I/O Type
33	IO_L10N_T1_33	AP21	HP
33	IO_L11P_T1_SRCC_33	AR23	HP
33	IO_L11N_T1_SRCC_33	AR22	HP
33	IO_L12P_T1_MRCC_33	AT22	HP
33	IO_L12N_T1_MRCC_33	AU22	HP
33	IO_L13P_T2_MRCC_33	AU23	HP
33	IO_L13N_T2_MRCC_33	AV23	HP
33	IO_L14P_T2_SRCC_33	AW23	HP
33	IO_L14N_T2_SRCC_33	AW22	HP
33	IO_L15P_T2_DQS_33	AT21	HP
33	IO_L15N_T2_DQS_33	AU21	HP
33	IO_L16P_T2_33	AR24	HP
33	IO_L16N_T2_33	AT24	HP
33	IO_L17P_T2_33	AV21	HP
33	IO_L17N_T2_33	AW21	HP
33	IO_L18P_T2_33	AU24	HP
33	IO_L18N_T2_33	AV24	HP
33	IO_L19P_T3_33	AY23	HP
33	IO_L19N_T3_VREF_33	AY22	HP
33	IO_L20P_T3_33	AY25	HP
33	IO_L20N_T3_33	BA25	HP
33	IO_L21P_T3_DQS_33	BA22	HP
33	IO_L21N_T3_DQS_33	BB22	HP
33	IO_L22P_T3_33	AY24	HP
33	IO_L22N_T3_33	BA24	HP
33	IO_L23P_T3_33	BA21	HP
33	IO_L23N_T3_33	BB21	HP
33	IO_L24P_T3_33	BB24	HP
33	IO_L24N_T3_33	BB23	HP
33	IO_25_VRP_33	AN20	HP
34	IO_0_VRN_34	R29	HP
34	IO_L1P_T0_34	K35	HP
34	IO_L1N_T0_34	J35	HP
34	IO_L2P_T0_34	J32	HP
34	IO_L2N_T0_34	J33	HP
34	IO_L3P_T0_DQS_34	K33	HP
34	IO_L3N_T0_DQS_34	K34	HP
34	IO_L4P_T0_34	L34	HP
34	IO_L4N_T0_34	L35	HP
34	IO_L5P_T0_34	M33	HP

Bank	Pin name	Pin	I/O Type
34	IO_L5N_T0_34	M34	HP
34	IO_L6P_T0_34	H34	HP
34	IO_L6N_T0_VREF_34	H35	HP
34	IO_L7P_T1_34	K29	HP
34	IO_L7N_T1_34	K30	HP
34	IO_L8P_T1_34	J30	HP
34	IO_L8N_T1_34	H30	HP
34	IO_L9P_T1_DQS_34	L29	HP
34	IO_L9N_T1_DQS_34	L30	HP
34	IO_L10P_T1_34	J31	HP
34	IO_L10N_T1_34	H31	HP
34	IO_L11P_T1_SRCC_34	M32	HP
34	IO_L11N_T1_SRCC_34	L32	HP
34	IO_L12P_T1_MRCC_34	L31	HP
34	IO_L12N_T1_MRCC_34	K32	HP
34	IO_L13P_T2_MRCC_34	N30	HP
34	IO_L13N_T2_MRCC_34	M31	HP
34	IO_L14P_T2_SRCC_34	P30	HP
34	IO_L14N_T2_SRCC_34	N31	HP
34	IO_L15P_T2_DQS_34	M28	HP
34	IO_L15N_T2_DQS_34	M29	HP
34	IO_L16P_T2_34	R28	HP
34	IO_L16N_T2_34	P28	HP
34	IO_L17P_T2_34	N28	HP
34	IO_L17N_T2_34	N29	HP
34	IO_L18P_T2_34	R30	HP
34	IO_L18N_T2_34	P31	HP
34	IO_L19P_T3_34	U31	HP
34	IO_L19N_T3_VREF_34	T31	HP
34	IO_L20P_T3_34	V30	HP
34	IO_L20N_T3_34	V31	HP
34	IO_L21P_T3_DQS_34	T29	HP
34	IO_L21N_T3_DQS_34	T30	HP
34	IO_L22P_T3_34	W30	HP
34	IO_L22N_T3_34	W31	HP
34	IO_L23P_T3_34	V29	HP
34	IO_L23N_T3_34	U29	HP
34	IO_L24P_T3_34	Y29	HP
34	IO_L24N_T3_34	Y30	HP
34	IO_25_VRP_34	U28	HP

Bank	Pin name	Pin	I/O Type
35	IO_0_VRN_35	G31	HP
35	IO_L1P_T0_AD4P_35	B36	HP
35	IO_L1N_T0_AD4N_35	A37	HP
35	IO_L2P_T0_AD12P_35	B34	HP
35	IO_L2N_T0_AD12N_35	A34	HP
35	IO_L3P_T0_DQS_AD5P_35	B39	HP
35	IO_L3N_T0_DQS_AD5N_35	A39	HP
35	IO_L4P_T0_35	A35	HP
35	IO_L4N_T0_35	A36	HP
35	IO_L5P_T0_AD13P_35	C38	HP
35	IO_L5N_T0_AD13N_35	C39	HP
35	IO_L6P_T0_35	B37	HP
35	IO_L6N_T0_VREF_35	B38	HP
35	IO_L7P_T1_AD6P_35	E32	HP
35	IO_L7N_T1_AD6N_35	D32	HP
35	IO_L8P_T1_AD14P_35	B32	HP
35	IO_L8N_T1_AD14N_35	B33	HP
35	IO_L9P_T1_DQS_AD7P_35	E33	HP
35	IO_L9N_T1_DQS_AD7N_35	D33	HP
35	IO_L10P_T1_AD15P_35	C33	HP
35	IO_L10N_T1_AD15N_35	C34	HP
35	IO_L11P_T1_SRCC_35	D35	HP
35	IO_L11N_T1_SRCC_35	D36	HP
35	IO_L12P_T1_MRCC_35	C35	HP
35	IO_L12N_T1_MRCC_35	C36	HP
35	IO_L13P_T2_MRCC_35	E34	HP
35	IO_L13N_T2_MRCC_35	E35	HP
35	IO_L14P_T2_SRCC_35	D37	HP
35	IO_L14N_T2_SRCC_35	D38	HP
35	IO_L15P_T2_DQS_35	G32	HP
35	IO_L15N_T2_DQS_35	F32	HP
35	IO_L16P_T2_35	F36	HP
35	IO_L16N_T2_35	F37	HP
35	IO_L17P_T2_35	F34	HP
35	IO_L17N_T2_35	F35	HP
35	IO_L18P_T2_35	H33	HP
35	IO_L18N_T2_35	G33	HP
35	IO_L19P_T3_35	E37	HP
35	IO_L19N_T3_VREF_35	E38	HP
35	IO_L20P_T3_35	G36	HP

Bank	Pin name	Pin	I/O Type
35	IO_L20N_T3_35	G37	HP
35	IO_L21P_T3_DQS_35	F39	HP
35	IO_L21N_T3_DQS_35	E39	HP
35	IO_L22P_T3_35	J37	HP
35	IO_L22N_T3_35	J38	HP
35	IO_L23P_T3_35	H38	HP
35	IO_L23N_T3_35	G38	HP
35	IO_L24P_T3_35	J36	HP
35	IO_L24N_T3_35	H36	HP
35	IO_25_VRP_35	G34	HP
36	IO_0_VRN_36	M23	HP
36	IO_L1P_T0_36	H24	HP
36	IO_L1N_T0_36	G24	HP
36	IO_L2P_T0_36	J21	HP
36	IO_L2N_T0_36	H21	HP
36	IO_L3P_T0_DQS_36	H25	HP
36	IO_L3N_T0_DQS_36	H26	HP
36	IO_L4P_T0_36	G21	HP
36	IO_L4N_T0_36	G22	HP
36	IO_L5P_T0_36	G26	HP
36	IO_L5N_T0_36	G27	HP
36	IO_L6P_T0_36	H23	HP
36	IO_L6N_T0_VREF_36	G23	HP
36	IO_L7P_T1_36	G28	HP
36	IO_L7N_T1_36	G29	HP
36	IO_L8P_T1_36	K28	HP
36	IO_L8N_T1_36	J28	HP
36	IO_L9P_T1_DQS_36	H28	HP
36	IO_L9N_T1_DQS_36	H29	HP
36	IO_L10P_T1_36	K27	HP
36	IO_L10N_T1_36	J27	HP
36	IO_L11P_T1_SRCC_36	K24	HP
36	IO_L11N_T1_SRCC_36	K25	HP
36	IO_L12P_T1_MRCC_36	J25	HP
36	IO_L12N_T1_MRCC_36	J26	HP
36	IO_L13P_T2_MRCC_36	M24	HP
36	IO_L13N_T2_MRCC_36	L24	HP
36	IO_L14P_T2_SRCC_36	K23	HP
36	IO_L14N_T2_SRCC_36	J23	HP
36	IO_L15P_T2_DQS_36	M22	HP

Bank	Pin name	Pin	I/O Type
36	IO_L15N_T2_DQS_36	L22	HP
36	IO_L16P_T2_36	L25	HP
36	IO_L16N_T2_36	L26	HP
36	IO_L17P_T2_36	K22	HP
36	IO_L17N_T2_36	J22	HP
36	IO_L18P_T2_36	M21	HP
36	IO_L18N_T2_36	L21	HP
36	IO_L19P_T3_36	P21	HP
36	IO_L19N_T3_VREF_36	N21	HP
36	IO_L20P_T3_36	P25	HP
36	IO_L20N_T3_36	P26	HP
36	IO_L21P_T3_DQS_36	P22	HP
36	IO_L21N_T3_DQS_36	P23	HP
36	IO_L22P_T3_36	N25	HP
36	IO_L22N_T3_36	N26	HP
36	IO_L23P_T3_36	N23	HP
36	IO_L23N_T3_36	N24	HP
36	IO_L24P_T3_36	M27	HP
36	IO_L24N_T3_36	L27	HP
36	IO_25_VRP_36	M26	HP
37	IO_0_VRN_37	F21	HP
37	IO_L1P_T0_37	A24	HP
37	IO_L1N_T0_37	A25	HP
37	IO_L2P_T0_37	B22	HP
37	IO_L2N_T0_37	A22	HP
37	IO_L3P_T0_DQS_37	A26	HP
37	IO_L3N_T0_DQS_37	A27	HP
37	IO_L4P_T0_37	C23	HP
37	IO_L4N_T0_37	B23	HP
37	IO_L5P_T0_37	B26	HP
37	IO_L5N_T0_37	B27	HP
37	IO_L6P_T0_37	C24	HP
37	IO_L6N_T0_VREF_37	B24	HP
37	IO_L7P_T1_37	E23	HP
37	IO_L7N_T1_37	E24	HP
37	IO_L8P_T1_37	F22	HP
37	IO_L8N_T1_37	E22	HP
37	IO_L9P_T1_DQS_37	F25	HP
37	IO_L9N_T1_DQS_37	E25	HP
37	IO_L10P_T1_37	D22	HP

Bank	Pin name	Pin	I/O Type
37	IO_L10N_T1_37	D23	HP
37	IO_L11P_T1_SRCC_37	D25	HP
37	IO_L11N_T1_SRCC_37	D26	HP
37	IO_L12P_T1_MRCC_37	C25	HP
37	IO_L12N_T1_MRCC_37	C26	HP
37	IO_L13P_T2_MRCC_37	D27	HP
37	IO_L13N_T2_MRCC_37	D28	HP
37	IO_L14P_T2_SRCC_37	C28	HP
37	IO_L14N_T2_SRCC_37	C29	HP
37	IO_L15P_T2_DQS_37	B28	HP
37	IO_L15N_T2_DQS_37	B29	HP
37	IO_L16P_T2_37	A31	HP
37	IO_L16N_T2_37	A32	HP
37	IO_L17P_T2_37	A29	HP
37	IO_L17N_T2_37	A30	HP
37	IO_L18P_T2_37	C31	HP
37	IO_L18N_T2_37	B31	HP
37	IO_L19P_T3_37	E30	HP
37	IO_L19N_T3_VREF_37	D31	HP
37	IO_L20P_T3_37	D30	HP
37	IO_L20N_T3_37	C30	HP
37	IO_L21P_T3_DQS_37	E27	HP
37	IO_L21N_T3_DQS_37	E28	HP
37	IO_L22P_T3_37	F29	HP
37	IO_L22N_T3_37	E29	HP
37	IO_L23P_T3_37	F26	HP
37	IO_L23N_T3_37	F27	HP
37	IO_L24P_T3_37	F30	HP
37	IO_L24N_T3_37	F31	HP
37	IO_25_VRP_37	F24	HP
38	IO_0_VRN_38	K18	HP
38	IO_L1P_T0_38	C19	HP
38	IO_L1N_T0_38	B19	HP
38	IO_L2P_T0_38	A16	HP
38	IO_L2N_T0_38	A15	HP
38	IO_L3P_T0_DQS_38	A20	HP
38	IO_L3N_T0_DQS_38	A19	HP
38	IO_L4P_T0_38	B17	HP
38	IO_L4N_T0_38	A17	HP
38	IO_L5P_T0_38	B21	HP

Bank	Pin name	Pin	I/O Type
38	IO_L5N_T0_38	A21	HP
38	IO_L6P_T0_38	C18	HP
38	IO_L6N_T0_VREF_38	B18	HP
38	IO_L7P_T1_38	D20	HP
38	IO_L7N_T1_38	C20	HP
38	IO_L8P_T1_38	F17	HP
38	IO_L8N_T1_38	E17	HP
38	IO_L9P_T1_DQS_38	D21	HP
38	IO_L9N_T1_DQS_38	C21	HP
38	IO_L10P_T1_38	D18	HP
38	IO_L10N_T1_38	D17	HP
38	IO_L11P_T1_SRCC_38	G19	HP
38	IO_L11N_T1_SRCC_38	F19	HP
38	IO_L12P_T1_MRCC_38	E19	HP
38	IO_L12N_T1_MRCC_38	E18	HP
38	IO_L13P_T2_MRCC_38	H19	HP
38	IO_L13N_T2_MRCC_38	G18	HP
38	IO_L14P_T2_SRCC_38	K19	HP
38	IO_L14N_T2_SRCC_38	J18	HP
38	IO_L15P_T2_DQS_38	F20	HP
38	IO_L15N_T2_DQS_38	E20	HP
38	IO_L16P_T2_38	K17	HP
38	IO_L16N_T2_38	J17	HP
38	IO_L17P_T2_38	J20	HP
38	IO_L17N_T2_38	H20	HP
38	IO_L18P_T2_38	H18	HP
38	IO_L18N_T2_38	G17	HP
38	IO_L19P_T3_38	P18	HP
38	IO_L19N_T3_VREF_38	P17	HP
38	IO_L20P_T3_38	M17	HP
38	IO_L20N_T3_38	L17	HP
38	IO_L21P_T3_DQS_38	N19	HP
38	IO_L21N_T3_DQS_38	N18	HP
38	IO_L22P_T3_38	M19	HP
38	IO_L22N_T3_38	M18	HP
38	IO_L23P_T3_38	P20	HP
38	IO_L23N_T3_38	N20	HP
38	IO_L24P_T3_38	L20	HP
38	IO_L24N_T3_38	L19	HP
38	IO_25_VRP_38	K20	HP

Bank	Pin name	Pin	I/O Type
39	IO_0_VRN_39	J16	HP
39	IO_L1P_T0_39	C16	HP
39	IO_L1N_T0_39	B16	HP
39	IO_L2P_T0_39	B14	HP
39	IO_L2N_T0_39	A14	HP
39	IO_L3P_T0_DQS_39	C15	HP
39	IO_L3N_T0_DQS_39	C14	HP
39	IO_L4P_T0_39	D13	HP
39	IO_L4N_T0_39	C13	HP
39	IO_L5P_T0_39	D16	HP
39	IO_L5N_T0_39	D15	HP
39	IO_L6P_T0_39	E12	HP
39	IO_L6N_T0_VREF_39	D12	HP
39	IO_L7P_T1_39	F16	HP
39	IO_L7N_T1_39	E15	HP
39	IO_L8P_T1_39	E14	HP
39	IO_L8N_T1_39	E13	HP
39	IO_L9P_T1_DQS_39	H16	HP
39	IO_L9N_T1_DQS_39	G16	HP
39	IO_L10P_T1_39	G12	HP
39	IO_L10N_T1_39	F12	HP
39	IO_L11P_T1_SRCC_39	F15	HP
39	IO_L11N_T1_SRCC_39	F14	HP
39	IO_L12P_T1_MRCC_39	G14	HP
39	IO_L12N_T1_MRCC_39	G13	HP
39	IO_L13P_T2_MRCC_39	H15	HP
39	IO_L13N_T2_MRCC_39	H14	HP
39	IO_L14P_T2_SRCC_39	J13	HP
39	IO_L14N_T2_SRCC_39	H13	HP
39	IO_L15P_T2_DQS_39	K12	HP
39	IO_L15N_T2_DQS_39	J12	HP
39	IO_L16P_T2_39	K15	HP
39	IO_L16N_T2_39	J15	HP
39	IO_L17P_T2_39	K14	HP
39	IO_L17N_T2_39	K13	HP
39	IO_L18P_T2_39	L16	HP
39	IO_L18N_T2_39	L15	HP
39	IO_L19P_T3_39	L12	HP
39	IO_L19N_T3_VREF_39	L11	HP
39	IO_L20P_T3_39	M14	HP

Bank	Pin name	Pin	I/O Type
39	IO_L20N_T3_39	L14	HP
39	IO_L21P_T3_DQS_39	N16	HP
39	IO_L21N_T3_DQS_39	M16	HP
39	IO_L22P_T3_39	N13	HP
39	IO_L22N_T3_39	M13	HP
39	IO_L23P_T3_39	N15	HP
39	IO_L23N_T3_39	N14	HP
39	IO_L24P_T3_39	M12	HP
39	IO_L24N_T3_39	M11	HP
39	IO_25_VRP_39	J11	HP
NA	NC	AW2	NA
NA	NC	AW6	NA
NA	NC	AW1	NA
NA	NC	AW5	NA
NA	NC	AY4	NA
NA	NC	AY8	NA
NA	NC	AY3	NA
NA	NC	AW10	NA
NA	NC	AY7	NA
NA	NC	AW9	NA
NA	NC	BA9	NA
NA	NC	BA10	NA
NA	NC	BA2	NA
NA	NC	BA6	NA
NA	NC	BA1	NA
NA	NC	BA5	NA
NA	NC	BB4	NA
NA	NC	BB8	NA
NA	NC	BB3	NA
NA	NC	BB7	NA
NA	NC	AR2	NA
NA	NC	AP8	NA
NA	NC	AR1	NA
NA	NC	AP7	NA
NA	NC	AT4	NA
NA	NC	AR6	NA
NA	NC	AT3	NA
NA	NC	AT8	NA
NA	NC	AR5	NA
NA	NC	AT7	NA

Bank	Pin name	Pin	I/O Type
NA	NC	AU9	NA
NA	NC	AU10	NA
NA	NC	AU2	NA
NA	NC	AU6	NA
NA	NC	AU1	NA
NA	NC	AU5	NA
NA	NC	AV4	NA
NA	NC	AV8	NA
NA	NC	AV3	NA
NA	NC	AV7	NA
113	MGTHTXP3_113	AL2	GTH
113	MGTHRXP3_113	AJ6	GTH
113	MGTHTXN3_113	AL1	GTH
113	MGTHRXN3_113	AJ5	GTH
113	MGTHTXP2_113	AM4	GTH
113	MGTHRXP2_113	AL6	GTH
113	MGTHTXN2_113	AM3	GTH
113	MGTREFCLK0P_113	AH8	GTH
113	MGTHRXN2_113	AL5	GTH
113	MGTREFCLK0N_113	AH7	GTH
113	MGTREFCLK1N_113	AK7	GTH
113	MGTREFCLK1P_113	AK8	GTH
113	MGTHTXP1_113	AN2	GTH
113	MGTHRXP1_113	AM8	GTH
113	MGTHTXN1_113	AN1	GTH
113	MGTHRXN1_113	AM7	GTH
113	MGTHTXP0_113	AP4	GTH
113	MGTHRXP0_113	AN6	GTH
113	MGTHTXN0_113	AP3	GTH
113	MGTHRXN0_113	AN5	GTH
114	MGTHTXP3_114	AG2	GTH
114	MGTHRXP3_114	AD4	GTH
114	MGTHTXN3_114	AG1	GTH
114	MGTHRXN3_114	AD3	GTH
114	MGTHTXP2_114	AH4	GTH
114	MGTHRXP2_114	AE6	GTH
114	MGTHTXN2_114	AH3	GTH
114	MGTREFCLK0P_114	AD8	GTH
114	MGTHRXN2_114	AE5	GTH
114	MGTREFCLK0N_114	AD7	GTH

Bank	Pin name	Pin	I/O Type
114	MGTREFCLK1N_114	AF7	GTH
114	MGTREFCLK1P_114	AF8	GTH
114	MGTHTXP1_114	AJ2	GTH
114	MGTHRXP1_114	AF4	GTH
114	MGTHTXN1_114	AJ1	GTH
114	MGTHRXN1_114	AF3	GTH
114	MGTHTXP0_114	AK4	GTH
114	MGTHRXP0_114	AG6	GTH
114	MGTHTXN0_114	AK3	GTH
114	MGTHRXN0_114	AG5	GTH
115	MGTHTXP3_115	W2	GTH
115	MGTHRXP3_115	Y4	GTH
115	MGTHTXN3_115	W1	GTH
115	MGTHRXN3_115	Y3	GTH
115	MGTHTXP2_115	AA2	GTH
115	MGTHRXP2_115	AA6	GTH
115	MGTHTXN2_115	AA1	GTH
115	MGTREFCLK0P_115	Y8	GTH
115	MGTHRXN2_115	AA5	GTH
115	MGTAVTTRCAL_115	A12	GTH
115	MGTREFCLK0N_115	Y7	GTH
115	MGTRREF_115	B11	GTH
115	MGTREFCLK1N_115	AB7	GTH
115	MGTREFCLK1P_115	AB8	GTH
115	MGTHTXP1_115	AC2	GTH
115	MGTHRXP1_115	AB4	GTH
115	MGTHTXN1_115	AC1	GTH
115	MGTHRXN1_115	AB3	GTH
115	MGTHTXP0_115	AE2	GTH
115	MGTHRXP0_115	AC6	GTH
115	MGTHTXN0_115	AE1	GTH
115	MGTHRXN0_115	AC5	GTH
116	MGTHTXP3_116	P4	GTH
116	MGTHRXP3_116	R6	GTH
116	MGTHTXN3_116	P3	GTH
116	MGTHRXN3_116	R5	GTH
116	MGTHTXP2_116	R2	GTH
116	MGTHRXP2_116	U6	GTH
116	MGTHTXN2_116	R1	GTH
116	MGTREFCLK0P_116	T8	GTH

Bank	Pin name	Pin	I/O Type
116	MGTHRXN2_116	U5	GTH
116	MGTREFCLK0N_116	T7	GTH
116	MGTREFCLK1N_116	V7	GTH
116	MGTREFCLK1P_116	V8	GTH
116	MGTHTXP1_116	T4	GTH
116	MGTHRXP1_116	V4	GTH
116	MGTHTXN1_116	T3	GTH
116	MGTHRXN1_116	V3	GTH
116	MGTHTXP0_116	U2	GTH
116	MGTHRXP0_116	W6	GTH
116	MGTHTXN0_116	U1	GTH
116	MGTHRXN0_116	W5	GTH
117	MGTHTXP3_117	K4	GTH
117	MGTHRXP3_117	J6	GTH
117	MGTHTXN3_117	K3	GTH
117	MGTHRXN3_117	J5	GTH
117	MGTHTXP2_117	L2	GTH
117	MGTHRXP2_117	L6	GTH
117	MGTHTXN2_117	L1	GTH
117	MGTREFCLK0P_117	K8	GTH
117	MGTHRXN2_117	L5	GTH
117	MGTREFCLK0N_117	K7	GTH
117	MGTREFCLK1N_117	M7	GTH
117	MGTREFCLK1P_117	M8	GTH
117	MGTHTXP1_117	M4	GTH
117	MGTHRXP1_117	N6	GTH
117	MGTHTXN1_117	M3	GTH
117	MGTHRXN1_117	N5	GTH
117	MGTHTXP0_117	N2	GTH
117	MGTHRXP0_117	P8	GTH
117	MGTHTXN0_117	N1	GTH
117	MGTHRXN0_117	P7	GTH
118	MGTHTXP3_118	F4	GTH
118	MGTHRXP3_118	E6	GTH
118	MGTHTXN3_118	F3	GTH
118	MGTHRXN3_118	E5	GTH
118	MGTHTXP2_118	G2	GTH
118	MGTHRXP2_118	F8	GTH
118	MGTHTXN2_118	G1	GTH
118	MGTREFCLK0P_118	E10	GTH

Bank	Pin name	Pin	I/O Type
118	MGTHRXN2_118	F7	GTH
118	MGTREFCLK0N_118	E9	GTH
118	MGTREFCLK1N_118	G9	GTH
118	MGTREFCLK1P_118	G10	GTH
118	MGTHTXP1_118	H4	GTH
118	MGTHRXP1_118	G6	GTH
118	MGTHTXN1_118	H3	GTH
118	MGTHRXN1_118	G5	GTH
118	MGTHTXP0_118	J2	GTH
118	MGTHRXP0_118	H8	GTH
118	MGTHTXN0_118	J1	GTH
118	MGTHRXN0_118	H7	GTH
119	MGTHTXP3_119	B4	GTH
119	MGTHRXP3_119	A6	GTH
119	MGTHTXN3_119	B3	GTH
119	MGTHRXN3_119	A5	GTH
119	MGTHTXP2_119	C2	GTH
119	MGTHRXP2_119	B8	GTH
119	MGTHTXN2_119	C1	GTH
119	MGTREFCLK0P_119	A10	GTH
119	MGTHRXN2_119	B7	GTH
119	MGTREFCLK0N_119	A9	GTH
119	MGTREFCLK1N_119	C9	GTH
119	MGTREFCLK1P_119	C10	GTH
119	MGTHTXP1_119	D4	GTH
119	MGTHRXP1_119	C6	GTH
119	MGTHTXN1_119	D3	GTH
119	MGTHRXN1_119	C5	GTH
119	MGTHTXP0_119	E2	GTH
119	MGTHRXP0_119	D8	GTH
119	MGTHTXN0_119	E1	GTH
119	MGTHRXN0_119	D7	GTH
NA	MGTAVCC_G11	C8	NA
NA	MGTAVCC_G11	E8	NA
NA	MGTAVCC_G11	G8	NA
NA	MGTAVCC_G11	J8	NA
NA	MGTAVCC_G11	L8	NA
NA	MGTAVCC_G10	AA8	NA
NA	MGTAVCC_G10	AC8	NA
NA	MGTAVCC_G10	AE8	NA

Bank	Pin name	Pin	I/O Type
NA	MGTAVCC_G10	AJ8	NA
NA	MGTAVCC_G10	AL8	NA
NA	MGTAVCC_G10	AN8	NA
NA	MGTAVCC_G10	AR8	NA
NA	MGTAVCC_G10	AU8	NA
NA	MGTAVCC_G10	AW8	NA
NA	MGTAVCC_G10	BA8	NA
NA	MGTAVCC_G10	W8	NA
NA	MGTAVTT_G11	B6	NA
NA	MGTAVTT_G11	C4	NA
NA	MGTAVTT_G11	D6	NA
NA	MGTAVTT_G11	E4	NA
NA	MGTAVTT_G11	F6	NA
NA	MGTAVTT_G11	G4	NA
NA	MGTAVTT_G11	H6	NA
NA	MGTAVTT_G11	J4	NA
NA	MGTAVTT_G11	L4	NA
NA	MGTAVTT_G11	N4	NA
NA	MGTAVTT_G11	P6	NA
NA	MGTAVTT_G10	R4	NA
NA	MGTAVTT_G10	W4	NA
NA	MGTAVTT_G10	AA4	NA
NA	MGTAVTT_G10	AC4	NA
NA	MGTAVTT_G10	AE4	NA
NA	MGTAVTT_G10	AJ4	NA
NA	MGTAVTT_G10	AL4	NA
NA	MGTAVTT_G10	AM6	NA
NA	MGTAVTT_G10	AN4	NA
NA	MGTAVTT_G10	AP6	NA
NA	MGTAVTT_G10	AR4	NA
NA	MGTAVTT_G10	AU4	NA
NA	MGTAVTT_G10	AV6	NA
NA	MGTAVTT_G10	AW4	NA
NA	MGTAVTT_G10	AY6	NA
NA	MGTAVTT_G10	BA4	NA
NA	MGTVCCAUX_G11	N8	NA
NA	MGTVCCAUX_G10	R8	NA
NA	MGTVCCAUX_G10	U8	NA
NA	GND	A2	NA
NA	GND	A3	NA

Bank	Pin name	Pin	I/O Type
NA	GND	A4	NA
NA	GND	A7	NA
NA	GND	A8	NA
NA	GND	A11	NA
NA	GND	A13	NA
NA	GND	A18	NA
NA	GND	A28	NA
NA	GND	A38	NA
NA	GND	AA3	NA
NA	GND	AA7	NA
NA	GND	AA9	NA
NA	GND	AA11	NA
NA	GND	AA13	NA
NA	GND	AA15	NA
NA	GND	AA17	NA
NA	GND	AA19	NA
NA	GND	AA23	NA
NA	GND	AA25	NA
NA	GND	AA27	NA
NA	GND	AA38	NA
NA	GND	AB1	NA
NA	GND	AB2	NA
NA	GND	AB5	NA
NA	GND	AB6	NA
NA	GND	AB9	NA
NA	GND	AB10	NA
NA	GND	AB12	NA
NA	GND	AB14	NA
NA	GND	AB16	NA
NA	GND	AB18	NA
NA	GND	AB22	NA
NA	GND	AB24	NA
NA	GND	AB26	NA
NA	GND	AB28	NA
NA	GND	AB35	NA
NA	GND	AC3	NA
NA	GND	AC7	NA
NA	GND	AC11	NA
NA	GND	AC13	NA
NA	GND	AC15	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AC17	NA
NA	GND	AC19	NA
NA	GND	AC23	NA
NA	GND	AC25	NA
NA	GND	AC27	NA
NA	GND	AC32	NA
NA	GND	AC42	NA
NA	GND	AD1	NA
NA	GND	AD2	NA
NA	GND	AD5	NA
NA	GND	AD6	NA
NA	GND	AD9	NA
NA	GND	AD10	NA
NA	GND	AD12	NA
NA	GND	AD14	NA
NA	GND	AD16	NA
NA	GND	AD18	NA
NA	GND	AD20	NA
NA	GND	AD22	NA
NA	GND	AD24	NA
NA	GND	AD26	NA
NA	GND	AD28	NA
NA	GND	AD29	NA
NA	GND	AD39	NA
NA	GND	AE3	NA
NA	GND	AE7	NA
NA	GND	AE9	NA
NA	GND	AE11	NA
NA	GND	AE13	NA
NA	GND	AE15	NA
NA	GND	AE17	NA
NA	GND	AE19	NA
NA	GND	AE21	NA
NA	GND	AE23	NA
NA	GND	AE25	NA
NA	GND	AE27	NA
NA	GND	AE36	NA
NA	GND	AF1	NA
NA	GND	AF2	NA
NA	GND	AF5	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AF6	NA
NA	GND	AF9	NA
NA	GND	AF10	NA
NA	GND	AF12	NA
NA	GND	AF14	NA
NA	GND	AF16	NA
NA	GND	AF18	NA
NA	GND	AF20	NA
NA	GND	AF22	NA
NA	GND	AF24	NA
NA	GND	AF26	NA
NA	GND	AF33	NA
NA	GND	AG3	NA
NA	GND	AG4	NA
NA	GND	AG7	NA
NA	GND	AG8	NA
NA	GND	AG9	NA
NA	GND	AG10	NA
NA	GND	AG13	NA
NA	GND	AG15	NA
NA	GND	AG17	NA
NA	GND	AG19	NA
NA	GND	AG21	NA
NA	GND	AG23	NA
NA	GND	AG25	NA
NA	GND	AG27	NA
NA	GND	AG30	NA
NA	GND	AG40	NA
NA	GND	AH1	NA
NA	GND	AH2	NA
NA	GND	AH5	NA
NA	GND	AH6	NA
NA	GND	AH9	NA
NA	GND	AH12	NA
NA	GND	AH14	NA
NA	GND	AH16	NA
NA	GND	AH17	NA
NA	GND	AH18	NA
NA	GND	AH20	NA
NA	GND	AH22	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AH24	NA
NA	GND	AH26	NA
NA	GND	AH37	NA
NA	GND	AJ3	NA
NA	GND	AJ7	NA
NA	GND	AJ9	NA
NA	GND	AJ14	NA
NA	GND	AJ24	NA
NA	GND	AJ27	NA
NA	GND	AJ34	NA
NA	GND	AK1	NA
NA	GND	AK2	NA
NA	GND	AK5	NA
NA	GND	AK6	NA
NA	GND	AK9	NA
NA	GND	AK11	NA
NA	GND	AK21	NA
NA	GND	AK31	NA
NA	GND	AK41	NA
NA	GND	AL3	NA
NA	GND	AL7	NA
NA	GND	AL9	NA
NA	GND	AL18	NA
NA	GND	AL28	NA
NA	GND	AL38	NA
NA	GND	AM1	NA
NA	GND	AM2	NA
NA	GND	AM5	NA
NA	GND	AM9	NA
NA	GND	AM10	NA
NA	GND	AM15	NA
NA	GND	AM25	NA
NA	GND	AM35	NA
NA	GND	AN3	NA
NA	GND	AN7	NA
NA	GND	AN9	NA
NA	GND	AN10	NA
NA	GND	AN12	NA
NA	GND	AN22	NA
NA	GND	AN32	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AN42	NA
NA	GND	AP1	NA
NA	GND	AP2	NA
NA	GND	AP5	NA
NA	GND	AP9	NA
NA	GND	AP10	NA
NA	GND	AP19	NA
NA	GND	AP29	NA
NA	GND	AP39	NA
NA	GND	AR3	NA
NA	GND	AR7	NA
NA	GND	AR9	NA
NA	GND	AR10	NA
NA	GND	AR16	NA
NA	GND	AR26	NA
NA	GND	AR36	NA
NA	GND	AT1	NA
NA	GND	AT2	NA
NA	GND	AT5	NA
NA	GND	AT6	NA
NA	GND	AT9	NA
NA	GND	AT10	NA
NA	GND	AT11	NA
NA	GND	AT13	NA
NA	GND	AT23	NA
NA	GND	AT33	NA
NA	GND	AU3	NA
NA	GND	AU7	NA
NA	GND	AU11	NA
NA	GND	AU20	NA
NA	GND	AU30	NA
NA	GND	AU40	NA
NA	GND	AV1	NA
NA	GND	AV2	NA
NA	GND	AV5	NA
NA	GND	AV9	NA
NA	GND	AV10	NA
NA	GND	AV11	NA
NA	GND	AV17	NA
NA	GND	AV27	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AV37	NA
NA	GND	AW3	NA
NA	GND	AW7	NA
NA	GND	AW11	NA
NA	GND	AW14	NA
NA	GND	AW24	NA
NA	GND	AW34	NA
NA	GND	AY1	NA
NA	GND	AY2	NA
NA	GND	AY5	NA
NA	GND	AY9	NA
NA	GND	AY10	NA
NA	GND	AY11	NA
NA	GND	AY21	NA
NA	GND	AY31	NA
NA	GND	AY41	NA
NA	GND	B1	NA
NA	GND	B2	NA
NA	GND	B5	NA
NA	GND	B9	NA
NA	GND	B10	NA
NA	GND	B12	NA
NA	GND	B13	NA
NA	GND	B15	NA
NA	GND	B25	NA
NA	GND	B35	NA
NA	GND	BA3	NA
NA	GND	BA7	NA
NA	GND	BA11	NA
NA	GND	BA18	NA
NA	GND	BA28	NA
NA	GND	BA38	NA
NA	GND	BB2	NA
NA	GND	BB5	NA
NA	GND	BB6	NA
NA	GND	BB9	NA
NA	GND	BB10	NA
NA	GND	BB11	NA
NA	GND	BB15	NA
NA	GND	BB25	NA

Bank	Pin name	Pin	I/O Type
NA	GND	BB35	NA
NA	GND	C3	NA
NA	GND	C7	NA
NA	GND	C11	NA
NA	GND	C12	NA
NA	GND	C22	NA
NA	GND	C32	NA
NA	GND	C42	NA
NA	GND	D1	NA
NA	GND	D2	NA
NA	GND	D5	NA
NA	GND	D9	NA
NA	GND	D10	NA
NA	GND	D11	NA
NA	GND	D19	NA
NA	GND	D29	NA
NA	GND	D39	NA
NA	GND	E3	NA
NA	GND	E7	NA
NA	GND	E11	NA
NA	GND	E16	NA
NA	GND	E26	NA
NA	GND	E36	NA
NA	GND	F1	NA
NA	GND	F2	NA
NA	GND	F5	NA
NA	GND	F9	NA
NA	GND	F10	NA
NA	GND	F11	NA
NA	GND	F13	NA
NA	GND	F23	NA
NA	GND	F33	NA
NA	GND	G3	NA
NA	GND	G7	NA
NA	GND	G11	NA
NA	GND	G20	NA
NA	GND	G30	NA
NA	GND	G40	NA
NA	GND	H1	NA
NA	GND	H2	NA

Bank	Pin name	Pin	I/O Type
NA	GND	H5	NA
NA	GND	H9	NA
NA	GND	H10	NA
NA	GND	H11	NA
NA	GND	H17	NA
NA	GND	H27	NA
NA	GND	H37	NA
NA	GND	J3	NA
NA	GND	J7	NA
NA	GND	J9	NA
NA	GND	J10	NA
NA	GND	J14	NA
NA	GND	J24	NA
NA	GND	J34	NA
NA	GND	K1	NA
NA	GND	K2	NA
NA	GND	K5	NA
NA	GND	K6	NA
NA	GND	K9	NA
NA	GND	K10	NA
NA	GND	K11	NA
NA	GND	K21	NA
NA	GND	K31	NA
NA	GND	K41	NA
NA	GND	L3	NA
NA	GND	L7	NA
NA	GND	L9	NA
NA	GND	L10	NA
NA	GND	L18	NA
NA	GND	L28	NA
NA	GND	L38	NA
NA	GND	M1	NA
NA	GND	M2	NA
NA	GND	M5	NA
NA	GND	M6	NA
NA	GND	M9	NA
NA	GND	M15	NA
NA	GND	M25	NA
NA	GND	M35	NA
NA	GND	N3	NA

Bank	Pin name	Pin	I/O Type
NA	GND	N7	NA
NA	GND	N9	NA
NA	GND	N12	NA
NA	GND	N22	NA
NA	GND	N32	NA
NA	GND	N42	NA
NA	GND	P1	NA
NA	GND	P2	NA
NA	GND	P5	NA
NA	GND	P9	NA
NA	GND	P12	NA
NA	GND	P16	NA
NA	GND	P19	NA
NA	GND	P29	NA
NA	GND	P39	NA
NA	GND	R3	NA
NA	GND	R7	NA
NA	GND	R9	NA
NA	GND	R11	NA
NA	GND	R13	NA
NA	GND	R15	NA
NA	GND	R17	NA
NA	GND	R19	NA
NA	GND	R21	NA
NA	GND	R23	NA
NA	GND	R25	NA
NA	GND	R27	NA
NA	GND	R36	NA
NA	GND	T1	NA
NA	GND	T2	NA
NA	GND	T5	NA
NA	GND	T6	NA
NA	GND	T9	NA
NA	GND	T12	NA
NA	GND	T14	NA
NA	GND	T16	NA
NA	GND	T18	NA
NA	GND	T20	NA
NA	GND	T22	NA
NA	GND	T24	NA

Bank	Pin name	Pin	I/O Type
NA	GND	T26	NA
NA	GND	T33	NA
NA	GND	U3	NA
NA	GND	U4	NA
NA	GND	U7	NA
NA	GND	U9	NA
NA	GND	U10	NA
NA	GND	U11	NA
NA	GND	U13	NA
NA	GND	U15	NA
NA	GND	U17	NA
NA	GND	U19	NA
NA	GND	U21	NA
NA	GND	U23	NA
NA	GND	U25	NA
NA	GND	U27	NA
NA	GND	U30	NA
NA	GND	U40	NA
NA	GND	V1	NA
NA	GND	V2	NA
NA	GND	V5	NA
NA	GND	V6	NA
NA	GND	V9	NA
NA	GND	V10	NA
NA	GND	V12	NA
NA	GND	V14	NA
NA	GND	V16	NA
NA	GND	V18	NA
NA	GND	V20	NA
NA	GND	V22	NA
NA	GND	V24	NA
NA	GND	V26	NA
NA	GND	V28	NA
NA	GND	V37	NA
NA	GND	W3	NA
NA	GND	W7	NA
NA	GND	W11	NA
NA	GND	W13	NA
NA	GND	W15	NA
NA	GND	W17	NA

Bank	Pin name	Pin	I/O Type
NA	GND	W19	NA
NA	GND	W21	NA
NA	GND	W23	NA
NA	GND	W25	NA
NA	GND	W27	NA
NA	GND	W34	NA
NA	GND	Y1	NA
NA	GND	Y2	NA
NA	GND	Y5	NA
NA	GND	Y6	NA
NA	GND	Y9	NA
NA	GND	Y10	NA
NA	GND	Y12	NA
NA	GND	Y14	NA
NA	GND	Y16	NA
NA	GND	Y18	NA
NA	GND	Y22	NA
NA	GND	Y24	NA
NA	GND	Y26	NA
NA	GND	Y28	NA
NA	GND	Y31	NA
NA	GND	Y41	NA
NA	VCCINT	AA10	NA
NA	VCCINT	AA12	NA
NA	VCCINT	AA14	NA
NA	VCCINT	AA16	NA
NA	VCCINT	AA24	NA
NA	VCCINT	AA28	NA
NA	VCCINT	AB11	NA
NA	VCCINT	AB13	NA
NA	VCCINT	AB15	NA
NA	VCCINT	AB19	NA
NA	VCCINT	AB23	NA
NA	VCCINT	AB27	NA
NA	VCCINT	AC12	NA
NA	VCCINT	AC14	NA
NA	VCCINT	AC16	NA
NA	VCCINT	AC24	NA
NA	VCCINT	AC28	NA
NA	VCCINT	AD11	NA

Bank	Pin name	Pin	I/O Type
NA	VCCINT	AD13	NA
NA	VCCINT	AD15	NA
NA	VCCINT	AD19	NA
NA	VCCINT	AD21	NA
NA	VCCINT	AD23	NA
NA	VCCINT	AD27	NA
NA	VCCINT	AE10	NA
NA	VCCINT	AE12	NA
NA	VCCINT	AE14	NA
NA	VCCINT	AE16	NA
NA	VCCINT	AE20	NA
NA	VCCINT	AE24	NA
NA	VCCINT	AE28	NA
NA	VCCINT	AF11	NA
NA	VCCINT	AF13	NA
NA	VCCINT	AF15	NA
NA	VCCINT	AF21	NA
NA	VCCINT	AF23	NA
NA	VCCINT	AF27	NA
NA	VCCINT	AG12	NA
NA	VCCINT	AG14	NA
NA	VCCINT	AG16	NA
NA	VCCINT	AG20	NA
NA	VCCINT	AG24	NA
NA	VCCINT	AG28	NA
NA	VCCINT	AH11	NA
NA	VCCINT	AH13	NA
NA	VCCINT	AH15	NA
NA	VCCINT	AH19	NA
NA	VCCINT	AH23	NA
NA	VCCINT	AH27	NA
NA	VCCINT	P13	NA
NA	VCCINT	P15	NA
NA	VCCINT	P27	NA
NA	VCCINT	R12	NA
NA	VCCINT	R14	NA
NA	VCCINT	R16	NA
NA	VCCINT	R20	NA
NA	VCCINT	R24	NA
NA	VCCINT	T13	NA

Bank	Pin name	Pin	I/O Type
NA	VCCINT	T15	NA
NA	VCCINT	T21	NA
NA	VCCINT	T23	NA
NA	VCCINT	T27	NA
NA	VCCINT	U12	NA
NA	VCCINT	U14	NA
NA	VCCINT	U16	NA
NA	VCCINT	U20	NA
NA	VCCINT	U24	NA
NA	VCCINT	V11	NA
NA	VCCINT	V13	NA
NA	VCCINT	V15	NA
NA	VCCINT	V19	NA
NA	VCCINT	V21	NA
NA	VCCINT	V23	NA
NA	VCCINT	V27	NA
NA	VCCINT	W12	NA
NA	VCCINT	W14	NA
NA	VCCINT	W16	NA
NA	VCCINT	W20	NA
NA	VCCINT	W24	NA
NA	VCCINT	W28	NA
NA	VCCINT	Y11	NA
NA	VCCINT	Y13	NA
NA	VCCINT	Y15	NA
NA	VCCINT	Y19	NA
NA	VCCINT	Y23	NA
NA	VCCINT	Y27	NA
NA	VCCAUX	AA26	NA
NA	VCCAUX	AB17	NA
NA	VCCAUX	AC26	NA
NA	VCCAUX	AD17	NA
NA	VCCAUX	AE26	NA
NA	VCCAUX	AF17	NA
NA	VCCAUX	AG26	NA
NA	VCCAUX	T17	NA
NA	VCCAUX	U26	NA
NA	VCCAUX	V17	NA
NA	VCCAUX	W26	NA
NA	VCCAUX	Y17	NA

Bank	Pin name	Pin	I/O Type
NA	VCCAUX_IO_G1	AD25	NA
NA	VCCAUX_IO_G1	AB25	NA
NA	VCCAUX_IO_G1	Y25	NA
NA	VCCAUX_IO_G2	V25	NA
NA	VCCAUX_IO_G2	T25	NA
NA	VCCAUX_IO_G2	R26	NA
NA	VCCAUX_IO_G3	AG18	NA
NA	VCCAUX_IO_G3	AF19	NA
NA	VCCAUX_IO_G3	AE18	NA
NA	VCCAUX_IO_G4	AC18	NA
NA	VCCAUX_IO_G4	AA18	NA
NA	VCCAUX_IO_G4	W18	NA
NA	VCCAUX_IO_G5	U18	NA
NA	VCCAUX_IO_G5	T19	NA
NA	VCCAUX_IO_G5	R18	NA
14	VCCO_14	AF28	NA
14	VCCO_14	AH32	NA
14	VCCO_14	AJ29	NA
14	VCCO_14	AK36	NA
14	VCCO_14	AL33	NA
14	VCCO_14	AM30	NA
14	VCCO_14	AN37	NA
15	VCCO_15	AM40	NA
15	VCCO_15	AR41	NA
15	VCCO_15	AT38	NA
15	VCCO_15	AV42	NA
15	VCCO_15	AW39	NA
15	VCCO_15	BB40	NA
16	VCCO_16	AA33	NA
16	VCCO_16	AB30	NA
16	VCCO_16	AD34	NA
16	VCCO_16	AE31	NA
16	VCCO_16	AG35	NA
16	VCCO_16	Y36	NA
17	VCCO_17	AB40	NA
17	VCCO_17	AC37	NA
17	VCCO_17	AE41	NA
17	VCCO_17	AF38	NA
17	VCCO_17	AH42	NA
17	VCCO_17	AJ39	NA

Bank	Pin name	Pin	I/O Type
18	VCCO_18	P34	NA
18	VCCO_18	T38	NA
18	VCCO_18	U35	NA
18	VCCO_18	V32	NA
18	VCCO_18	V42	NA
18	VCCO_18	W39	NA
19	VCCO_19	B40	NA
19	VCCO_19	E41	NA
19	VCCO_19	H42	NA
19	VCCO_19	J39	NA
19	VCCO_19	M40	NA
19	VCCO_19	N37	NA
19	VCCO_19	R41	NA
31	VCCO_31	AK16	NA
31	VCCO_31	AL13	NA
31	VCCO_31	AP14	NA
31	VCCO_31	AR11	NA
31	VCCO_31	AU15	NA
31	VCCO_31	AV12	NA
31	VCCO_31	BA13	NA
32	VCCO_32	AJ19	NA
32	VCCO_32	AN17	NA
32	VCCO_32	AT18	NA
32	VCCO_32	AW19	NA
32	VCCO_32	AY16	NA
32	VCCO_32	BB20	NA
33	VCCO_33	AL23	NA
33	VCCO_33	AM20	NA
33	VCCO_33	AP24	NA
33	VCCO_33	AR21	NA
33	VCCO_33	AV22	NA
33	VCCO_33	BA23	NA
34	VCCO_34	H32	NA
34	VCCO_34	L33	NA
34	VCCO_34	M30	NA
34	VCCO_34	R31	NA
34	VCCO_34	T28	NA
34	VCCO_34	W29	NA
35	VCCO_35	A33	NA
35	VCCO_35	C37	NA

Bank	Pin name	Pin	I/O Type
35	VCCO_35	D34	NA
35	VCCO_35	E31	NA
35	VCCO_35	F38	NA
35	VCCO_35	G35	NA
35	VCCO_35	K36	NA
36	VCCO_36	G25	NA
36	VCCO_36	H22	NA
36	VCCO_36	J29	NA
36	VCCO_36	K26	NA
36	VCCO_36	L23	NA
36	VCCO_36	N27	NA
36	VCCO_36	P24	NA
37	VCCO_37	A23	NA
37	VCCO_37	B30	NA
37	VCCO_37	C27	NA
37	VCCO_37	D24	NA
37	VCCO_37	E21	NA
37	VCCO_37	F28	NA
38	VCCO_38	B20	NA
38	VCCO_38	C17	NA
38	VCCO_38	F18	NA
38	VCCO_38	J19	NA
38	VCCO_38	M20	NA
38	VCCO_38	N17	NA
39	VCCO_39	D14	NA
39	VCCO_39	G15	NA
39	VCCO_39	H12	NA
39	VCCO_39	K16	NA
39	VCCO_39	L13	NA
39	VCCO_39	P14	NA
0	VCCO_0	M10	NA
0	VCCO_0	T11	NA
12	VCCO_12	AK26	NA
12	VCCO_12	AN27	NA
12	VCCO_12	AT28	NA
12	VCCO_12	AU25	NA
12	VCCO_12	AW29	NA
12	VCCO_12	AY26	NA
13	VCCO_13	AP34	NA
13	VCCO_13	AR31	NA

Bank	Pin name	Pin	I/O Type
13	VCCO_13	AU35	NA
13	VCCO_13	AV32	NA
13	VCCO_13	AY36	NA
13	VCCO_13	BA33	NA
13	VCCO_13	BB30	NA
NA	VCCBRAM	AA22	NA
NA	VCCBRAM	AC22	NA
NA	VCCBRAM	AE22	NA
NA	VCCBRAM	AG22	NA
NA	VCCBRAM	AH21	NA
NA	VCCBRAM	R22	NA
NA	VCCBRAM	U22	NA
NA	VCCBRAM	W22	NA
NA	NC	W9	NA
NA	NC	W10	NA
NA	NC	AC9	NA
NA	NC	AC10	NA
NA	NC	AH25	NA
NA	NC	AF25	NA

Table 2 BQ7VX690TBG1761-PBGA1761 Pinout

Bank	Pin name	Pin	I/O Type
0	DXN_0	AC20	CONFIG
0	VCCADC_0	Y21	CONFIG
0	GNDADC_0	Y20	CONFIG
0	DXP_0	AC21	CONFIG
0	VREFN_0	AA20	CONFIG
0	VREFP_0	AB21	CONFIG
0	VP_0	AA21	CONFIG
0	VN_0	AB20	CONFIG
0	VCCBATT_0	N11	CONFIG
0	CCLK_0	N10	CONFIG
0	TCK_0	P10	CONFIG
0	TMS_0	P11	CONFIG
0	TDO_0	R10	CONFIG
0	TDI_0	T10	CONFIG
0	INIT_B_0	AG11	CONFIG
0	PROGRAM_B_0	AJ11	CONFIG
0	CFGBVS_0	AH10	CONFIG
0	DONE_0	AL11	CONFIG

Bank	Pin name	Pin	I/O Type
0	M2_0	AJ10	CONFIG
0	M0_0	AL10	CONFIG
0	M1_0	AK10	CONFIG
12	IO_0_VRN_12	AN29	HP
12	IO_L1P_T0_12	AY27	HP
12	IO_L1N_T0_12	AY28	HP
12	IO_L2P_T0_12	AU29	HP
12	IO_L2N_T0_12	AV29	HP
12	IO_L3P_T0_DQS_12	BA26	HP
12	IO_L3N_T0_DQS_12	BA27	HP
12	IO_L4P_T0_12	BB28	HP
12	IO_L4N_T0_12	BB29	HP
12	IO_L5P_T0_12	BB26	HP
12	IO_L5N_T0_12	BB27	HP
12	IO_L6P_T0_12	AY29	HP
12	IO_L6N_T0_VREF_12	BA29	HP
12	IO_L7P_T1_12	AW25	HP
12	IO_L7N_T1_12	AW26	HP
12	IO_L8P_T1_12	AR29	HP
12	IO_L8N_T1_12	AT29	HP
12	IO_L9P_T1_DQS_12	AV25	HP
12	IO_L9N_T1_DQS_12	AV26	HP
12	IO_L10P_T1_12	AW27	HP
12	IO_L10N_T1_12	AW28	HP
12	IO_L11P_T1_SRCC_12	AU28	HP
12	IO_L11N_T1_SRCC_12	AV28	HP
12	IO_L12P_T1_MRCC_12	AU26	HP
12	IO_L12N_T1_MRCC_12	AU27	HP
12	IO_L13P_T2_MRCC_12	AR27	HP
12	IO_L13N_T2_MRCC_12	AT27	HP
12	IO_L14P_T2_SRCC_12	AP27	HP
12	IO_L14N_T2_SRCC_12	AR28	HP
12	IO_L15P_T2_DQS_12	AN28	HP
12	IO_L15N_T2_DQS_12	AP28	HP
12	IO_L16P_T2_12	AT25	HP
12	IO_L16N_T2_12	AT26	HP
12	IO_L17P_T2_12	AP25	HP
12	IO_L17N_T2_12	AR25	HP
12	IO_L18P_T2_12	AN25	HP
12	IO_L18N_T2_12	AN26	HP

Bank	Pin name	Pin	I/O Type
12	IO_L19P_T3_12	AM28	HP
12	IO_L19N_T3_VREF_12	AM29	HP
12	IO_L20P_T3_12	AK27	HP
12	IO_L20N_T3_12	AL27	HP
12	IO_L21P_T3_DQS_12	AM26	HP
12	IO_L21N_T3_DQS_12	AM27	HP
12	IO_L22P_T3_12	AK24	HP
12	IO_L22N_T3_12	AK25	HP
12	IO_L23P_T3_12	AL25	HP
12	IO_L23N_T3_12	AL26	HP
12	IO_L24P_T3_12	AJ25	HP
12	IO_L24N_T3_12	AJ26	HP
12	IO_25_VRP_12	AP26	HP
13	IO_0_VRN_13	AR35	HP
13	IO_L1P_T0_13	AY34	HP
13	IO_L1N_T0_13	BA35	HP
13	IO_L2P_T0_13	AV36	HP
13	IO_L2N_T0_13	AW36	HP
13	IO_L3P_T0_DQS_13	BA34	HP
13	IO_L3N_T0_DQS_13	BB34	HP
13	IO_L4P_T0_13	BA36	HP
13	IO_L4N_T0_13	BB36	HP
13	IO_L5P_T0_13	BB32	HP
13	IO_L5N_T0_13	BB33	HP
13	IO_L6P_T0_13	AW35	HP
13	IO_L6N_T0_VREF_13	AY35	HP
13	IO_L7P_T1_13	AT34	HP
13	IO_L7N_T1_13	AU34	HP
13	IO_L8P_T1_13	AT36	HP
13	IO_L8N_T1_13	AU36	HP
13	IO_L9P_T1_DQS_13	AT32	HP
13	IO_L9N_T1_DQS_13	AU33	HP
13	IO_L10P_T1_13	AR34	HP
13	IO_L10N_T1_13	AT35	HP
13	IO_L11P_T1_SRCC_13	AU32	HP
13	IO_L11N_T1_SRCC_13	AV33	HP
13	IO_L12P_T1_MRCC_13	AW32	HP
13	IO_L12N_T1_MRCC_13	AW33	HP
13	IO_L13P_T2_MRCC_13	AV34	HP
13	IO_L13N_T2_MRCC_13	AV35	HP

Bank	Pin name	Pin	I/O Type
13	IO_L14P_T2_SRCC_13	AY32	HP
13	IO_L14N_T2_SRCC_13	AY33	HP
13	IO_L15P_T2_DQS_13	BA31	HP
13	IO_L15N_T2_DQS_13	BA32	HP
13	IO_L16P_T2_13	AW30	HP
13	IO_L16N_T2_13	AY30	HP
13	IO_L17P_T2_13	BA30	HP
13	IO_L17N_T2_13	BB31	HP
13	IO_L18P_T2_13	AV30	HP
13	IO_L18N_T2_13	AW31	HP
13	IO_L19P_T3_13	AR30	HP
13	IO_L19N_T3_VREF_13	AT30	HP
13	IO_L20P_T3_13	AU31	HP
13	IO_L20N_T3_13	AV31	HP
13	IO_L21P_T3_DQS_13	AN30	HP
13	IO_L21N_T3_DQS_13	AP30	HP
13	IO_L22P_T3_13	AP32	HP
13	IO_L22N_T3_13	AR32	HP
13	IO_L23P_T3_13	AN31	HP
13	IO_L23N_T3_13	AP31	HP
13	IO_L24P_T3_13	AP33	HP
13	IO_L24N_T3_13	AR33	HP
13	IO_25_VRP_13	AT31	HP
14	IO_0_VRN_14	AH35	HP
14	IO_L1P_T0_D00_MOSI_14	AM36	HP
14	IO_L1N_T0_D01_DIN_14	AN36	HP
14	IO_L2P_T0_D02_14	AJ36	HP
14	IO_L2N_T0_D03_14	AJ37	HP
14	IO_L3P_T0_DQS_PUDC_B_14	AP36	HP
14	IO_L3N_T0_DQS_EMCCLK_14	AP37	HP
14	IO_L4P_T0_D04_14	AK37	HP
14	IO_L4N_T0_D05_14	AL37	HP
14	IO_L5P_T0_D06_14	AN35	HP
14	IO_L5N_T0_D07_14	AP35	HP
14	IO_L6P_T0_FCS_B_14	AL36	HP
14	IO_L6N_T0_D08_VREF_14	AM37	HP
14	IO_L7P_T1_D09_14	AG33	HP
14	IO_L7N_T1_D10_14	AH33	HP
14	IO_L8P_T1_D11_14	AK35	HP
14	IO_L8N_T1_D12_14	AL35	HP

Bank	Pin name	Pin	I/O Type
14	IO_L9P_T1_DQS_14	AH31	HP
14	IO_L9N_T1_DQS_D13_14	AJ31	HP
14	IO_L10P_T1_D14_14	AH34	HP
14	IO_L10N_T1_D15_14	AJ35	HP
14	IO_L11P_T1_SRCC_14	AJ33	HP
14	IO_L11N_T1_SRCC_14	AK33	HP
14	IO_L12P_T1_MRCC_14	AK34	HP
14	IO_L12N_T1_MRCC_14	AL34	HP
14	IO_L13P_T2_MRCC_14	AJ32	HP
14	IO_L13N_T2_MRCC_14	AK32	HP
14	IO_L14P_T2_SRCC_14	AL31	HP
14	IO_L14N_T2_SRCC_14	AL32	HP
14	IO_L15P_T2_DQS_RDWR_B_14	AM34	HP
14	IO_L15N_T2_DQS_DOUT_CSO_B_14	AN34	HP
14	IO_L16P_T2_CSI_B_14	AM31	HP
14	IO_L16N_T2_A15_D31_14	AM32	HP
14	IO_L17P_T2_A14_D30_14	AM33	HP
14	IO_L17N_T2_A13_D29_14	AN33	HP
14	IO_L18P_T2_A12_D28_14	AL29	HP
14	IO_L18N_T2_A11_D27_14	AL30	HP
14	IO_L19P_T3_A10_D26_14	AH29	HP
14	IO_L19N_T3_A09_D25_VREF_14	AH30	HP
14	IO_L20P_T3_A08_D24_14	AJ30	HP
14	IO_L20N_T3_A07_D23_14	AK30	HP
14	IO_L21P_T3_DQS_14	AF29	HP
14	IO_L21N_T3_DQS_A06_D22_14	AG29	HP
14	IO_L22P_T3_A05_D21_14	AK28	HP
14	IO_L22N_T3_A04_D20_14	AK29	HP
14	IO_L23P_T3_A03_D19_14	AF30	HP
14	IO_L23N_T3_A02_D18_14	AG31	HP
14	IO_L24P_T3_A01_D17_14	AH28	HP
14	IO_L24N_T3_A00_D16_14	AJ28	HP
14	IO_25_VRP_14	AG32	HP
15	IO_0_VRN_15	AM38	HP
15	IO_L1P_T0_AD0P_15	AN38	HP
15	IO_L1N_T0_AD0N_15	AP38	HP
15	IO_L2P_T0_AD8P_15	AM41	HP
15	IO_L2N_T0_AD8N_15	AM42	HP
15	IO_L3P_T0_DQS_AD1P_15	AR38	HP
15	IO_L3N_T0_DQS_AD1N_15	AR39	HP

Bank	Pin name	Pin	I/O Type
15	IO_L4P_T0_15	AN40	HP
15	IO_L4N_T0_15	AN41	HP
15	IO_L5P_T0_AD9P_15	AR37	HP
15	IO_L5N_T0_AD9N_15	AT37	HP
15	IO_L6P_T0_15	AM39	HP
15	IO_L6N_T0_VREF_15	AN39	HP
15	IO_L7P_T1_AD2P_15	AP40	HP
15	IO_L7N_T1_AD2N_15	AR40	HP
15	IO_L8P_T1_AD10P_15	AP41	HP
15	IO_L8N_T1_AD10N_15	AP42	HP
15	IO_L9P_T1_DQS_AD3P_15	AT39	HP
15	IO_L9N_T1_DQS_AD3N_15	AT40	HP
15	IO_L10P_T1_AD11P_15	AR42	HP
15	IO_L10N_T1_AD11N_15	AT42	HP
15	IO_L11P_T1_SRCC_15	AU39	HP
15	IO_L11N_T1_SRCC_15	AV39	HP
15	IO_L12P_T1_MRCC_15	AU38	HP
15	IO_L12N_T1_MRCC_15	AV38	HP
15	IO_L13P_T2_MRCC_15	AV40	HP
15	IO_L13N_T2_MRCC_15	AW40	HP
15	IO_L14P_T2_SRCC_15	AY39	HP
15	IO_L14N_T2_SRCC_15	AY40	HP
15	IO_L15P_T2_DQS_15	AW37	HP
15	IO_L15N_T2_DQS_ADV_B_15	AY37	HP
15	IO_L16P_T2_A28_15	BA37	HP
15	IO_L16N_T2_A27_15	BB37	HP
15	IO_L17P_T2_A26_15	AW38	HP
15	IO_L17N_T2_A25_15	AY38	HP
15	IO_L18P_T2_A24_15	BB38	HP
15	IO_L18N_T2_A23_15	BB39	HP
15	IO_L19P_T3_A22_15	BA39	HP
15	IO_L19N_T3_A21_VREF_15	BA40	HP
15	IO_L20P_T3_A20_15	AT41	HP
15	IO_L20N_T3_A19_15	AU42	HP
15	IO_L21P_T3_DQS_15	AY42	HP
15	IO_L21N_T3_DQS_A18_15	BA42	HP
15	IO_L22P_T3_A17_15	AU41	HP
15	IO_L22N_T3_A16_15	AV41	HP
15	IO_L23P_T3_FOE_B_15	BA41	HP
15	IO_L23N_T3_FWE_B_15	BB41	HP

Bank	Pin name	Pin	I/O Type
15	IO_L24P_T3_RS1_15	AW41	HP
15	IO_L24N_T3_RS0_15	AW42	HP
15	IO_25_VRP_15	AU37	HP
16	IO_0_VRN_16	Y34	HP
16	IO_L1P_T0_16	AF35	HP
16	IO_L1N_T0_16	AF36	HP
16	IO_L2P_T0_16	AE37	HP
16	IO_L2N_T0_16	AF37	HP
16	IO_L3P_T0_DQS_16	AF34	HP
16	IO_L3N_T0_DQS_16	AG34	HP
16	IO_L4P_T0_16	AD36	HP
16	IO_L4N_T0_16	AD37	HP
16	IO_L5P_T0_16	AC35	HP
16	IO_L5N_T0_16	AC36	HP
16	IO_L6P_T0_16	AG36	HP
16	IO_L6N_T0_VREF_16	AH36	HP
16	IO_L7P_T1_16	Y37	HP
16	IO_L7N_T1_16	AA37	HP
16	IO_L8P_T1_16	Y35	HP
16	IO_L8N_T1_16	AA36	HP
16	IO_L9P_T1_DQS_16	AB36	HP
16	IO_L9N_T1_DQS_16	AB37	HP
16	IO_L10P_T1_16	AA34	HP
16	IO_L10N_T1_16	AA35	HP
16	IO_L11P_T1_SRCC_16	AB31	HP
16	IO_L11N_T1_SRCC_16	AB32	HP
16	IO_L12P_T1_MRCC_16	AB33	HP
16	IO_L12N_T1_MRCC_16	AC33	HP
16	IO_L13P_T2_MRCC_16	AD32	HP
16	IO_L13N_T2_MRCC_16	AD33	HP
16	IO_L14P_T2_SRCC_16	AC34	HP
16	IO_L14N_T2_SRCC_16	AD35	HP
16	IO_L15P_T2_DQS_16	AE32	HP
16	IO_L15N_T2_DQS_16	AE33	HP
16	IO_L16P_T2_16	AF31	HP
16	IO_L16N_T2_16	AF32	HP
16	IO_L17P_T2_16	AE34	HP
16	IO_L17N_T2_16	AE35	HP
16	IO_L18P_T2_16	AE29	HP
16	IO_L18N_T2_16	AE30	HP

Bank	Pin name	Pin	I/O Type
16	IO_L19P_T3_16	Y32	HP
16	IO_L19N_T3_VREF_16	Y33	HP
16	IO_L20P_T3_16	AC31	HP
16	IO_L20N_T3_16	AD31	HP
16	IO_L21P_T3_DQS_16	AA31	HP
16	IO_L21N_T3_DQS_16	AA32	HP
16	IO_L22P_T3_16	AC30	HP
16	IO_L22N_T3_16	AD30	HP
16	IO_L23P_T3_16	AA29	HP
16	IO_L23N_T3_16	AA30	HP
16	IO_L24P_T3_16	AB29	HP
16	IO_L24N_T3_16	AC29	HP
16	IO_25_VRP_16	AB34	HP
17	IO_0_VRN_17	Y38	HP
17	IO_L1P_T0_17	AB41	HP
17	IO_L1N_T0_17	AB42	HP
17	IO_L2P_T0_17	W40	HP
17	IO_L2N_T0_17	Y40	HP
17	IO_L3P_T0_DQS_17	Y39	HP
17	IO_L3N_T0_DQS_17	AA39	HP
17	IO_L4P_T0_17	Y42	HP
17	IO_L4N_T0_17	AA42	HP
17	IO_L5P_T0_17	AB38	HP
17	IO_L5N_T0_17	AB39	HP
17	IO_L6P_T0_17	AA40	HP
17	IO_L6N_T0_VREF_17	AA41	HP
17	IO_L7P_T1_17	AC38	HP
17	IO_L7N_T1_17	AC39	HP
17	IO_L8P_T1_17	AD42	HP
17	IO_L8N_T1_17	AE42	HP
17	IO_L9P_T1_DQS_17	AD38	HP
17	IO_L9N_T1_DQS_17	AE38	HP
17	IO_L10P_T1_17	AC40	HP
17	IO_L10N_T1_17	AC41	HP
17	IO_L11P_T1_SRCC_17	AE39	HP
17	IO_L11N_T1_SRCC_17	AE40	HP
17	IO_L12P_T1_MRCC_17	AD40	HP
17	IO_L12N_T1_MRCC_17	AD41	HP
17	IO_L13P_T2_MRCC_17	AF39	HP
17	IO_L13N_T2_MRCC_17	AF40	HP

Bank	Pin name	Pin	I/O Type
17	IO_L14P_T2_SRCC_17	AF41	HP
17	IO_L14N_T2_SRCC_17	AG41	HP
17	IO_L15P_T2_DQS_17	AG39	HP
17	IO_L15N_T2_DQS_17	AH39	HP
17	IO_L16P_T2_17	AF42	HP
17	IO_L16N_T2_17	AG42	HP
17	IO_L17P_T2_17	AG38	HP
17	IO_L17N_T2_17	AH38	HP
17	IO_L18P_T2_17	AJ38	HP
17	IO_L18N_T2_17	AK38	HP
17	IO_L19P_T3_17	AK40	HP
17	IO_L19N_T3_VREF_17	AL40	HP
17	IO_L20P_T3_17	AH40	HP
17	IO_L20N_T3_17	AH41	HP
17	IO_L21P_T3_DQS_17	AL41	HP
17	IO_L21N_T3_DQS_17	AL42	HP
17	IO_L22P_T3_17	AJ40	HP
17	IO_L22N_T3_17	AJ41	HP
17	IO_L23P_T3_17	AK39	HP
17	IO_L23N_T3_17	AL39	HP
17	IO_L24P_T3_17	AJ42	HP
17	IO_L24N_T3_17	AK42	HP
17	IO_25_VRP_17	AG37	HP
18	IO_0_VRN_18	N35	HP
18	IO_L1P_T0_18	T34	HP
18	IO_L1N_T0_18	R35	HP
18	IO_L2P_T0_18	N33	HP
18	IO_L2N_T0_18	N34	HP
18	IO_L3P_T0_DQS_18	R33	HP
18	IO_L3N_T0_DQS_18	R34	HP
18	IO_L4P_T0_18	P35	HP
18	IO_L4N_T0_18	P36	HP
18	IO_L5P_T0_18	T32	HP
18	IO_L5N_T0_18	R32	HP
18	IO_L6P_T0_18	P32	HP
18	IO_L6N_T0_VREF_18	P33	HP
18	IO_L7P_T1_18	T36	HP
18	IO_L7N_T1_18	R37	HP
18	IO_L8P_T1_18	P37	HP
18	IO_L8N_T1_18	P38	HP

Bank	Pin name	Pin	I/O Type
18	IO_L9P_T1_DQS_18	U34	HP
18	IO_L9N_T1_DQS_18	T35	HP
18	IO_L10P_T1_18	R38	HP
18	IO_L10N_T1_18	R39	HP
18	IO_L11P_T1_SRCC_18	U37	HP
18	IO_L11N_T1_SRCC_18	U38	HP
18	IO_L12P_T1_MRCC_18	U39	HP
18	IO_L12N_T1_MRCC_18	T39	HP
18	IO_L13P_T2_MRCC_18	U36	HP
18	IO_L13N_T2_MRCC_18	T37	HP
18	IO_L14P_T2_SRCC_18	V35	HP
18	IO_L14N_T2_SRCC_18	V36	HP
18	IO_L15P_T2_DQS_18	V33	HP
18	IO_L15N_T2_DQS_18	V34	HP
18	IO_L16P_T2_18	W36	HP
18	IO_L16N_T2_18	W37	HP
18	IO_L17P_T2_18	U32	HP
18	IO_L17N_T2_18	U33	HP
18	IO_L18P_T2_18	W32	HP
18	IO_L18N_T2_18	W33	HP
18	IO_L19P_T3_18	V39	HP
18	IO_L19N_T3_VREF_18	V40	HP
18	IO_L20P_T3_18	T40	HP
18	IO_L20N_T3_18	T41	HP
18	IO_L21P_T3_DQS_18	W41	HP
18	IO_L21N_T3_DQS_18	W42	HP
18	IO_L22P_T3_18	U41	HP
18	IO_L22N_T3_18	T42	HP
18	IO_L23P_T3_18	W38	HP
18	IO_L23N_T3_18	V38	HP
18	IO_L24P_T3_18	V41	HP
18	IO_L24N_T3_18	U42	HP
18	IO_25_VRP_18	W35	HP
19	IO_0_VRN_19	L36	HP
19	IO_L1P_T0_19	E40	HP
19	IO_L1N_T0_19	D40	HP
19	IO_L2P_T0_19	A40	HP
19	IO_L2N_T0_19	A41	HP
19	IO_L3P_T0_DQS_19	D41	HP
19	IO_L3N_T0_DQS_19	D42	HP

Bank	Pin name	Pin	I/O Type
19	IO_L4P_T0_19	B41	HP
19	IO_L4N_T0_19	B42	HP
19	IO_L5P_T0_19	F42	HP
19	IO_L5N_T0_19	E42	HP
19	IO_L6P_T0_19	C40	HP
19	IO_L6N_T0_VREF_19	C41	HP
19	IO_L7P_T1_19	H40	HP
19	IO_L7N_T1_19	H41	HP
19	IO_L8P_T1_19	H39	HP
19	IO_L8N_T1_19	G39	HP
19	IO_L9P_T1_DQS_19	G41	HP
19	IO_L9N_T1_DQS_19	G42	HP
19	IO_L10P_T1_19	F40	HP
19	IO_L10N_T1_19	F41	HP
19	IO_L11P_T1_SRCC_19	J40	HP
19	IO_L11N_T1_SRCC_19	J41	HP
19	IO_L12P_T1_MRCC_19	K39	HP
19	IO_L12N_T1_MRCC_19	K40	HP
19	IO_L13P_T2_MRCC_19	L39	HP
19	IO_L13N_T2_MRCC_19	L40	HP
19	IO_L14P_T2_SRCC_19	M41	HP
19	IO_L14N_T2_SRCC_19	L41	HP
19	IO_L15P_T2_DQS_19	K42	HP
19	IO_L15N_T2_DQS_19	J42	HP
19	IO_L16P_T2_19	M42	HP
19	IO_L16N_T2_19	L42	HP
19	IO_L17P_T2_19	K37	HP
19	IO_L17N_T2_19	K38	HP
19	IO_L18P_T2_19	M36	HP
19	IO_L18N_T2_19	L37	HP
19	IO_L19P_T3_19	P41	HP
19	IO_L19N_T3_VREF_19	N41	HP
19	IO_L20P_T3_19	M37	HP
19	IO_L20N_T3_19	M38	HP
19	IO_L21P_T3_DQS_19	R42	HP
19	IO_L21N_T3_DQS_19	P42	HP
19	IO_L22P_T3_19	N38	HP
19	IO_L22N_T3_19	M39	HP
19	IO_L23P_T3_19	R40	HP
19	IO_L23N_T3_19	P40	HP

Bank	Pin name	Pin	I/O Type
19	IO_L24P_T3_19	N39	HP
19	IO_L24N_T3_19	N40	HP
19	IO_25_VRP_19	N36	HP
31	IO_0_VRN_31	AM14	HP
31	IO_L1P_T0_31	AJ16	HP
31	IO_L1N_T0_31	AJ15	HP
31	IO_L2P_T0_31	AK14	HP
31	IO_L2N_T0_31	AK13	HP
31	IO_L3P_T0_DQS_31	AK15	HP
31	IO_L3N_T0_DQS_31	AL14	HP
31	IO_L4P_T0_31	AJ13	HP
31	IO_L4N_T0_31	AJ12	HP
31	IO_L5P_T0_31	AL16	HP
31	IO_L5N_T0_31	AL15	HP
31	IO_L6P_T0_31	AK12	HP
31	IO_L6N_T0_VREF_31	AL12	HP
31	IO_L7P_T1_31	AM13	HP
31	IO_L7N_T1_31	AN13	HP
31	IO_L8P_T1_31	AM12	HP
31	IO_L8N_T1_31	AM11	HP
31	IO_L9P_T1_DQS_31	AN15	HP
31	IO_L9N_T1_DQS_31	AN14	HP
31	IO_L10P_T1_31	AN11	HP
31	IO_L10N_T1_31	AP11	HP
31	IO_L11P_T1_SRCC_31	AR14	HP
31	IO_L11N_T1_SRCC_31	AT14	HP
31	IO_L12P_T1_MRCC_31	AP13	HP
31	IO_L12N_T1_MRCC_31	AR13	HP
31	IO_L13P_T2_MRCC_31	AU14	HP
31	IO_L13N_T2_MRCC_31	AU13	HP
31	IO_L14P_T2_SRCC_31	AV13	HP
31	IO_L14N_T2_SRCC_31	AW13	HP
31	IO_L15P_T2_DQS_31	AP12	HP
31	IO_L15N_T2_DQS_31	AR12	HP
31	IO_L16P_T2_31	AR15	HP
31	IO_L16N_T2_31	AT15	HP
31	IO_L17P_T2_31	AT12	HP
31	IO_L17N_T2_31	AU12	HP
31	IO_L18P_T2_31	AV15	HP
31	IO_L18N_T2_31	AV14	HP

Bank	Pin name	Pin	I/O Type
31	IO_L19P_T3_31	AW15	HP
31	IO_L19N_T3_VREF_31	AY15	HP
31	IO_L20P_T3_31	AW12	HP
31	IO_L20N_T3_31	AY12	HP
31	IO_L21P_T3_DQS_31	BA15	HP
31	IO_L21N_T3_DQS_31	BA14	HP
31	IO_L22P_T3_31	AY14	HP
31	IO_L22N_T3_31	AY13	HP
31	IO_L23P_T3_31	BB14	HP
31	IO_L23N_T3_31	BB13	HP
31	IO_L24P_T3_31	BA12	HP
31	IO_L24N_T3_31	BB12	HP
31	IO_25_VRP_31	AP15	HP
32	IO_0_VRN_32	AR20	HP
32	IO_L1P_T0_32	AL19	HP
32	IO_L1N_T0_32	AM19	HP
32	IO_L2P_T0_32	AK17	HP
32	IO_L2N_T0_32	AL17	HP
32	IO_L3P_T0_DQS_32	AM18	HP
32	IO_L3N_T0_DQS_32	AM17	HP
32	IO_L4P_T0_32	AK19	HP
32	IO_L4N_T0_32	AK18	HP
32	IO_L5P_T0_32	AM16	HP
32	IO_L5N_T0_32	AN16	HP
32	IO_L6P_T0_32	AJ18	HP
32	IO_L6N_T0_VREF_32	AJ17	HP
32	IO_L7P_T1_32	AP18	HP
32	IO_L7N_T1_32	AP17	HP
32	IO_L8P_T1_32	AP20	HP
32	IO_L8N_T1_32	AR19	HP
32	IO_L9P_T1_DQS_32	AN19	HP
32	IO_L9N_T1_DQS_32	AN18	HP
32	IO_L10P_T1_32	AR18	HP
32	IO_L10N_T1_32	AR17	HP
32	IO_L11P_T1_SRCC_32	AU18	HP
32	IO_L11N_T1_SRCC_32	AV18	HP
32	IO_L12P_T1_MRCC_32	AT17	HP
32	IO_L12N_T1_MRCC_32	AU17	HP
32	IO_L13P_T2_MRCC_32	AY18	HP
32	IO_L13N_T2_MRCC_32	AY17	HP

Bank	Pin name	Pin	I/O Type
32	IO_L14P_T2_SRCC_32	AW18	HP
32	IO_L14N_T2_SRCC_32	AW17	HP
32	IO_L15P_T2_DQS_32	AU19	HP
32	IO_L15N_T2_DQS_32	AV19	HP
32	IO_L16P_T2_32	AT20	HP
32	IO_L16N_T2_32	AT19	HP
32	IO_L17P_T2_32	AV16	HP
32	IO_L17N_T2_32	AW16	HP
32	IO_L18P_T2_32	AT16	HP
32	IO_L18N_T2_32	AU16	HP
32	IO_L19P_T3_32	BB19	HP
32	IO_L19N_T3_VREF_32	BB18	HP
32	IO_L20P_T3_32	AV20	HP
32	IO_L20N_T3_32	AW20	HP
32	IO_L21P_T3_DQS_32	BA17	HP
32	IO_L21N_T3_DQS_32	BB17	HP
32	IO_L22P_T3_32	AY20	HP
32	IO_L22N_T3_32	BA20	HP
32	IO_L23P_T3_32	BA16	HP
32	IO_L23N_T3_32	BB16	HP
32	IO_L24P_T3_32	AY19	HP
32	IO_L24N_T3_32	BA19	HP
32	IO_25_VRP_32	AP16	HP
33	IO_0_VRN_33	AL24	HP
33	IO_L1P_T0_33	AJ23	HP
33	IO_L1N_T0_33	AK23	HP
33	IO_L2P_T0_33	AK20	HP
33	IO_L2N_T0_33	AL20	HP
33	IO_L3P_T0_DQS_33	AJ22	HP
33	IO_L3N_T0_DQS_33	AK22	HP
33	IO_L4P_T0_33	AL21	HP
33	IO_L4N_T0_33	AM21	HP
33	IO_L5P_T0_33	AJ21	HP
33	IO_L5N_T0_33	AJ20	HP
33	IO_L6P_T0_33	AL22	HP
33	IO_L6N_T0_VREF_33	AM22	HP
33	IO_L7P_T1_33	AM24	HP
33	IO_L7N_T1_33	AN24	HP
33	IO_L8P_T1_33	AM23	HP
33	IO_L8N_T1_33	AN23	HP

Bank	Pin name	Pin	I/O Type
33	IO_L9P_T1_DQS_33	AP23	HP
33	IO_L9N_T1_DQS_33	AP22	HP
33	IO_L10P_T1_33	AN21	HP
33	IO_L10N_T1_33	AP21	HP
33	IO_L11P_T1_SRCC_33	AR23	HP
33	IO_L11N_T1_SRCC_33	AR22	HP
33	IO_L12P_T1_MRCC_33	AT22	HP
33	IO_L12N_T1_MRCC_33	AU22	HP
33	IO_L13P_T2_MRCC_33	AU23	HP
33	IO_L13N_T2_MRCC_33	AV23	HP
33	IO_L14P_T2_SRCC_33	AW23	HP
33	IO_L14N_T2_SRCC_33	AW22	HP
33	IO_L15P_T2_DQS_33	AT21	HP
33	IO_L15N_T2_DQS_33	AU21	HP
33	IO_L16P_T2_33	AR24	HP
33	IO_L16N_T2_33	AT24	HP
33	IO_L17P_T2_33	AV21	HP
33	IO_L17N_T2_33	AW21	HP
33	IO_L18P_T2_33	AU24	HP
33	IO_L18N_T2_33	AV24	HP
33	IO_L19P_T3_33	AY23	HP
33	IO_L19N_T3_VREF_33	AY22	HP
33	IO_L20P_T3_33	AY25	HP
33	IO_L20N_T3_33	BA25	HP
33	IO_L21P_T3_DQS_33	BA22	HP
33	IO_L21N_T3_DQS_33	BB22	HP
33	IO_L22P_T3_33	AY24	HP
33	IO_L22N_T3_33	BA24	HP
33	IO_L23P_T3_33	BA21	HP
33	IO_L23N_T3_33	BB21	HP
33	IO_L24P_T3_33	BB24	HP
33	IO_L24N_T3_33	BB23	HP
33	IO_25_VRP_33	AN20	HP
34	IO_0_VRN_34	R29	HP
34	IO_L1P_T0_34	K35	HP
34	IO_L1N_T0_34	J35	HP
34	IO_L2P_T0_34	J32	HP
34	IO_L2N_T0_34	J33	HP
34	IO_L3P_T0_DQS_34	K33	HP
34	IO_L3N_T0_DQS_34	K34	HP

Bank	Pin name	Pin	I/O Type
34	IO_L4P_T0_34	L34	HP
34	IO_L4N_T0_34	L35	HP
34	IO_L5P_T0_34	M33	HP
34	IO_L5N_T0_34	M34	HP
34	IO_L6P_T0_34	H34	HP
34	IO_L6N_T0_VREF_34	H35	HP
34	IO_L7P_T1_34	K29	HP
34	IO_L7N_T1_34	K30	HP
34	IO_L8P_T1_34	J30	HP
34	IO_L8N_T1_34	H30	HP
34	IO_L9P_T1_DQS_34	L29	HP
34	IO_L9N_T1_DQS_34	L30	HP
34	IO_L10P_T1_34	J31	HP
34	IO_L10N_T1_34	H31	HP
34	IO_L11P_T1_SRCC_34	M32	HP
34	IO_L11N_T1_SRCC_34	L32	HP
34	IO_L12P_T1_MRCC_34	L31	HP
34	IO_L12N_T1_MRCC_34	K32	HP
34	IO_L13P_T2_MRCC_34	N30	HP
34	IO_L13N_T2_MRCC_34	M31	HP
34	IO_L14P_T2_SRCC_34	P30	HP
34	IO_L14N_T2_SRCC_34	N31	HP
34	IO_L15P_T2_DQS_34	M28	HP
34	IO_L15N_T2_DQS_34	M29	HP
34	IO_L16P_T2_34	R28	HP
34	IO_L16N_T2_34	P28	HP
34	IO_L17P_T2_34	N28	HP
34	IO_L17N_T2_34	N29	HP
34	IO_L18P_T2_34	R30	HP
34	IO_L18N_T2_34	P31	HP
34	IO_L19P_T3_34	U31	HP
34	IO_L19N_T3_VREF_34	T31	HP
34	IO_L20P_T3_34	V30	HP
34	IO_L20N_T3_34	V31	HP
34	IO_L21P_T3_DQS_34	T29	HP
34	IO_L21N_T3_DQS_34	T30	HP
34	IO_L22P_T3_34	W30	HP
34	IO_L22N_T3_34	W31	HP
34	IO_L23P_T3_34	V29	HP
34	IO_L23N_T3_34	U29	HP

Bank	Pin name	Pin	I/O Type
34	IO_L24P_T3_34	Y29	HP
34	IO_L24N_T3_34	Y30	HP
34	IO_25_VRP_34	U28	HP
35	IO_0_VRN_35	G31	HP
35	IO_L1P_T0_AD4P_35	B36	HP
35	IO_L1N_T0_AD4N_35	A37	HP
35	IO_L2P_T0_AD12P_35	B34	HP
35	IO_L2N_T0_AD12N_35	A34	HP
35	IO_L3P_T0_DQS_AD5P_35	B39	HP
35	IO_L3N_T0_DQS_AD5N_35	A39	HP
35	IO_L4P_T0_35	A35	HP
35	IO_L4N_T0_35	A36	HP
35	IO_L5P_T0_AD13P_35	C38	HP
35	IO_L5N_T0_AD13N_35	C39	HP
35	IO_L6P_T0_35	B37	HP
35	IO_L6N_T0_VREF_35	B38	HP
35	IO_L7P_T1_AD6P_35	E32	HP
35	IO_L7N_T1_AD6N_35	D32	HP
35	IO_L8P_T1_AD14P_35	B32	HP
35	IO_L8N_T1_AD14N_35	B33	HP
35	IO_L9P_T1_DQS_AD7P_35	E33	HP
35	IO_L9N_T1_DQS_AD7N_35	D33	HP
35	IO_L10P_T1_AD15P_35	C33	HP
35	IO_L10N_T1_AD15N_35	C34	HP
35	IO_L11P_T1_SRCC_35	D35	HP
35	IO_L11N_T1_SRCC_35	D36	HP
35	IO_L12P_T1_MRCC_35	C35	HP
35	IO_L12N_T1_MRCC_35	C36	HP
35	IO_L13P_T2_MRCC_35	E34	HP
35	IO_L13N_T2_MRCC_35	E35	HP
35	IO_L14P_T2_SRCC_35	D37	HP
35	IO_L14N_T2_SRCC_35	D38	HP
35	IO_L15P_T2_DQS_35	G32	HP
35	IO_L15N_T2_DQS_35	F32	HP
35	IO_L16P_T2_35	F36	HP
35	IO_L16N_T2_35	F37	HP
35	IO_L17P_T2_35	F34	HP
35	IO_L17N_T2_35	F35	HP
35	IO_L18P_T2_35	H33	HP
35	IO_L18N_T2_35	G33	HP

Bank	Pin name	Pin	I/O Type
35	IO_L19P_T3_35	E37	HP
35	IO_L19N_T3_VREF_35	E38	HP
35	IO_L20P_T3_35	G36	HP
35	IO_L20N_T3_35	G37	HP
35	IO_L21P_T3_DQS_35	F39	HP
35	IO_L21N_T3_DQS_35	E39	HP
35	IO_L22P_T3_35	J37	HP
35	IO_L22N_T3_35	J38	HP
35	IO_L23P_T3_35	H38	HP
35	IO_L23N_T3_35	G38	HP
35	IO_L24P_T3_35	J36	HP
35	IO_L24N_T3_35	H36	HP
35	IO_25_VRP_35	G34	HP
36	IO_0_VRN_36	M23	HP
36	IO_L1P_T0_36	H24	HP
36	IO_L1N_T0_36	G24	HP
36	IO_L2P_T0_36	J21	HP
36	IO_L2N_T0_36	H21	HP
36	IO_L3P_T0_DQS_36	H25	HP
36	IO_L3N_T0_DQS_36	H26	HP
36	IO_L4P_T0_36	G21	HP
36	IO_L4N_T0_36	G22	HP
36	IO_L5P_T0_36	G26	HP
36	IO_L5N_T0_36	G27	HP
36	IO_L6P_T0_36	H23	HP
36	IO_L6N_T0_VREF_36	G23	HP
36	IO_L7P_T1_36	G28	HP
36	IO_L7N_T1_36	G29	HP
36	IO_L8P_T1_36	K28	HP
36	IO_L8N_T1_36	J28	HP
36	IO_L9P_T1_DQS_36	H28	HP
36	IO_L9N_T1_DQS_36	H29	HP
36	IO_L10P_T1_36	K27	HP
36	IO_L10N_T1_36	J27	HP
36	IO_L11P_T1_SRCC_36	K24	HP
36	IO_L11N_T1_SRCC_36	K25	HP
36	IO_L12P_T1_MRCC_36	J25	HP
36	IO_L12N_T1_MRCC_36	J26	HP
36	IO_L13P_T2_MRCC_36	M24	HP
36	IO_L13N_T2_MRCC_36	L24	HP

Bank	Pin name	Pin	I/O Type
36	IO_L14P_T2_SRCC_36	K23	HP
36	IO_L14N_T2_SRCC_36	J23	HP
36	IO_L15P_T2_DQS_36	M22	HP
36	IO_L15N_T2_DQS_36	L22	HP
36	IO_L16P_T2_36	L25	HP
36	IO_L16N_T2_36	L26	HP
36	IO_L17P_T2_36	K22	HP
36	IO_L17N_T2_36	J22	HP
36	IO_L18P_T2_36	M21	HP
36	IO_L18N_T2_36	L21	HP
36	IO_L19P_T3_36	P21	HP
36	IO_L19N_T3_VREF_36	N21	HP
36	IO_L20P_T3_36	P25	HP
36	IO_L20N_T3_36	P26	HP
36	IO_L21P_T3_DQS_36	P22	HP
36	IO_L21N_T3_DQS_36	P23	HP
36	IO_L22P_T3_36	N25	HP
36	IO_L22N_T3_36	N26	HP
36	IO_L23P_T3_36	N23	HP
36	IO_L23N_T3_36	N24	HP
36	IO_L24P_T3_36	M27	HP
36	IO_L24N_T3_36	L27	HP
36	IO_25_VRP_36	M26	HP
37	IO_0_VRN_37	F21	HP
37	IO_L1P_T0_37	A24	HP
37	IO_L1N_T0_37	A25	HP
37	IO_L2P_T0_37	B22	HP
37	IO_L2N_T0_37	A22	HP
37	IO_L3P_T0_DQS_37	A26	HP
37	IO_L3N_T0_DQS_37	A27	HP
37	IO_L4P_T0_37	C23	HP
37	IO_L4N_T0_37	B23	HP
37	IO_L5P_T0_37	B26	HP
37	IO_L5N_T0_37	B27	HP
37	IO_L6P_T0_37	C24	HP
37	IO_L6N_T0_VREF_37	B24	HP
37	IO_L7P_T1_37	E23	HP
37	IO_L7N_T1_37	E24	HP
37	IO_L8P_T1_37	F22	HP
37	IO_L8N_T1_37	E22	HP

Bank	Pin name	Pin	I/O Type
37	IO_L9P_T1_DQS_37	F25	HP
37	IO_L9N_T1_DQS_37	E25	HP
37	IO_L10P_T1_37	D22	HP
37	IO_L10N_T1_37	D23	HP
37	IO_L11P_T1_SRCC_37	D25	HP
37	IO_L11N_T1_SRCC_37	D26	HP
37	IO_L12P_T1_MRCC_37	C25	HP
37	IO_L12N_T1_MRCC_37	C26	HP
37	IO_L13P_T2_MRCC_37	D27	HP
37	IO_L13N_T2_MRCC_37	D28	HP
37	IO_L14P_T2_SRCC_37	C28	HP
37	IO_L14N_T2_SRCC_37	C29	HP
37	IO_L15P_T2_DQS_37	B28	HP
37	IO_L15N_T2_DQS_37	B29	HP
37	IO_L16P_T2_37	A31	HP
37	IO_L16N_T2_37	A32	HP
37	IO_L17P_T2_37	A29	HP
37	IO_L17N_T2_37	A30	HP
37	IO_L18P_T2_37	C31	HP
37	IO_L18N_T2_37	B31	HP
37	IO_L19P_T3_37	E30	HP
37	IO_L19N_T3_VREF_37	D31	HP
37	IO_L20P_T3_37	D30	HP
37	IO_L20N_T3_37	C30	HP
37	IO_L21P_T3_DQS_37	E27	HP
37	IO_L21N_T3_DQS_37	E28	HP
37	IO_L22P_T3_37	F29	HP
37	IO_L22N_T3_37	E29	HP
37	IO_L23P_T3_37	F26	HP
37	IO_L23N_T3_37	F27	HP
37	IO_L24P_T3_37	F30	HP
37	IO_L24N_T3_37	F31	HP
37	IO_25_VRP_37	F24	HP
38	IO_0_VRN_38	K18	HP
38	IO_L1P_T0_38	C19	HP
38	IO_L1N_T0_38	B19	HP
38	IO_L2P_T0_38	A16	HP
38	IO_L2N_T0_38	A15	HP
38	IO_L3P_T0_DQS_38	A20	HP
38	IO_L3N_T0_DQS_38	A19	HP

Bank	Pin name	Pin	I/O Type
38	IO_L4P_T0_38	B17	HP
38	IO_L4N_T0_38	A17	HP
38	IO_L5P_T0_38	B21	HP
38	IO_L5N_T0_38	A21	HP
38	IO_L6P_T0_38	C18	HP
38	IO_L6N_T0_VREF_38	B18	HP
38	IO_L7P_T1_38	D20	HP
38	IO_L7N_T1_38	C20	HP
38	IO_L8P_T1_38	F17	HP
38	IO_L8N_T1_38	E17	HP
38	IO_L9P_T1_DQS_38	D21	HP
38	IO_L9N_T1_DQS_38	C21	HP
38	IO_L10P_T1_38	D18	HP
38	IO_L10N_T1_38	D17	HP
38	IO_L11P_T1_SRCC_38	G19	HP
38	IO_L11N_T1_SRCC_38	F19	HP
38	IO_L12P_T1_MRCC_38	E19	HP
38	IO_L12N_T1_MRCC_38	E18	HP
38	IO_L13P_T2_MRCC_38	H19	HP
38	IO_L13N_T2_MRCC_38	G18	HP
38	IO_L14P_T2_SRCC_38	K19	HP
38	IO_L14N_T2_SRCC_38	J18	HP
38	IO_L15P_T2_DQS_38	F20	HP
38	IO_L15N_T2_DQS_38	E20	HP
38	IO_L16P_T2_38	K17	HP
38	IO_L16N_T2_38	J17	HP
38	IO_L17P_T2_38	J20	HP
38	IO_L17N_T2_38	H20	HP
38	IO_L18P_T2_38	H18	HP
38	IO_L18N_T2_38	G17	HP
38	IO_L19P_T3_38	P18	HP
38	IO_L19N_T3_VREF_38	P17	HP
38	IO_L20P_T3_38	M17	HP
38	IO_L20N_T3_38	L17	HP
38	IO_L21P_T3_DQS_38	N19	HP
38	IO_L21N_T3_DQS_38	N18	HP
38	IO_L22P_T3_38	M19	HP
38	IO_L22N_T3_38	M18	HP
38	IO_L23P_T3_38	P20	HP
38	IO_L23N_T3_38	N20	HP

Bank	Pin name	Pin	I/O Type
38	IO_L24P_T3_38	L20	HP
38	IO_L24N_T3_38	L19	HP
38	IO_25_VRP_38	K20	HP
39	IO_0_VRN_39	J16	HP
39	IO_L1P_T0_39	C16	HP
39	IO_L1N_T0_39	B16	HP
39	IO_L2P_T0_39	B14	HP
39	IO_L2N_T0_39	A14	HP
39	IO_L3P_T0_DQS_39	C15	HP
39	IO_L3N_T0_DQS_39	C14	HP
39	IO_L4P_T0_39	D13	HP
39	IO_L4N_T0_39	C13	HP
39	IO_L5P_T0_39	D16	HP
39	IO_L5N_T0_39	D15	HP
39	IO_L6P_T0_39	E12	HP
39	IO_L6N_T0_VREF_39	D12	HP
39	IO_L7P_T1_39	F16	HP
39	IO_L7N_T1_39	E15	HP
39	IO_L8P_T1_39	E14	HP
39	IO_L8N_T1_39	E13	HP
39	IO_L9P_T1_DQS_39	H16	HP
39	IO_L9N_T1_DQS_39	G16	HP
39	IO_L10P_T1_39	G12	HP
39	IO_L10N_T1_39	F12	HP
39	IO_L11P_T1_SRCC_39	F15	HP
39	IO_L11N_T1_SRCC_39	F14	HP
39	IO_L12P_T1_MRCC_39	G14	HP
39	IO_L12N_T1_MRCC_39	G13	HP
39	IO_L13P_T2_MRCC_39	H15	HP
39	IO_L13N_T2_MRCC_39	H14	HP
39	IO_L14P_T2_SRCC_39	J13	HP
39	IO_L14N_T2_SRCC_39	H13	HP
39	IO_L15P_T2_DQS_39	K12	HP
39	IO_L15N_T2_DQS_39	J12	HP
39	IO_L16P_T2_39	K15	HP
39	IO_L16N_T2_39	J15	HP
39	IO_L17P_T2_39	K14	HP
39	IO_L17N_T2_39	K13	HP
39	IO_L18P_T2_39	L16	HP
39	IO_L18N_T2_39	L15	HP

Bank	Pin name	Pin	I/O Type
39	IO_L19P_T3_39	L12	HP
39	IO_L19N_T3_VREF_39	L11	HP
39	IO_L20P_T3_39	M14	HP
39	IO_L20N_T3_39	L14	HP
39	IO_L21P_T3_DQS_39	N16	HP
39	IO_L21N_T3_DQS_39	M16	HP
39	IO_L22P_T3_39	N13	HP
39	IO_L22N_T3_39	M13	HP
39	IO_L23P_T3_39	N15	HP
39	IO_L23N_T3_39	N14	HP
39	IO_L24P_T3_39	M12	HP
39	IO_L24N_T3_39	M11	HP
39	IO_25_VRP_39	J11	HP
111	MGTHTXP3_111	AW2	GTH
111	MGTHRXP3_111	AW6	GTH
111	MGTHTXN3_111	AW1	GTH
111	MGTHRXN3_111	AW5	GTH
111	MGTHTXP2_111	AY4	GTH
111	MGTHRXP2_111	AY8	GTH
111	MGTHTXN2_111	AY3	GTH
111	MGTREFCLK0P_111	AW10	GTH
111	MGTHRXN2_111	AY7	GTH
111	MGTREFCLK0N_111	AW9	GTH
111	MGTREFCLK1N_111	BA9	GTH
111	MGTREFCLK1P_111	BA10	GTH
111	MGTHTXP1_111	BA2	GTH
111	MGTHRXP1_111	BA6	GTH
111	MGTHTXN1_111	BA1	GTH
111	MGTHRXN1_111	BA5	GTH
111	MGTHTXP0_111	BB4	GTH
111	MGTHRXP0_111	BB8	GTH
111	MGTHTXN0_111	BB3	GTH
111	MGTHRXN0_111	BB7	GTH
112	MGTHTXP3_112	AR2	GTH
112	MGTHRXP3_112	AP8	GTH
112	MGTHTXN3_112	AR1	GTH
112	MGTHRXN3_112	AP7	GTH
112	MGTHTXP2_112	AT4	GTH
112	MGTHRXP2_112	AR6	GTH
112	MGTHTXN2_112	AT3	GTH

Bank	Pin name	Pin	I/O Type
112	MGTREFCLK0P_112	AT8	GTH
112	MGTHRXN2_112	AR5	GTH
112	MGTREFCLK0N_112	AT7	GTH
112	MGTREFCLK1N_112	AU9	GTH
112	MGTREFCLK1P_112	AU10	GTH
112	MGTHTXP1_112	AU2	GTH
112	MGTHRXP1_112	AU6	GTH
112	MGTHTXN1_112	AU1	GTH
112	MGTHRXN1_112	AU5	GTH
112	MGTHTXP0_112	AV4	GTH
112	MGTHRXP0_112	AV8	GTH
112	MGTHTXN0_112	AV3	GTH
112	MGTHRXN0_112	AV7	GTH
113	MGTHTXP3_113	AL2	GTH
113	MGTHRXP3_113	AJ6	GTH
113	MGTHTXN3_113	AL1	GTH
113	MGTHRXN3_113	AJ5	GTH
113	MGTHTXP2_113	AM4	GTH
113	MGTHRXP2_113	AL6	GTH
113	MGTHTXN2_113	AM3	GTH
113	MGTREFCLK0P_113	AH8	GTH
113	MGTHRXN2_113	AL5	GTH
113	MGTREFCLK0N_113	AH7	GTH
113	MGTREFCLK1N_113	AK7	GTH
113	MGTREFCLK1P_113	AK8	GTH
113	MGTHTXP1_113	AN2	GTH
113	MGTHRXP1_113	AM8	GTH
113	MGTHTXN1_113	AN1	GTH
113	MGTHRXN1_113	AM7	GTH
113	MGTHTXP0_113	AP4	GTH
113	MGTHRXP0_113	AN6	GTH
113	MGTHTXN0_113	AP3	GTH
113	MGTHRXN0_113	AN5	GTH
114	MGTHTXP3_114	AG2	GTH
114	MGTHRXP3_114	AD4	GTH
114	MGTHTXN3_114	AG1	GTH
114	MGTHRXN3_114	AD3	GTH
114	MGTHTXP2_114	AH4	GTH
114	MGTHRXP2_114	AE6	GTH
114	MGTHTXN2_114	AH3	GTH

Bank	Pin name	Pin	I/O Type
114	MGTREFCLK0P_114	AD8	GTH
114	MGTHRXN2_114	AE5	GTH
114	MGTREFCLK0N_114	AD7	GTH
114	MGTREFCLK1N_114	AF7	GTH
114	MGTREFCLK1P_114	AF8	GTH
114	MGTHTXP1_114	AJ2	GTH
114	MGTHRXP1_114	AF4	GTH
114	MGTHTXN1_114	AJ1	GTH
114	MGTHRXN1_114	AF3	GTH
114	MGTHTXP0_114	AK4	GTH
114	MGTHRXP0_114	AG6	GTH
114	MGTHTXN0_114	AK3	GTH
114	MGTHRXN0_114	AG5	GTH
115	MGTHTXP3_115	W2	GTH
115	MGTHRXP3_115	Y4	GTH
115	MGTHTXN3_115	W1	GTH
115	MGTHRXN3_115	Y3	GTH
115	MGTHTXP2_115	AA2	GTH
115	MGTHRXP2_115	AA6	GTH
115	MGTHTXN2_115	AA1	GTH
115	MGTREFCLK0P_115	Y8	GTH
115	MGTHRXN2_115	AA5	GTH
115	MGTAVTTRCAL_115	A12	GTH
115	MGTREFCLK0N_115	Y7	GTH
115	MGTRREF_115	B11	GTH
115	MGTREFCLK1N_115	AB7	GTH
115	MGTREFCLK1P_115	AB8	GTH
115	MGTHTXP1_115	AC2	GTH
115	MGTHRXP1_115	AB4	GTH
115	MGTHTXN1_115	AC1	GTH
115	MGTHRXN1_115	AB3	GTH
115	MGTHTXP0_115	AE2	GTH
115	MGTHRXP0_115	AC6	GTH
115	MGTHTXN0_115	AE1	GTH
115	MGTHRXN0_115	AC5	GTH
116	MGTHTXP3_116	P4	GTH
116	MGTHRXP3_116	R6	GTH
116	MGTHTXN3_116	P3	GTH
116	MGTHRXN3_116	R5	GTH
116	MGTHTXP2_116	R2	GTH

Bank	Pin name	Pin	I/O Type
116	MGTHRXP2_116	U6	GTH
116	MGTHTXN2_116	R1	GTH
116	MGTREFCLK0P_116	T8	GTH
116	MGTHRXN2_116	U5	GTH
116	MGTREFCLK0N_116	T7	GTH
116	MGTREFCLK1N_116	V7	GTH
116	MGTREFCLK1P_116	V8	GTH
116	MGTHTXP1_116	T4	GTH
116	MGTHRXP1_116	V4	GTH
116	MGTHTXN1_116	T3	GTH
116	MGTHRXN1_116	V3	GTH
116	MGTHTXP0_116	U2	GTH
116	MGTHRXP0_116	W6	GTH
116	MGTHTXN0_116	U1	GTH
116	MGTHRXN0_116	W5	GTH
117	MGTHTXP3_117	K4	GTH
117	MGTHRXP3_117	J6	GTH
117	MGTHTXN3_117	K3	GTH
117	MGTHRXN3_117	J5	GTH
117	MGTHTXP2_117	L2	GTH
117	MGTHRXP2_117	L6	GTH
117	MGTHTXN2_117	L1	GTH
117	MGTREFCLK0P_117	K8	GTH
117	MGTHRXN2_117	L5	GTH
117	MGTREFCLK0N_117	K7	GTH
117	MGTREFCLK1N_117	M7	GTH
117	MGTREFCLK1P_117	M8	GTH
117	MGTHTXP1_117	M4	GTH
117	MGTHRXP1_117	N6	GTH
117	MGTHTXN1_117	M3	GTH
117	MGTHRXN1_117	N5	GTH
117	MGTHTXP0_117	N2	GTH
117	MGTHRXP0_117	P8	GTH
117	MGTHTXN0_117	N1	GTH
117	MGTHRXN0_117	P7	GTH
118	MGTHTXP3_118	F4	GTH
118	MGTHRXP3_118	E6	GTH
118	MGTHTXN3_118	F3	GTH
118	MGTHRXN3_118	E5	GTH
118	MGTHTXP2_118	G2	GTH

Bank	Pin name	Pin	I/O Type
118	MGTHRXP2_118	F8	GTH
118	MGTHTXN2_118	G1	GTH
118	MGTREFCLK0P_118	E10	GTH
118	MGTHRXN2_118	F7	GTH
118	MGTREFCLK0N_118	E9	GTH
118	MGTREFCLK1N_118	G9	GTH
118	MGTREFCLK1P_118	G10	GTH
118	MGTHTXP1_118	H4	GTH
118	MGTHRXP1_118	G6	GTH
118	MGTHTXN1_118	H3	GTH
118	MGTHRXN1_118	G5	GTH
118	MGTHTXP0_118	J2	GTH
118	MGTHRXP0_118	H8	GTH
118	MGTHTXN0_118	J1	GTH
118	MGTHRXN0_118	H7	GTH
119	MGTHTXP3_119	B4	GTH
119	MGTHRXP3_119	A6	GTH
119	MGTHTXN3_119	B3	GTH
119	MGTHRXN3_119	A5	GTH
119	MGTHTXP2_119	C2	GTH
119	MGTHRXP2_119	B8	GTH
119	MGTHTXN2_119	C1	GTH
119	MGTREFCLK0P_119	A10	GTH
119	MGTHRXN2_119	B7	GTH
119	MGTREFCLK0N_119	A9	GTH
119	MGTREFCLK1N_119	C9	GTH
119	MGTREFCLK1P_119	C10	GTH
119	MGTHTXP1_119	D4	GTH
119	MGTHRXP1_119	C6	GTH
119	MGTHTXN1_119	D3	GTH
119	MGTHRXN1_119	C5	GTH
119	MGTHTXP0_119	E2	GTH
119	MGTHRXP0_119	D8	GTH
119	MGTHTXN0_119	E1	GTH
119	MGTHRXN0_119	D7	GTH
NA	MGTAVCC_G11	C8	NA
NA	MGTAVCC_G11	E8	NA
NA	MGTAVCC_G11	G8	NA
NA	MGTAVCC_G11	J8	NA
NA	MGTAVCC_G11	L8	NA

Bank	Pin name	Pin	I/O Type
NA	MGTAVCC_G10	AA8	NA
NA	MGTAVCC_G10	AC8	NA
NA	MGTAVCC_G10	AE8	NA
NA	MGTAVCC_G10	AJ8	NA
NA	MGTAVCC_G10	AL8	NA
NA	MGTAVCC_G10	AN8	NA
NA	MGTAVCC_G10	AR8	NA
NA	MGTAVCC_G10	AU8	NA
NA	MGTAVCC_G10	AW8	NA
NA	MGTAVCC_G10	BA8	NA
NA	MGTAVCC_G10	W8	NA
NA	MGTAVTT_G11	B6	NA
NA	MGTAVTT_G11	C4	NA
NA	MGTAVTT_G11	D6	NA
NA	MGTAVTT_G11	E4	NA
NA	MGTAVTT_G11	F6	NA
NA	MGTAVTT_G11	G4	NA
NA	MGTAVTT_G11	H6	NA
NA	MGTAVTT_G11	J4	NA
NA	MGTAVTT_G11	L4	NA
NA	MGTAVTT_G11	N4	NA
NA	MGTAVTT_G11	P6	NA
NA	MGTAVTT_G10	R4	NA
NA	MGTAVTT_G10	W4	NA
NA	MGTAVTT_G10	AA4	NA
NA	MGTAVTT_G10	AC4	NA
NA	MGTAVTT_G10	AE4	NA
NA	MGTAVTT_G10	AJ4	NA
NA	MGTAVTT_G10	AL4	NA
NA	MGTAVTT_G10	AM6	NA
NA	MGTAVTT_G10	AN4	NA
NA	MGTAVTT_G10	AP6	NA
NA	MGTAVTT_G10	AR4	NA
NA	MGTAVTT_G10	AU4	NA
NA	MGTAVTT_G10	AV6	NA
NA	MGTAVTT_G10	AW4	NA
NA	MGTAVTT_G10	AY6	NA
NA	MGTAVTT_G10	BA4	NA
NA	MGTVCCAUX_G11	N8	NA
NA	MGTVCCAUX_G10	R8	NA

Bank	Pin name	Pin	I/O Type
NA	MGTVCCAUX_G10	U8	NA
NA	GND	A2	NA
NA	GND	A3	NA
NA	GND	A4	NA
NA	GND	A7	NA
NA	GND	A8	NA
NA	GND	A11	NA
NA	GND	A13	NA
NA	GND	A18	NA
NA	GND	A28	NA
NA	GND	A38	NA
NA	GND	AA3	NA
NA	GND	AA7	NA
NA	GND	AA9	NA
NA	GND	AA11	NA
NA	GND	AA13	NA
NA	GND	AA15	NA
NA	GND	AA17	NA
NA	GND	AA19	NA
NA	GND	AA23	NA
NA	GND	AA25	NA
NA	GND	AA27	NA
NA	GND	AA38	NA
NA	GND	AB1	NA
NA	GND	AB2	NA
NA	GND	AB5	NA
NA	GND	AB6	NA
NA	GND	AB9	NA
NA	GND	AB10	NA
NA	GND	AB12	NA
NA	GND	AB14	NA
NA	GND	AB16	NA
NA	GND	AB18	NA
NA	GND	AB22	NA
NA	GND	AB24	NA
NA	GND	AB26	NA
NA	GND	AB28	NA
NA	GND	AB35	NA
NA	GND	AC3	NA
NA	GND	AC7	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AC11	NA
NA	GND	AC13	NA
NA	GND	AC15	NA
NA	GND	AC17	NA
NA	GND	AC19	NA
NA	GND	AC23	NA
NA	GND	AC25	NA
NA	GND	AC27	NA
NA	GND	AC32	NA
NA	GND	AC42	NA
NA	GND	AD1	NA
NA	GND	AD2	NA
NA	GND	AD5	NA
NA	GND	AD6	NA
NA	GND	AD9	NA
NA	GND	AD10	NA
NA	GND	AD12	NA
NA	GND	AD14	NA
NA	GND	AD16	NA
NA	GND	AD18	NA
NA	GND	AD20	NA
NA	GND	AD22	NA
NA	GND	AD24	NA
NA	GND	AD26	NA
NA	GND	AD28	NA
NA	GND	AD29	NA
NA	GND	AD39	NA
NA	GND	AE3	NA
NA	GND	AE7	NA
NA	GND	AE9	NA
NA	GND	AE11	NA
NA	GND	AE13	NA
NA	GND	AE15	NA
NA	GND	AE17	NA
NA	GND	AE19	NA
NA	GND	AE21	NA
NA	GND	AE23	NA
NA	GND	AE25	NA
NA	GND	AE27	NA
NA	GND	AE36	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AF1	NA
NA	GND	AF2	NA
NA	GND	AF5	NA
NA	GND	AF6	NA
NA	GND	AF9	NA
NA	GND	AF10	NA
NA	GND	AF12	NA
NA	GND	AF14	NA
NA	GND	AF16	NA
NA	GND	AF18	NA
NA	GND	AF20	NA
NA	GND	AF22	NA
NA	GND	AF24	NA
NA	GND	AF26	NA
NA	GND	AF33	NA
NA	GND	AG3	NA
NA	GND	AG4	NA
NA	GND	AG7	NA
NA	GND	AG8	NA
NA	GND	AG9	NA
NA	GND	AG10	NA
NA	GND	AG13	NA
NA	GND	AG15	NA
NA	GND	AG17	NA
NA	GND	AG19	NA
NA	GND	AG21	NA
NA	GND	AG23	NA
NA	GND	AG25	NA
NA	GND	AG27	NA
NA	GND	AG30	NA
NA	GND	AG40	NA
NA	GND	AH1	NA
NA	GND	AH2	NA
NA	GND	AH5	NA
NA	GND	AH6	NA
NA	GND	AH9	NA
NA	GND	AH12	NA
NA	GND	AH14	NA
NA	GND	AH16	NA
NA	GND	AH17	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AH18	NA
NA	GND	AH20	NA
NA	GND	AH22	NA
NA	GND	AH24	NA
NA	GND	AH26	NA
NA	GND	AH37	NA
NA	GND	AJ3	NA
NA	GND	AJ7	NA
NA	GND	AJ9	NA
NA	GND	AJ14	NA
NA	GND	AJ24	NA
NA	GND	AJ27	NA
NA	GND	AJ34	NA
NA	GND	AK1	NA
NA	GND	AK2	NA
NA	GND	AK5	NA
NA	GND	AK6	NA
NA	GND	AK9	NA
NA	GND	AK11	NA
NA	GND	AK21	NA
NA	GND	AK31	NA
NA	GND	AK41	NA
NA	GND	AL3	NA
NA	GND	AL7	NA
NA	GND	AL9	NA
NA	GND	AL18	NA
NA	GND	AL28	NA
NA	GND	AL38	NA
NA	GND	AM1	NA
NA	GND	AM2	NA
NA	GND	AM5	NA
NA	GND	AM9	NA
NA	GND	AM10	NA
NA	GND	AM15	NA
NA	GND	AM25	NA
NA	GND	AM35	NA
NA	GND	AN3	NA
NA	GND	AN7	NA
NA	GND	AN9	NA
NA	GND	AN10	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AN12	NA
NA	GND	AN22	NA
NA	GND	AN32	NA
NA	GND	AN42	NA
NA	GND	AP1	NA
NA	GND	AP2	NA
NA	GND	AP5	NA
NA	GND	AP9	NA
NA	GND	AP10	NA
NA	GND	AP19	NA
NA	GND	AP29	NA
NA	GND	AP39	NA
NA	GND	AR3	NA
NA	GND	AR7	NA
NA	GND	AR9	NA
NA	GND	AR10	NA
NA	GND	AR16	NA
NA	GND	AR26	NA
NA	GND	AR36	NA
NA	GND	AT1	NA
NA	GND	AT2	NA
NA	GND	AT5	NA
NA	GND	AT6	NA
NA	GND	AT9	NA
NA	GND	AT10	NA
NA	GND	AT11	NA
NA	GND	AT13	NA
NA	GND	AT23	NA
NA	GND	AT33	NA
NA	GND	AU3	NA
NA	GND	AU7	NA
NA	GND	AU11	NA
NA	GND	AU20	NA
NA	GND	AU30	NA
NA	GND	AU40	NA
NA	GND	AV1	NA
NA	GND	AV2	NA
NA	GND	AV5	NA
NA	GND	AV9	NA
NA	GND	AV10	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AV11	NA
NA	GND	AV17	NA
NA	GND	AV27	NA
NA	GND	AV37	NA
NA	GND	AW3	NA
NA	GND	AW7	NA
NA	GND	AW11	NA
NA	GND	AW14	NA
NA	GND	AW24	NA
NA	GND	AW34	NA
NA	GND	AY1	NA
NA	GND	AY2	NA
NA	GND	AY5	NA
NA	GND	AY9	NA
NA	GND	AY10	NA
NA	GND	AY11	NA
NA	GND	AY21	NA
NA	GND	AY31	NA
NA	GND	AY41	NA
NA	GND	B1	NA
NA	GND	B2	NA
NA	GND	B5	NA
NA	GND	B9	NA
NA	GND	B10	NA
NA	GND	B12	NA
NA	GND	B13	NA
NA	GND	B15	NA
NA	GND	B25	NA
NA	GND	B35	NA
NA	GND	BA3	NA
NA	GND	BA7	NA
NA	GND	BA11	NA
NA	GND	BA18	NA
NA	GND	BA28	NA
NA	GND	BA38	NA
NA	GND	BB2	NA
NA	GND	BB5	NA
NA	GND	BB6	NA
NA	GND	BB9	NA
NA	GND	BB10	NA

Bank	Pin name	Pin	I/O Type
NA	GND	BB11	NA
NA	GND	BB15	NA
NA	GND	BB25	NA
NA	GND	BB35	NA
NA	GND	C3	NA
NA	GND	C7	NA
NA	GND	C11	NA
NA	GND	C12	NA
NA	GND	C22	NA
NA	GND	C32	NA
NA	GND	C42	NA
NA	GND	D1	NA
NA	GND	D2	NA
NA	GND	D5	NA
NA	GND	D9	NA
NA	GND	D10	NA
NA	GND	D11	NA
NA	GND	D19	NA
NA	GND	D29	NA
NA	GND	D39	NA
NA	GND	E3	NA
NA	GND	E7	NA
NA	GND	E11	NA
NA	GND	E16	NA
NA	GND	E26	NA
NA	GND	E36	NA
NA	GND	F1	NA
NA	GND	F2	NA
NA	GND	F5	NA
NA	GND	F9	NA
NA	GND	F10	NA
NA	GND	F11	NA
NA	GND	F13	NA
NA	GND	F23	NA
NA	GND	F33	NA
NA	GND	G3	NA
NA	GND	G7	NA
NA	GND	G11	NA
NA	GND	G20	NA
NA	GND	G30	NA

Bank	Pin name	Pin	I/O Type
NA	GND	G40	NA
NA	GND	H1	NA
NA	GND	H2	NA
NA	GND	H5	NA
NA	GND	H9	NA
NA	GND	H10	NA
NA	GND	H11	NA
NA	GND	H17	NA
NA	GND	H27	NA
NA	GND	H37	NA
NA	GND	J3	NA
NA	GND	J7	NA
NA	GND	J9	NA
NA	GND	J10	NA
NA	GND	J14	NA
NA	GND	J24	NA
NA	GND	J34	NA
NA	GND	K1	NA
NA	GND	K2	NA
NA	GND	K5	NA
NA	GND	K6	NA
NA	GND	K9	NA
NA	GND	K10	NA
NA	GND	K11	NA
NA	GND	K21	NA
NA	GND	K31	NA
NA	GND	K41	NA
NA	GND	L3	NA
NA	GND	L7	NA
NA	GND	L9	NA
NA	GND	L10	NA
NA	GND	L18	NA
NA	GND	L28	NA
NA	GND	L38	NA
NA	GND	M1	NA
NA	GND	M2	NA
NA	GND	M5	NA
NA	GND	M6	NA
NA	GND	M9	NA
NA	GND	M15	NA

Bank	Pin name	Pin	I/O Type
NA	GND	M25	NA
NA	GND	M35	NA
NA	GND	N3	NA
NA	GND	N7	NA
NA	GND	N9	NA
NA	GND	N12	NA
NA	GND	N22	NA
NA	GND	N32	NA
NA	GND	N42	NA
NA	GND	P1	NA
NA	GND	P2	NA
NA	GND	P5	NA
NA	GND	P9	NA
NA	GND	P12	NA
NA	GND	P16	NA
NA	GND	P19	NA
NA	GND	P29	NA
NA	GND	P39	NA
NA	GND	R3	NA
NA	GND	R7	NA
NA	GND	R9	NA
NA	GND	R11	NA
NA	GND	R13	NA
NA	GND	R15	NA
NA	GND	R17	NA
NA	GND	R19	NA
NA	GND	R21	NA
NA	GND	R23	NA
NA	GND	R25	NA
NA	GND	R27	NA
NA	GND	R36	NA
NA	GND	T1	NA
NA	GND	T2	NA
NA	GND	T5	NA
NA	GND	T6	NA
NA	GND	T9	NA
NA	GND	T12	NA
NA	GND	T14	NA
NA	GND	T16	NA
NA	GND	T18	NA

Bank	Pin name	Pin	I/O Type
NA	GND	T20	NA
NA	GND	T22	NA
NA	GND	T24	NA
NA	GND	T26	NA
NA	GND	T33	NA
NA	GND	U3	NA
NA	GND	U4	NA
NA	GND	U7	NA
NA	GND	U9	NA
NA	GND	U10	NA
NA	GND	U11	NA
NA	GND	U13	NA
NA	GND	U15	NA
NA	GND	U17	NA
NA	GND	U19	NA
NA	GND	U21	NA
NA	GND	U23	NA
NA	GND	U25	NA
NA	GND	U27	NA
NA	GND	U30	NA
NA	GND	U40	NA
NA	GND	V1	NA
NA	GND	V2	NA
NA	GND	V5	NA
NA	GND	V6	NA
NA	GND	V9	NA
NA	GND	V10	NA
NA	GND	V12	NA
NA	GND	V14	NA
NA	GND	V16	NA
NA	GND	V18	NA
NA	GND	V20	NA
NA	GND	V22	NA
NA	GND	V24	NA
NA	GND	V26	NA
NA	GND	V28	NA
NA	GND	V37	NA
NA	GND	W3	NA
NA	GND	W7	NA
NA	GND	W11	NA

Bank	Pin name	Pin	I/O Type
NA	GND	W13	NA
NA	GND	W15	NA
NA	GND	W17	NA
NA	GND	W19	NA
NA	GND	W21	NA
NA	GND	W23	NA
NA	GND	W25	NA
NA	GND	W27	NA
NA	GND	W34	NA
NA	GND	Y1	NA
NA	GND	Y2	NA
NA	GND	Y5	NA
NA	GND	Y6	NA
NA	GND	Y9	NA
NA	GND	Y10	NA
NA	GND	Y12	NA
NA	GND	Y14	NA
NA	GND	Y16	NA
NA	GND	Y18	NA
NA	GND	Y22	NA
NA	GND	Y24	NA
NA	GND	Y26	NA
NA	GND	Y28	NA
NA	GND	Y31	NA
NA	GND	Y41	NA
NA	VCCINT	AA10	NA
NA	VCCINT	AA12	NA
NA	VCCINT	AA14	NA
NA	VCCINT	AA16	NA
NA	VCCINT	AA24	NA
NA	VCCINT	AA28	NA
NA	VCCINT	AB11	NA
NA	VCCINT	AB13	NA
NA	VCCINT	AB15	NA
NA	VCCINT	AB19	NA
NA	VCCINT	AB23	NA
NA	VCCINT	AB27	NA
NA	VCCINT	AC12	NA
NA	VCCINT	AC14	NA
NA	VCCINT	AC16	NA

Bank	Pin name	Pin	I/O Type
NA	VCCINT	AC24	NA
NA	VCCINT	AC28	NA
NA	VCCINT	AD11	NA
NA	VCCINT	AD13	NA
NA	VCCINT	AD15	NA
NA	VCCINT	AD19	NA
NA	VCCINT	AD21	NA
NA	VCCINT	AD23	NA
NA	VCCINT	AD27	NA
NA	VCCINT	AE10	NA
NA	VCCINT	AE12	NA
NA	VCCINT	AE14	NA
NA	VCCINT	AE16	NA
NA	VCCINT	AE20	NA
NA	VCCINT	AE24	NA
NA	VCCINT	AE28	NA
NA	VCCINT	AF11	NA
NA	VCCINT	AF13	NA
NA	VCCINT	AF15	NA
NA	VCCINT	AF21	NA
NA	VCCINT	AF23	NA
NA	VCCINT	AF27	NA
NA	VCCINT	AG12	NA
NA	VCCINT	AG14	NA
NA	VCCINT	AG16	NA
NA	VCCINT	AG20	NA
NA	VCCINT	AG24	NA
NA	VCCINT	AG28	NA
NA	VCCINT	AH11	NA
NA	VCCINT	AH13	NA
NA	VCCINT	AH15	NA
NA	VCCINT	AH19	NA
NA	VCCINT	AH23	NA
NA	VCCINT	AH27	NA
NA	VCCINT	P13	NA
NA	VCCINT	P15	NA
NA	VCCINT	P27	NA
NA	VCCINT	R12	NA
NA	VCCINT	R14	NA
NA	VCCINT	R16	NA

Bank	Pin name	Pin	I/O Type
NA	VCCINT	R20	NA
NA	VCCINT	R24	NA
NA	VCCINT	T13	NA
NA	VCCINT	T15	NA
NA	VCCINT	T21	NA
NA	VCCINT	T23	NA
NA	VCCINT	T27	NA
NA	VCCINT	U12	NA
NA	VCCINT	U14	NA
NA	VCCINT	U16	NA
NA	VCCINT	U20	NA
NA	VCCINT	U24	NA
NA	VCCINT	V11	NA
NA	VCCINT	V13	NA
NA	VCCINT	V15	NA
NA	VCCINT	V19	NA
NA	VCCINT	V21	NA
NA	VCCINT	V23	NA
NA	VCCINT	V27	NA
NA	VCCINT	W12	NA
NA	VCCINT	W14	NA
NA	VCCINT	W16	NA
NA	VCCINT	W20	NA
NA	VCCINT	W24	NA
NA	VCCINT	W28	NA
NA	VCCINT	Y11	NA
NA	VCCINT	Y13	NA
NA	VCCINT	Y15	NA
NA	VCCINT	Y19	NA
NA	VCCINT	Y23	NA
NA	VCCINT	Y27	NA
NA	VCCAUX	AA26	NA
NA	VCCAUX	AB17	NA
NA	VCCAUX	AC26	NA
NA	VCCAUX	AD17	NA
NA	VCCAUX	AE26	NA
NA	VCCAUX	AF17	NA
NA	VCCAUX	AG26	NA
NA	VCCAUX	T17	NA
NA	VCCAUX	U26	NA

Bank	Pin name	Pin	I/O Type
NA	VCCAUX	V17	NA
NA	VCCAUX	W26	NA
NA	VCCAUX	Y17	NA
NA	VCCAUX_IO_G0	AH25	NA
NA	VCCAUX_IO_G0	AF25	NA
NA	VCCAUX_IO_G1	AD25	NA
NA	VCCAUX_IO_G1	AB25	NA
NA	VCCAUX_IO_G1	Y25	NA
NA	VCCAUX_IO_G2	V25	NA
NA	VCCAUX_IO_G2	T25	NA
NA	VCCAUX_IO_G2	R26	NA
NA	VCCAUX_IO_G3	AG18	NA
NA	VCCAUX_IO_G3	AF19	NA
NA	VCCAUX_IO_G3	AE18	NA
NA	VCCAUX_IO_G4	AC18	NA
NA	VCCAUX_IO_G4	AA18	NA
NA	VCCAUX_IO_G4	W18	NA
NA	VCCAUX_IO_G5	U18	NA
NA	VCCAUX_IO_G5	T19	NA
NA	VCCAUX_IO_G5	R18	NA
14	VCCO_14	AF28	NA
14	VCCO_14	AH32	NA
14	VCCO_14	AJ29	NA
14	VCCO_14	AK36	NA
14	VCCO_14	AL33	NA
14	VCCO_14	AM30	NA
14	VCCO_14	AN37	NA
15	VCCO_15	AM40	NA
15	VCCO_15	AR41	NA
15	VCCO_15	AT38	NA
15	VCCO_15	AV42	NA
15	VCCO_15	AW39	NA
15	VCCO_15	BB40	NA
16	VCCO_16	AA33	NA
16	VCCO_16	AB30	NA
16	VCCO_16	AD34	NA
16	VCCO_16	AE31	NA
16	VCCO_16	AG35	NA
16	VCCO_16	Y36	NA
17	VCCO_17	AB40	NA

Bank	Pin name	Pin	I/O Type
17	VCCO_17	AC37	NA
17	VCCO_17	AE41	NA
17	VCCO_17	AF38	NA
17	VCCO_17	AH42	NA
17	VCCO_17	AJ39	NA
18	VCCO_18	P34	NA
18	VCCO_18	T38	NA
18	VCCO_18	U35	NA
18	VCCO_18	V32	NA
18	VCCO_18	V42	NA
18	VCCO_18	W39	NA
19	VCCO_19	B40	NA
19	VCCO_19	E41	NA
19	VCCO_19	H42	NA
19	VCCO_19	J39	NA
19	VCCO_19	M40	NA
19	VCCO_19	N37	NA
19	VCCO_19	R41	NA
31	VCCO_31	AK16	NA
31	VCCO_31	AL13	NA
31	VCCO_31	AP14	NA
31	VCCO_31	AR11	NA
31	VCCO_31	AU15	NA
31	VCCO_31	AV12	NA
31	VCCO_31	BA13	NA
32	VCCO_32	AJ19	NA
32	VCCO_32	AN17	NA
32	VCCO_32	AT18	NA
32	VCCO_32	AW19	NA
32	VCCO_32	AY16	NA
32	VCCO_32	BB20	NA
33	VCCO_33	AL23	NA
33	VCCO_33	AM20	NA
33	VCCO_33	AP24	NA
33	VCCO_33	AR21	NA
33	VCCO_33	AV22	NA
33	VCCO_33	BA23	NA
34	VCCO_34	H32	NA
34	VCCO_34	L33	NA
34	VCCO_34	M30	NA

Bank	Pin name	Pin	I/O Type
34	VCCO_34	R31	NA
34	VCCO_34	T28	NA
34	VCCO_34	W29	NA
35	VCCO_35	A33	NA
35	VCCO_35	C37	NA
35	VCCO_35	D34	NA
35	VCCO_35	E31	NA
35	VCCO_35	F38	NA
35	VCCO_35	G35	NA
35	VCCO_35	K36	NA
36	VCCO_36	G25	NA
36	VCCO_36	H22	NA
36	VCCO_36	J29	NA
36	VCCO_36	K26	NA
36	VCCO_36	L23	NA
36	VCCO_36	N27	NA
36	VCCO_36	P24	NA
37	VCCO_37	A23	NA
37	VCCO_37	B30	NA
37	VCCO_37	C27	NA
37	VCCO_37	D24	NA
37	VCCO_37	E21	NA
37	VCCO_37	F28	NA
38	VCCO_38	B20	NA
38	VCCO_38	C17	NA
38	VCCO_38	F18	NA
38	VCCO_38	J19	NA
38	VCCO_38	M20	NA
38	VCCO_38	N17	NA
39	VCCO_39	D14	NA
39	VCCO_39	G15	NA
39	VCCO_39	H12	NA
39	VCCO_39	K16	NA
39	VCCO_39	L13	NA
39	VCCO_39	P14	NA
0	VCCO_0	M10	NA
0	VCCO_0	T11	NA
12	VCCO_12	AK26	NA
12	VCCO_12	AN27	NA
12	VCCO_12	AT28	NA

Bank	Pin name	Pin	I/O Type
12	VCCO_12	AU25	NA
12	VCCO_12	AW29	NA
12	VCCO_12	AY26	NA
13	VCCO_13	AP34	NA
13	VCCO_13	AR31	NA
13	VCCO_13	AU35	NA
13	VCCO_13	AV32	NA
13	VCCO_13	AY36	NA
13	VCCO_13	BA33	NA
13	VCCO_13	BB30	NA
NA	VCCBRAM	AA22	NA
NA	VCCBRAM	AC22	NA
NA	VCCBRAM	AE22	NA
NA	VCCBRAM	AG22	NA
NA	VCCBRAM	AH21	NA
NA	VCCBRAM	R22	NA
NA	VCCBRAM	U22	NA
NA	VCCBRAM	W22	NA
NA	NC	W9	NA
NA	NC	W10	NA
NA	NC	AC9	NA
NA	NC	AC10	NA

Table 3 BQ7VX690TBG1927-PBGA1927 Pinout

Bank	Pin name	Pin	I/O Type
0	DXN_0	AE22	CONFIG
0	VCCADC_0	AB23	CONFIG
0	GNDADC_0	AB22	CONFIG
0	DXP_0	AE23	CONFIG
0	VREFN_0	AC22	CONFIG
0	VREFP_0	AD23	CONFIG
0	VP_0	AC23	CONFIG
0	VN_0	AD22	CONFIG
0	VCCBATT_0	AE35	CONFIG
0	CCLK_0	AE34	CONFIG
0	TCK_0	AF35	CONFIG
0	TMS_0	AF34	CONFIG
0	TDO_0	AG34	CONFIG
0	TDI_0	AG35	CONFIG
0	INIT_B_0	AK34	CONFIG

Bank	Pin name	Pin	I/O Type
0	PROGRAM_B_0	AE10	CONFIG
0	CFGBVS_0	AK11	CONFIG
0	DONE_0	AE11	CONFIG
0	M2_0	AF10	CONFIG
0	M0_0	AG11	CONFIG
0	M1_0	AG10	CONFIG
14	IO_0_VRN_14	AT30	HP
14	IO_L1P_T0_D00_MOSI_14	BC27	HP
14	IO_L1N_T0_D01_DIN_14	BD27	HP
14	IO_L2P_T0_D02_14	BD29	HP
14	IO_L2N_T0_D03_14	BD30	HP
14	IO_L3P_T0_DQS_PUDC_B_14	BB27	HP
14	IO_L3N_T0_DQS_EMCCLK_14	BB28	HP
14	IO_L4P_T0_D04_14	BB30	HP
14	IO_L4N_T0_D05_14	BC30	HP
14	IO_L5P_T0_D06_14	BC28	HP
14	IO_L5N_T0_D07_14	BC29	HP
14	IO_L6P_T0_FCS_B_14	BA29	HP
14	IO_L6N_T0_D08_VREF_14	BA30	HP
14	IO_L7P_T1_D09_14	AW29	HP
14	IO_L7N_T1_D10_14	AY29	HP
14	IO_L8P_T1_D11_14	AW27	HP
14	IO_L8N_T1_D12_14	AY27	HP
14	IO_L9P_T1_DQS_14	AY31	HP
14	IO_L9N_T1_DQS_D13_14	BA31	HP
14	IO_L10P_T1_D14_14	AY28	HP
14	IO_L10N_T1_D15_14	BA28	HP
14	IO_L11P_T1_SRCC_14	AW30	HP
14	IO_L11N_T1_SRCC_14	AW31	HP
14	IO_L12P_T1_MRCC_14	AV27	HP
14	IO_L12N_T1_MRCC_14	AV28	HP
14	IO_L13P_T2_MRCC_14	AU30	HP
14	IO_L13N_T2_MRCC_14	AV30	HP
14	IO_L14P_T2_SRCC_14	AU28	HP
14	IO_L14N_T2_SRCC_14	AV29	HP
14	IO_L15P_T2_DQS_RDWR_B_14	AN27	HP
14	IO_L15N_T2_DQS_DOUT_CSO_B_14	AP27	HP
14	IO_L16P_T2_CSI_B_14	AT28	HP
14	IO_L16N_T2_A15_D31_14	AT29	HP
14	IO_L17P_T2_A14_D30_14	AP29	HP

Bank	Pin name	Pin	I/O Type
14	IO_L17N_T2_A13_D29_14	AP30	HP
14	IO_L18P_T2_A12_D28_14	AR28	HP
14	IO_L18N_T2_A11_D27_14	AR29	HP
14	IO_L19P_T3_A10_D26_14	AN28	HP
14	IO_L19N_T3_A09_D25_VREF_14	AN29	HP
14	IO_L20P_T3_A08_D24_14	AM30	HP
14	IO_L20N_T3_A07_D23_14	AN30	HP
14	IO_L21P_T3_DQS_14	AK27	HP
14	IO_L21N_T3_DQS_A06_D22_14	AK28	HP
14	IO_L22P_T3_A05_D21_14	AM27	HP
14	IO_L22N_T3_A04_D20_14	AM28	HP
14	IO_L23P_T3_A03_D19_14	AJ29	HP
14	IO_L23N_T3_A02_D18_14	AK29	HP
14	IO_L24P_T3_A01_D17_14	AL28	HP
14	IO_L24N_T3_A00_D16_14	AL29	HP
14	IO_25_VRP_14	AR27	HP
15	IO_0_VRN_15	AR24	HP
15	IO_L1P_T0_AD0P_15	BD25	HP
15	IO_L1N_T0_AD0N_15	BD26	HP
15	IO_L2P_T0_AD8P_15	BB23	HP
15	IO_L2N_T0_AD8N_15	BC23	HP
15	IO_L3P_T0_DQS_AD1P_15	BB25	HP
15	IO_L3N_T0_DQS_AD1N_15	BC25	HP
15	IO_L4P_T0_15	BC24	HP
15	IO_L4N_T0_15	BD24	HP
15	IO_L5P_T0_AD9P_15	BA26	HP
15	IO_L5N_T0_AD9N_15	BB26	HP
15	IO_L6P_T0_15	BA24	HP
15	IO_L6N_T0_VREF_15	BA25	HP
15	IO_L7P_T1_AD2P_15	AW26	HP
15	IO_L7N_T1_AD2N_15	AY26	HP
15	IO_L8P_T1_AD10P_15	AY23	HP
15	IO_L8N_T1_AD10N_15	BA23	HP
15	IO_L9P_T1_DQS_AD3P_15	AV25	HP
15	IO_L9N_T1_DQS_AD3N_15	AW25	HP
15	IO_L10P_T1_AD11P_15	AW24	HP
15	IO_L10N_T1_AD11N_15	AY24	HP
15	IO_L11P_T1_SRCC_15	AV23	HP
15	IO_L11N_T1_SRCC_15	AV24	HP
15	IO_L12P_T1_MRCC_15	AU25	HP

Bank	Pin name	Pin	I/O Type
15	IO_L12N_T1_MRCC_15	AU26	HP
15	IO_L13P_T2_MRCC_15	AT23	HP
15	IO_L13N_T2_MRCC_15	AU23	HP
15	IO_L14P_T2_SRCC_15	AT24	HP
15	IO_L14N_T2_SRCC_15	AT25	HP
15	IO_L15P_T2_DQS_15	AN23	HP
15	IO_L15N_T2_DQS_ADV_B_15	AN24	HP
15	IO_L16P_T2_A28_15	AT26	HP
15	IO_L16N_T2_A27_15	AU27	HP
15	IO_L17P_T2_A26_15	AP24	HP
15	IO_L17N_T2_A25_15	AP25	HP
15	IO_L18P_T2_A24_15	AN25	HP
15	IO_L18N_T2_A23_15	AP26	HP
15	IO_L19P_T3_A22_15	AL23	HP
15	IO_L19N_T3_A21_VREF_15	AM23	HP
15	IO_L20P_T3_A20_15	AM25	HP
15	IO_L20N_T3_A19_15	AM26	HP
15	IO_L21P_T3_DQS_15	AK23	HP
15	IO_L21N_T3_DQS_A18_15	AK24	HP
15	IO_L22P_T3_A17_15	AK26	HP
15	IO_L22N_T3_A16_15	AL26	HP
15	IO_L23P_T3_FOE_B_15	AL24	HP
15	IO_L23N_T3_FWE_B_15	AL25	HP
15	IO_L24P_T3_RS1_15	AJ25	HP
15	IO_L24N_T3_RS0_15	AJ26	HP
15	IO_25_VRP_15	AR26	HP
16	IO_0_VRN_16	AU35	HP
16	IO_L1P_T0_16	AK33	HP
16	IO_L1N_T0_16	AL33	HP
16	IO_L2P_T0_16	AJ30	HP
16	IO_L2N_T0_16	AJ31	HP
16	IO_L3P_T0_DQS_16	AK31	HP
16	IO_L3N_T0_DQS_16	AL31	HP
16	IO_L4P_T0_16	AJ32	HP
16	IO_L4N_T0_16	AK32	HP
16	IO_L5P_T0_16	AL30	HP
16	IO_L5N_T0_16	AM31	HP
16	IO_L6P_T0_16	AM32	HP
16	IO_L6N_T0_VREF_16	AM33	HP
16	IO_L7P_T1_16	AN32	HP

Bank	Pin name	Pin	I/O Type
16	IO_L7N_T1_16	AN33	HP
16	IO_L8P_T1_16	AR33	HP
16	IO_L8N_T1_16	AT33	HP
16	IO_L9P_T1_DQS_16	AP31	HP
16	IO_L9N_T1_DQS_16	AP32	HP
16	IO_L10P_T1_16	AR31	HP
16	IO_L10N_T1_16	AR32	HP
16	IO_L11P_T1_SRCC_16	AU31	HP
16	IO_L11N_T1_SRCC_16	AU32	HP
16	IO_L12P_T1_MRCC_16	AU33	HP
16	IO_L12N_T1_MRCC_16	AV33	HP
16	IO_L13P_T2_MRCC_16	AV32	HP
16	IO_L13N_T2_MRCC_16	AW32	HP
16	IO_L14P_T2_SRCC_16	AV34	HP
16	IO_L14N_T2_SRCC_16	AV35	HP
16	IO_L15P_T2_DQS_16	AW34	HP
16	IO_L15N_T2_DQS_16	AW35	HP
16	IO_L16P_T2_16	AY33	HP
16	IO_L16N_T2_16	AY34	HP
16	IO_L17P_T2_16	BA34	HP
16	IO_L17N_T2_16	BA35	HP
16	IO_L18P_T2_16	AY32	HP
16	IO_L18N_T2_16	BA33	HP
16	IO_L19P_T3_16	BB31	HP
16	IO_L19N_T3_VREF_16	BB32	HP
16	IO_L20P_T3_16	BB35	HP
16	IO_L20N_T3_16	BC35	HP
16	IO_L21P_T3_DQS_16	BC32	HP
16	IO_L21N_T3_DQS_16	BC33	HP
16	IO_L22P_T3_16	BB33	HP
16	IO_L22N_T3_16	BC34	HP
16	IO_L23P_T3_16	BD31	HP
16	IO_L23N_T3_16	BD32	HP
16	IO_L24P_T3_16	BD34	HP
16	IO_L24N_T3_16	BD35	HP
16	IO_25_VRP_16	AT31	HP
17	IO_0_VRN_17	M26	HP
17	IO_L1P_T0_17	B23	HP
17	IO_L1N_T0_17	A23	HP
17	IO_L2P_T0_17	C25	HP

Bank	Pin name	Pin	I/O Type
17	IO_L2N_T0_17	B25	HP
17	IO_L3P_T0_DQS_17	C23	HP
17	IO_L3N_T0_DQS_17	C24	HP
17	IO_L4P_T0_17	A24	HP
17	IO_L4N_T0_17	A25	HP
17	IO_L5P_T0_17	D24	HP
17	IO_L5N_T0_17	D25	HP
17	IO_L6P_T0_17	E23	HP
17	IO_L6N_T0_VREF_17	E24	HP
17	IO_L7P_T1_17	G23	HP
17	IO_L7N_T1_17	F23	HP
17	IO_L8P_T1_17	F24	HP
17	IO_L8N_T1_17	F25	HP
17	IO_L9P_T1_DQS_17	H23	HP
17	IO_L9N_T1_DQS_17	H24	HP
17	IO_L10P_T1_17	G25	HP
17	IO_L10N_T1_17	G26	HP
17	IO_L11P_T1_SRCC_17	J24	HP
17	IO_L11N_T1_SRCC_17	H25	HP
17	IO_L12P_T1_MRCC_17	J25	HP
17	IO_L12N_T1_MRCC_17	J26	HP
17	IO_L13P_T2_MRCC_17	K23	HP
17	IO_L13N_T2_MRCC_17	K24	HP
17	IO_L14P_T2_SRCC_17	L24	HP
17	IO_L14N_T2_SRCC_17	L25	HP
17	IO_L15P_T2_DQS_17	L26	HP
17	IO_L15N_T2_DQS_17	K26	HP
17	IO_L16P_T2_17	N23	HP
17	IO_L16N_T2_17	N24	HP
17	IO_L17P_T2_17	N25	HP
17	IO_L17N_T2_17	M25	HP
17	IO_L18P_T2_17	M23	HP
17	IO_L18N_T2_17	L23	HP
17	IO_L19P_T3_17	T24	HP
17	IO_L19N_T3_VREF_17	T25	HP
17	IO_L20P_T3_17	P25	HP
17	IO_L20N_T3_17	P26	HP
17	IO_L21P_T3_DQS_17	U25	HP
17	IO_L21N_T3_DQS_17	U26	HP
17	IO_L22P_T3_17	T26	HP

Bank	Pin name	Pin	I/O Type
17	IO_L22N_T3_17	R26	HP
17	IO_L23P_T3_17	U23	HP
17	IO_L23N_T3_17	T23	HP
17	IO_L24P_T3_17	R23	HP
17	IO_L24N_T3_17	R24	HP
17	IO_25_VRP_17	P24	HP
18	IO_0_VRN_18	L30	HP
18	IO_L1P_T0_18	C30	HP
18	IO_L1N_T0_18	B30	HP
18	IO_L2P_T0_18	B33	HP
18	IO_L2N_T0_18	A33	HP
18	IO_L3P_T0_DQS_18	A30	HP
18	IO_L3N_T0_DQS_18	A31	HP
18	IO_L4P_T0_18	C32	HP
18	IO_L4N_T0_18	C33	HP
18	IO_L5P_T0_18	B31	HP
18	IO_L5N_T0_18	B32	HP
18	IO_L6P_T0_18	D30	HP
18	IO_L6N_T0_VREF_18	D31	HP
18	IO_L7P_T1_18	E31	HP
18	IO_L7N_T1_18	D32	HP
18	IO_L8P_T1_18	E32	HP
18	IO_L8N_T1_18	E33	HP
18	IO_L9P_T1_DQS_18	F30	HP
18	IO_L9N_T1_DQS_18	F31	HP
18	IO_L10P_T1_18	G33	HP
18	IO_L10N_T1_18	F33	HP
18	IO_L11P_T1_SRCC_18	G31	HP
18	IO_L11N_T1_SRCC_18	G32	HP
18	IO_L12P_T1_MRCC_18	H30	HP
18	IO_L12N_T1_MRCC_18	G30	HP
18	IO_L13P_T2_MRCC_18	H32	HP
18	IO_L13N_T2_MRCC_18	H33	HP
18	IO_L14P_T2_SRCC_18	J30	HP
18	IO_L14N_T2_SRCC_18	J31	HP
18	IO_L15P_T2_DQS_18	L31	HP
18	IO_L15N_T2_DQS_18	K31	HP
18	IO_L16P_T2_18	K32	HP
18	IO_L16N_T2_18	J32	HP
18	IO_L17P_T2_18	M31	HP

Bank	Pin name	Pin	I/O Type
18	IO_L17N_T2_18	M32	HP
18	IO_L18P_T2_18	L33	HP
18	IO_L18N_T2_18	K33	HP
18	IO_L19P_T3_18	R32	HP
18	IO_L19N_T3_VREF_18	P32	HP
18	IO_L20P_T3_18	N33	HP
18	IO_L20N_T3_18	M33	HP
18	IO_L21P_T3_DQS_18	T31	HP
18	IO_L21N_T3_DQS_18	R31	HP
18	IO_L22P_T3_18	P31	HP
18	IO_L22N_T3_18	N32	HP
18	IO_L23P_T3_18	U32	HP
18	IO_L23N_T3_18	U33	HP
18	IO_L24P_T3_18	T33	HP
18	IO_L24N_T3_18	R33	HP
18	IO_25_VRP_18	U31	HP
19	IO_0_VRN_19	M27	HP
19	IO_L1P_T0_19	A28	HP
19	IO_L1N_T0_19	A29	HP
19	IO_L2P_T0_19	D29	HP
19	IO_L2N_T0_19	C29	HP
19	IO_L3P_T0_DQS_19	C27	HP
19	IO_L3N_T0_DQS_19	B27	HP
19	IO_L4P_T0_19	C28	HP
19	IO_L4N_T0_19	B28	HP
19	IO_L5P_T0_19	B26	HP
19	IO_L5N_T0_19	A26	HP
19	IO_L6P_T0_19	D26	HP
19	IO_L6N_T0_VREF_19	D27	HP
19	IO_L7P_T1_19	G28	HP
19	IO_L7N_T1_19	F28	HP
19	IO_L8P_T1_19	F26	HP
19	IO_L8N_T1_19	E26	HP
19	IO_L9P_T1_DQS_19	F29	HP
19	IO_L9N_T1_DQS_19	E29	HP
19	IO_L10P_T1_19	E27	HP
19	IO_L10N_T1_19	E28	HP
19	IO_L11P_T1_SRCC_19	H27	HP
19	IO_L11N_T1_SRCC_19	G27	HP
19	IO_L12P_T1_MRCC_19	H28	HP

Bank	Pin name	Pin	I/O Type
19	IO_L12N_T1_MRCC_19	H29	HP
19	IO_L13P_T2_MRCC_19	K27	HP
19	IO_L13N_T2_MRCC_19	J27	HP
19	IO_L14P_T2_SRCC_19	K28	HP
19	IO_L14N_T2_SRCC_19	J29	HP
19	IO_L15P_T2_DQS_19	N30	HP
19	IO_L15N_T2_DQS_19	M30	HP
19	IO_L16P_T2_19	L28	HP
19	IO_L16N_T2_19	K29	HP
19	IO_L17P_T2_19	N28	HP
19	IO_L17N_T2_19	N29	HP
19	IO_L18P_T2_19	M28	HP
19	IO_L18N_T2_19	L29	HP
19	IO_L19P_T3_19	P29	HP
19	IO_L19N_T3_VREF_19	P30	HP
19	IO_L20P_T3_19	T28	HP
19	IO_L20N_T3_19	T29	HP
19	IO_L21P_T3_DQS_19	R28	HP
19	IO_L21N_T3_DQS_19	R29	HP
19	IO_L22P_T3_19	U30	HP
19	IO_L22N_T3_19	T30	HP
19	IO_L23P_T3_19	R27	HP
19	IO_L23N_T3_19	P27	HP
19	IO_L24P_T3_19	U27	HP
19	IO_L24N_T3_19	U28	HP
19	IO_25_VRP_19	N27	HP
34	IO_0_VRN_34	AP15	HP
34	IO_L1P_T0_34	BA18	HP
34	IO_L1N_T0_34	BB18	HP
34	IO_L2P_T0_34	BC19	HP
34	IO_L2N_T0_34	BC18	HP
34	IO_L3P_T0_DQS_34	BB17	HP
34	IO_L3N_T0_DQS_34	BC17	HP
34	IO_L4P_T0_34	BD17	HP
34	IO_L4N_T0_34	BD16	HP
34	IO_L5P_T0_34	BC15	HP
34	IO_L5N_T0_34	BD15	HP
34	IO_L6P_T0_34	BB16	HP
34	IO_L6N_T0_VREF_34	BB15	HP
34	IO_L7P_T1_34	AW17	HP

Bank	Pin name	Pin	I/O Type
34	IO_L7N_T1_34	AY16	HP
34	IO_L8P_T1_34	AY18	HP
34	IO_L8N_T1_34	AY17	HP
34	IO_L9P_T1_DQS_34	AW16	HP
34	IO_L9N_T1_DQS_34	AW15	HP
34	IO_L10P_T1_34	BA16	HP
34	IO_L10N_T1_34	BA15	HP
34	IO_L11P_T1_SRCC_34	AV18	HP
34	IO_L11N_T1_SRCC_34	AV17	HP
34	IO_L12P_T1_MRCC_34	AU15	HP
34	IO_L12N_T1_MRCC_34	AV15	HP
34	IO_L13P_T2_MRCC_34	AT18	HP
34	IO_L13N_T2_MRCC_34	AU18	HP
34	IO_L14P_T2_SRCC_34	AU17	HP
34	IO_L14N_T2_SRCC_34	AU16	HP
34	IO_L15P_T2_DQS_34	AP16	HP
34	IO_L15N_T2_DQS_34	AR16	HP
34	IO_L16P_T2_34	AR18	HP
34	IO_L16N_T2_34	AR17	HP
34	IO_L17P_T2_34	AT16	HP
34	IO_L17N_T2_34	AT15	HP
34	IO_L18P_T2_34	AN17	HP
34	IO_L18N_T2_34	AP17	HP
34	IO_L19P_T3_34	AM18	HP
34	IO_L19N_T3_VREF_34	AN18	HP
34	IO_L20P_T3_34	AM15	HP
34	IO_L20N_T3_34	AN15	HP
34	IO_L21P_T3_DQS_34	AK18	HP
34	IO_L21N_T3_DQS_34	AL18	HP
34	IO_L22P_T3_34	AM17	HP
34	IO_L22N_T3_34	AM16	HP
34	IO_L23P_T3_34	AJ16	HP
34	IO_L23N_T3_34	AK16	HP
34	IO_L24P_T3_34	AL16	HP
34	IO_L24N_T3_34	AL15	HP
34	IO_25_VRP_34	AK17	HP
35	IO_0_VRN_35	AR23	HP
35	IO_L1P_T0_AD4P_35	BB22	HP
35	IO_L1N_T0_AD4N_35	BB21	HP
35	IO_L2P_T0_AD12P_35	BC22	HP

Bank	Pin name	Pin	I/O Type
35	IO_L2N_T0_AD12N_35	BD22	HP
35	IO_L3P_T0_DQS_AD5P_35	BC20	HP
35	IO_L3N_T0_DQS_AD5N_35	BD19	HP
35	IO_L4P_T0_35	BD21	HP
35	IO_L4N_T0_35	BD20	HP
35	IO_L5P_T0_AD13P_35	BA21	HP
35	IO_L5N_T0_AD13N_35	BB20	HP
35	IO_L6P_T0_35	BA20	HP
35	IO_L6N_T0_VREF_35	BA19	HP
35	IO_L7P_T1_AD6P_35	AW22	HP
35	IO_L7N_T1_AD6N_35	AY22	HP
35	IO_L8P_T1_AD14P_35	AV20	HP
35	IO_L8N_T1_AD14N_35	AW20	HP
35	IO_L9P_T1_DQS_AD7P_35	AW21	HP
35	IO_L9N_T1_DQS_AD7N_35	AY21	HP
35	IO_L10P_T1_AD15P_35	AW19	HP
35	IO_L10N_T1_AD15N_35	AY19	HP
35	IO_L11P_T1_SRCC_35	AU22	HP
35	IO_L11N_T1_SRCC_35	AV22	HP
35	IO_L12P_T1_MRCC_35	AU20	HP
35	IO_L12N_T1_MRCC_35	AV19	HP
35	IO_L13P_T2_MRCC_35	AT21	HP
35	IO_L13N_T2_MRCC_35	AU21	HP
35	IO_L14P_T2_SRCC_35	AT20	HP
35	IO_L14N_T2_SRCC_35	AT19	HP
35	IO_L15P_T2_DQS_35	AP21	HP
35	IO_L15N_T2_DQS_35	AP20	HP
35	IO_L16P_T2_35	AR22	HP
35	IO_L16N_T2_35	AR21	HP
35	IO_L17P_T2_35	AN20	HP
35	IO_L17N_T2_35	AP19	HP
35	IO_L18P_T2_35	AN22	HP
35	IO_L18N_T2_35	AP22	HP
35	IO_L19P_T3_35	AM22	HP
35	IO_L19N_T3_VREF_35	AM21	HP
35	IO_L20P_T3_35	AJ22	HP
35	IO_L20N_T3_35	AJ21	HP
35	IO_L21P_T3_DQS_35	AM20	HP
35	IO_L21N_T3_DQS_35	AN19	HP
35	IO_L22P_T3_35	AK22	HP

Bank	Pin name	Pin	I/O Type
35	IO_L22N_T3_35	AK21	HP
35	IO_L23P_T3_35	AL21	HP
35	IO_L23N_T3_35	AL20	HP
35	IO_L24P_T3_35	AK19	HP
35	IO_L24N_T3_35	AL19	HP
35	IO_25_VRP_35	AR19	HP
36	IO_0_VRN_36	AP12	HP
36	IO_L1P_T0_36	AJ14	HP
36	IO_L1N_T0_36	AK14	HP
36	IO_L2P_T0_36	AM13	HP
36	IO_L2N_T0_36	AM12	HP
36	IO_L3P_T0_DQS_36	AK13	HP
36	IO_L3N_T0_DQS_36	AK12	HP
36	IO_L4P_T0_36	AN13	HP
36	IO_L4N_T0_36	AN12	HP
36	IO_L5P_T0_36	AL14	HP
36	IO_L5N_T0_36	AL13	HP
36	IO_L6P_T0_36	AN14	HP
36	IO_L6N_T0_VREF_36	AP14	HP
36	IO_L7P_T1_36	AR13	HP
36	IO_L7N_T1_36	AR12	HP
36	IO_L8P_T1_36	AU12	HP
36	IO_L8N_T1_36	AU11	HP
36	IO_L9P_T1_DQS_36	AT14	HP
36	IO_L9N_T1_DQS_36	AT13	HP
36	IO_L10P_T1_36	AU10	HP
36	IO_L10N_T1_36	AV10	HP
36	IO_L11P_T1_SRCC_36	AV12	HP
36	IO_L11N_T1_SRCC_36	AW12	HP
36	IO_L12P_T1_MRCC_36	AU13	HP
36	IO_L12N_T1_MRCC_36	AV13	HP
36	IO_L13P_T2_MRCC_36	AV14	HP
36	IO_L13N_T2_MRCC_36	AW14	HP
36	IO_L14P_T2_SRCC_36	AW11	HP
36	IO_L14N_T2_SRCC_36	AW10	HP
36	IO_L15P_T2_DQS_36	AY13	HP
36	IO_L15N_T2_DQS_36	BA13	HP
36	IO_L16P_T2_36	AY12	HP
36	IO_L16N_T2_36	AY11	HP
36	IO_L17P_T2_36	BA11	HP

Bank	Pin name	Pin	I/O Type
36	IO_L17N_T2_36	BA10	HP
36	IO_L18P_T2_36	AY14	HP
36	IO_L18N_T2_36	BA14	HP
36	IO_L19P_T3_36	BB11	HP
36	IO_L19N_T3_VREF_36	BB10	HP
36	IO_L20P_T3_36	BB12	HP
36	IO_L20N_T3_36	BC12	HP
36	IO_L21P_T3_DQS_36	BD12	HP
36	IO_L21N_T3_DQS_36	BD11	HP
36	IO_L22P_T3_36	BB13	HP
36	IO_L22N_T3_36	BC13	HP
36	IO_L23P_T3_36	BC14	HP
36	IO_L23N_T3_36	BD14	HP
36	IO_L24P_T3_36	BC10	HP
36	IO_L24N_T3_36	BD10	HP
36	IO_25_VRP_36	AR14	HP
37	IO_0_VRN_37	P19	HP
37	IO_L1P_T0_37	B21	HP
37	IO_L1N_T0_37	A21	HP
37	IO_L2P_T0_37	B20	HP
37	IO_L2N_T0_37	A20	HP
37	IO_L3P_T0_DQS_37	C22	HP
37	IO_L3N_T0_DQS_37	B22	HP
37	IO_L4P_T0_37	D20	HP
37	IO_L4N_T0_37	C20	HP
37	IO_L5P_T0_37	D22	HP
37	IO_L5N_T0_37	D21	HP
37	IO_L6P_T0_37	E22	HP
37	IO_L6N_T0_VREF_37	E21	HP
37	IO_L7P_T1_37	G21	HP
37	IO_L7N_T1_37	F21	HP
37	IO_L8P_T1_37	F20	HP
37	IO_L8N_T1_37	F19	HP
37	IO_L9P_T1_DQS_37	H22	HP
37	IO_L9N_T1_DQS_37	G22	HP
37	IO_L10P_T1_37	J19	HP
37	IO_L10N_T1_37	H19	HP
37	IO_L11P_T1_SRCC_37	J21	HP
37	IO_L11N_T1_SRCC_37	J20	HP
37	IO_L12P_T1_MRCC_37	H20	HP

Bank	Pin name	Pin	I/O Type
37	IO_L12N_T1_MRCC_37	G20	HP
37	IO_L13P_T2_MRCC_37	K22	HP
37	IO_L13N_T2_MRCC_37	J22	HP
37	IO_L14P_T2_SRCC_37	L21	HP
37	IO_L14N_T2_SRCC_37	K21	HP
37	IO_L15P_T2_DQS_37	L19	HP
37	IO_L15N_T2_DQS_37	K19	HP
37	IO_L16P_T2_37	M20	HP
37	IO_L16N_T2_37	L20	HP
37	IO_L17P_T2_37	N20	HP
37	IO_L17N_T2_37	N19	HP
37	IO_L18P_T2_37	N22	HP
37	IO_L18N_T2_37	M22	HP
37	IO_L19P_T3_37	U20	HP
37	IO_L19N_T3_VREF_37	T20	HP
37	IO_L20P_T3_37	T19	HP
37	IO_L20N_T3_37	R19	HP
37	IO_L21P_T3_DQS_37	U22	HP
37	IO_L21N_T3_DQS_37	U21	HP
37	IO_L22P_T3_37	P21	HP
37	IO_L22N_T3_37	P20	HP
37	IO_L23P_T3_37	R22	HP
37	IO_L23N_T3_37	P22	HP
37	IO_L24P_T3_37	T21	HP
37	IO_L24N_T3_37	R21	HP
37	IO_25_VRP_37	M21	HP
38	IO_0_VRN_38	L15	HP
38	IO_L1P_T0_38	C15	HP
38	IO_L1N_T0_38	C14	HP
38	IO_L2P_T0_38	B15	HP
38	IO_L2N_T0_38	A15	HP
38	IO_L3P_T0_DQS_38	B13	HP
38	IO_L3N_T0_DQS_38	B12	HP
38	IO_L4P_T0_38	A14	HP
38	IO_L4N_T0_38	A13	HP
38	IO_L5P_T0_38	C13	HP
38	IO_L5N_T0_38	C12	HP
38	IO_L6P_T0_38	D15	HP
38	IO_L6N_T0_VREF_38	D14	HP
38	IO_L7P_T1_38	E12	HP

Bank	Pin name	Pin	I/O Type
38	IO_L7N_T1_38	D12	HP
38	IO_L8P_T1_38	E14	HP
38	IO_L8N_T1_38	E13	HP
38	IO_L9P_T1_DQS_38	G15	HP
38	IO_L9N_T1_DQS_38	F15	HP
38	IO_L10P_T1_38	F14	HP
38	IO_L10N_T1_38	F13	HP
38	IO_L11P_T1_SRCC_38	H13	HP
38	IO_L11N_T1_SRCC_38	G13	HP
38	IO_L12P_T1_MRCC_38	H15	HP
38	IO_L12N_T1_MRCC_38	H14	HP
38	IO_L13P_T2_MRCC_38	J15	HP
38	IO_L13N_T2_MRCC_38	J14	HP
38	IO_L14P_T2_SRCC_38	K14	HP
38	IO_L14N_T2_SRCC_38	K13	HP
38	IO_L15P_T2_DQS_38	H12	HP
38	IO_L15N_T2_DQS_38	G12	HP
38	IO_L16P_T2_38	M13	HP
38	IO_L16N_T2_38	L13	HP
38	IO_L17P_T2_38	M15	HP
38	IO_L17N_T2_38	L14	HP
38	IO_L18P_T2_38	K12	HP
38	IO_L18N_T2_38	J12	HP
38	IO_L19P_T3_38	R14	HP
38	IO_L19N_T3_VREF_38	P14	HP
38	IO_L20P_T3_38	N14	HP
38	IO_L20N_T3_38	N13	HP
38	IO_L21P_T3_DQS_38	T14	HP
38	IO_L21N_T3_DQS_38	R13	HP
38	IO_L22P_T3_38	N12	HP
38	IO_L22N_T3_38	M12	HP
38	IO_L23P_T3_38	U13	HP
38	IO_L23N_T3_38	T13	HP
38	IO_L24P_T3_38	R12	HP
38	IO_L24N_T3_38	P12	HP
38	IO_25_VRP_38	U12	HP
39	IO_0_VRN_39	K18	HP
39	IO_L1P_T0_39	C18	HP
39	IO_L1N_T0_39	B18	HP
39	IO_L2P_T0_39	B16	HP

Bank	Pin name	Pin	I/O Type
39	IO_L2N_T0_39	A16	HP
39	IO_L3P_T0_DQS_39	D19	HP
39	IO_L3N_T0_DQS_39	C19	HP
39	IO_L4P_T0_39	C17	HP
39	IO_L4N_T0_39	B17	HP
39	IO_L5P_T0_39	A19	HP
39	IO_L5N_T0_39	A18	HP
39	IO_L6P_T0_39	D17	HP
39	IO_L6N_T0_VREF_39	D16	HP
39	IO_L7P_T1_39	E17	HP
39	IO_L7N_T1_39	E16	HP
39	IO_L8P_T1_39	G18	HP
39	IO_L8N_T1_39	F18	HP
39	IO_L9P_T1_DQS_39	G16	HP
39	IO_L9N_T1_DQS_39	F16	HP
39	IO_L10P_T1_39	E19	HP
39	IO_L10N_T1_39	E18	HP
39	IO_L11P_T1_SRCC_39	J17	HP
39	IO_L11N_T1_SRCC_39	H17	HP
39	IO_L12P_T1_MRCC_39	H18	HP
39	IO_L12N_T1_MRCC_39	G17	HP
39	IO_L13P_T2_MRCC_39	K17	HP
39	IO_L13N_T2_MRCC_39	J16	HP
39	IO_L14P_T2_SRCC_39	L16	HP
39	IO_L14N_T2_SRCC_39	K16	HP
39	IO_L15P_T2_DQS_39	P17	HP
39	IO_L15N_T2_DQS_39	N17	HP
39	IO_L16P_T2_39	M18	HP
39	IO_L16N_T2_39	L18	HP
39	IO_L17P_T2_39	P15	HP
39	IO_L17N_T2_39	N15	HP
39	IO_L18P_T2_39	M17	HP
39	IO_L18N_T2_39	M16	HP
39	IO_L19P_T3_39	T16	HP
39	IO_L19N_T3_VREF_39	T15	HP
39	IO_L20P_T3_39	R16	HP
39	IO_L20N_T3_39	P16	HP
39	IO_L21P_T3_DQS_39	U17	HP
39	IO_L21N_T3_DQS_39	U16	HP
39	IO_L22P_T3_39	R18	HP

Bank	Pin name	Pin	I/O Type
39	IO_L22N_T3_39	R17	HP
39	IO_L23P_T3_39	U18	HP
39	IO_L23N_T3_39	T18	HP
39	IO_L24P_T3_39	V15	HP
39	IO_L24N_T3_39	U15	HP
39	IO_25_VRP_39	N18	HP
110	MGTHTXP3_110	AY4	GTH
110	MGTHRXP3_110	AW6	GTH
110	MGTHTXN3_110	AY3	GTH
110	MGTHRXN3_110	AW5	GTH
110	MGTHTXP2_110	BA2	GTH
110	MGTHRXP2_110	BA6	GTH
110	MGTHTXN2_110	BA1	GTH
110	MGTREFCLK0P_110	AY8	GTH
110	MGTHRXN2_110	BA5	GTH
110	MGTREFCLK0N_110	AY7	GTH
110	MGTREFCLK1N_110	BB7	GTH
110	MGTREFCLK1P_110	BB8	GTH
110	MGTHTXP1_110	BB4	GTH
110	MGTHRXP1_110	BC6	GTH
110	MGTHTXN1_110	BB3	GTH
110	MGTHRXN1_110	BC5	GTH
110	MGTHTXP0_110	BD4	GTH
110	MGTHRXP0_110	BD8	GTH
110	MGTHTXN0_110	BD3	GTH
110	MGTHRXN0_110	BD7	GTH
111	MGTHTXP3_111	AT4	GTH
111	MGTHRXP3_111	AP8	GTH
111	MGTHTXN3_111	AT3	GTH
111	MGTHRXN3_111	AP7	GTH
111	MGTHTXP2_111	AU2	GTH
111	MGTHRXP2_111	AR6	GTH
111	MGTHTXN2_111	AU1	GTH
111	MGTREFCLK0P_111	AR10	GTH
111	MGTHRXN2_111	AR5	GTH
111	MGTREFCLK0N_111	AR9	GTH
111	MGTREFCLK1N_111	AT7	GTH
111	MGTREFCLK1P_111	AT8	GTH
111	MGTHTXP1_111	AV4	GTH
111	MGTHRXP1_111	AU6	GTH

Bank	Pin name	Pin	I/O Type
111	MGTHTXN1_111	AV3	GTH
111	MGTHRXN1_111	AU5	GTH
111	MGTHTXP0_111	AW2	GTH
111	MGTHRXP0_111	AV8	GTH
111	MGTHTXN0_111	AW1	GTH
111	MGTHRXN0_111	AV7	GTH
112	MGTHTXP3_112	AL2	GTH
112	MGTHRXP3_112	AL6	GTH
112	MGTHTXN3_112	AL1	GTH
112	MGTHRXN3_112	AL5	GTH
112	MGTHTXP2_112	AN2	GTH
112	MGTHRXP2_112	AM8	GTH
112	MGTHTXN2_112	AN1	GTH
112	MGTREFCLK0P_112	AL10	GTH
112	MGTHRXN2_112	AM7	GTH
112	MGTREFCLK0N_112	AL9	GTH
112	MGTREFCLK1N_112	AN9	GTH
112	MGTREFCLK1P_112	AN10	GTH
112	MGTHTXP1_112	AP4	GTH
112	MGTHRXP1_112	AM4	GTH
112	MGTHTXN1_112	AP3	GTH
112	MGTHRXN1_112	AM3	GTH
112	MGTHTXP0_112	AR2	GTH
112	MGTHRXP0_112	AN6	GTH
112	MGTHTXN0_112	AR1	GTH
112	MGTHRXN0_112	AN5	GTH
113	MGTHTXP3_113	AG2	GTH
113	MGTHRXP3_113	AE6	GTH
113	MGTHTXN3_113	AG1	GTH
113	MGTHRXN3_113	AE5	GTH
113	MGTHTXP2_113	AH4	GTH
113	MGTHRXP2_113	AG6	GTH
113	MGTHTXN2_113	AH3	GTH
113	MGTREFCLK0P_113	AF8	GTH
113	MGTHRXN2_113	AG5	GTH
113	MGTREFCLK0N_113	AF7	GTH
113	MGTREFCLK1N_113	AH7	GTH
113	MGTREFCLK1P_113	AH8	GTH
113	MGTHTXP1_113	AJ2	GTH
113	MGTHRXP1_113	AJ6	GTH

Bank	Pin name	Pin	I/O Type
113	MGTHTXN1_113	AJ1	GTH
113	MGTHRXN1_113	AJ5	GTH
113	MGTHTXP0_113	AK4	GTH
113	MGTHRXP0_113	AK8	GTH
113	MGTHTXN0_113	AK3	GTH
113	MGTHRXN0_113	AK7	GTH
114	MGTHTXP3_114	AC2	GTH
114	MGTHRXP3_114	Y8	GTH
114	MGTHTXN3_114	AC1	GTH
114	MGTHRXN3_114	Y7	GTH
114	MGTHTXP2_114	AD4	GTH
114	MGTHRXP2_114	AA6	GTH
114	MGTHTXN2_114	AD3	GTH
114	MGTREFCLK0P_114	AA10	GTH
114	MGTHRXN2_114	AA5	GTH
114	MGTREFCLK0N_114	AA9	GTH
114	MGTREFCLK1N_114	AB7	GTH
114	MGTREFCLK1P_114	AB8	GTH
114	MGTHTXP1_114	AE2	GTH
114	MGTHRXP1_114	AC6	GTH
114	MGTHTXN1_114	AE1	GTH
114	MGTHRXN1_114	AC5	GTH
114	MGTHTXP0_114	AF4	GTH
114	MGTHRXP0_114	AD8	GTH
114	MGTHTXN0_114	AF3	GTH
114	MGTHRXN0_114	AD7	GTH
115	MGTHTXP3_115	W2	GTH
115	MGTHRXP3_115	T8	GTH
115	MGTHTXN3_115	W1	GTH
115	MGTHRXN3_115	T7	GTH
115	MGTHTXP2_115	Y4	GTH
115	MGTHRXP2_115	U6	GTH
115	MGTHTXN2_115	Y3	GTH
115	MGTREFCLK0P_115	U10	GTH
115	MGTHRXN2_115	U5	GTH
115	MGTAVTTRCAL_115	AC10	GTH
115	MGTREFCLK0N_115	U9	GTH
115	MGTRREF_115	AC9	GTH
115	MGTREFCLK1N_115	W9	GTH
115	MGTREFCLK1P_115	W10	GTH

Bank	Pin name	Pin	I/O Type
115	MGTHTXP1_115	AA2	GTH
115	MGTHRXP1_115	V8	GTH
115	MGTHTXN1_115	AA1	GTH
115	MGTHRXN1_115	V7	GTH
115	MGTHTXP0_115	AB4	GTH
115	MGTHRXP0_115	W6	GTH
115	MGTHTXN0_115	AB3	GTH
115	MGTHRXN0_115	W5	GTH
116	MGTHTXP3_116	R2	GTH
116	MGTHRXP3_116	M8	GTH
116	MGTHTXN3_116	R1	GTH
116	MGTHRXN3_116	M7	GTH
116	MGTHTXP2_116	T4	GTH
116	MGTHRXP2_116	N6	GTH
116	MGTHTXN2_116	T3	GTH
116	MGTREFCLK0P_116	N10	GTH
116	MGTHRXN2_116	N5	GTH
116	MGTREFCLK0N_116	N9	GTH
116	MGTREFCLK1N_116	R9	GTH
116	MGTREFCLK1P_116	R10	GTH
116	MGTHTXP1_116	U2	GTH
116	MGTHRXP1_116	P8	GTH
116	MGTHTXN1_116	U1	GTH
116	MGTHRXN1_116	P7	GTH
116	MGTHTXP0_116	V4	GTH
116	MGTHRXP0_116	R6	GTH
116	MGTHTXN0_116	V3	GTH
116	MGTHRXN0_116	R5	GTH
117	MGTHTXP3_117	L2	GTH
117	MGTHRXP3_117	H8	GTH
117	MGTHTXN3_117	L1	GTH
117	MGTHRXN3_117	H7	GTH
117	MGTHTXP2_117	M4	GTH
117	MGTHRXP2_117	J6	GTH
117	MGTHTXN2_117	M3	GTH
117	MGTREFCLK0P_117	J10	GTH
117	MGTHRXN2_117	J5	GTH
117	MGTREFCLK0N_117	J9	GTH
117	MGTREFCLK1N_117	L9	GTH
117	MGTREFCLK1P_117	L10	GTH

Bank	Pin name	Pin	I/O Type
117	MGTHTXP1_117	N2	GTH
117	MGTHRXP1_117	K8	GTH
117	MGTHTXN1_117	N1	GTH
117	MGTHRXN1_117	K7	GTH
117	MGTHTXP0_117	P4	GTH
117	MGTHRXP0_117	L6	GTH
117	MGTHTXN0_117	P3	GTH
117	MGTHRXN0_117	L5	GTH
118	MGTHTXP3_118	G2	GTH
118	MGTHRXP3_118	D8	GTH
118	MGTHTXN3_118	G1	GTH
118	MGTHRXN3_118	D7	GTH
118	MGTHTXP2_118	H4	GTH
118	MGTHRXP2_118	E6	GTH
118	MGTHTXN2_118	H3	GTH
118	MGTREFCLK0P_118	E10	GTH
118	MGTHRXN2_118	E5	GTH
118	MGTREFCLK0N_118	E9	GTH
118	MGTREFCLK1N_118	G9	GTH
118	MGTREFCLK1P_118	G10	GTH
118	MGTHTXP1_118	J2	GTH
118	MGTHRXP1_118	F8	GTH
118	MGTHTXN1_118	J1	GTH
118	MGTHRXN1_118	F7	GTH
118	MGTHTXP0_118	K4	GTH
118	MGTHRXP0_118	G6	GTH
118	MGTHTXN0_118	K3	GTH
118	MGTHRXN0_118	G5	GTH
119	MGTHTXP3_119	B4	GTH
119	MGTHRXP3_119	A6	GTH
119	MGTHTXN3_119	B3	GTH
119	MGTHRXN3_119	A5	GTH
119	MGTHTXP2_119	C2	GTH
119	MGTHRXP2_119	B8	GTH
119	MGTHTXN2_119	C1	GTH
119	MGTREFCLK0P_119	A10	GTH
119	MGTHRXN2_119	B7	GTH
119	MGTREFCLK0N_119	A9	GTH
119	MGTREFCLK1N_119	C9	GTH
119	MGTREFCLK1P_119	C10	GTH

Bank	Pin name	Pin	I/O Type
119	MGTHTXP1_119	E2	GTH
119	MGTHRXP1_119	C6	GTH
119	MGTHTXN1_119	E1	GTH
119	MGTHRXN1_119	C5	GTH
119	MGTHTXP0_119	F4	GTH
119	MGTHRXP0_119	D4	GTH
119	MGTHTXN0_119	F3	GTH
119	MGTHRXN0_119	D3	GTH
210	MGTHTXP3_210	AY41	GTH
210	MGTHRXP3_210	AW39	GTH
210	MGTHTXN3_210	AY42	GTH
210	MGTHRXN3_210	AW40	GTH
210	MGTHTXP2_210	BA43	GTH
210	MGTHRXP2_210	BA39	GTH
210	MGTHTXN2_210	BA44	GTH
210	MGTREFCLK0P_210	AY37	GTH
210	MGTHRXN2_210	BA40	GTH
210	MGTREFCLK0N_210	AY38	GTH
210	MGTREFCLK1N_210	BB38	GTH
210	MGTREFCLK1P_210	BB37	GTH
210	MGTHTXP1_210	BB41	GTH
210	MGTHRXP1_210	BC39	GTH
210	MGTHTXN1_210	BB42	GTH
210	MGTHRXN1_210	BC40	GTH
210	MGTHTXP0_210	BD41	GTH
210	MGTHRXP0_210	BD37	GTH
210	MGTHTXN0_210	BD42	GTH
210	MGTHRXN0_210	BD38	GTH
211	MGTHTXP3_211	AT41	GTH
211	MGTHRXP3_211	AP37	GTH
211	MGTHTXN3_211	AT42	GTH
211	MGTHRXN3_211	AP38	GTH
211	MGTHTXP2_211	AU43	GTH
211	MGTHRXP2_211	AR39	GTH
211	MGTHTXN2_211	AU44	GTH
211	MGTREFCLK0P_211	AR35	GTH
211	MGTHRXN2_211	AR40	GTH
211	MGTREFCLK0N_211	AR36	GTH
211	MGTREFCLK1N_211	AT38	GTH
211	MGTREFCLK1P_211	AT37	GTH

Bank	Pin name	Pin	I/O Type
211	MGTHTXP1_211	AV41	GTH
211	MGTHRXP1_211	AU39	GTH
211	MGTHTXN1_211	AV42	GTH
211	MGTHRXN1_211	AU40	GTH
211	MGTHTXP0_211	AW43	GTH
211	MGTHRXP0_211	AV37	GTH
211	MGTHTXN0_211	AW44	GTH
211	MGTHRXN0_211	AV38	GTH
212	MGTHTXP3_212	AL43	GTH
212	MGTHRXP3_212	AL39	GTH
212	MGTHTXN3_212	AL44	GTH
212	MGTHRXN3_212	AL40	GTH
212	MGTHTXP2_212	AN43	GTH
212	MGTHRXP2_212	AM37	GTH
212	MGTHTXN2_212	AN44	GTH
212	MGTREFCLK0P_212	AL35	GTH
212	MGTHRXN2_212	AM38	GTH
212	MGTREFCLK0N_212	AL36	GTH
212	MGTREFCLK1N_212	AN36	GTH
212	MGTREFCLK1P_212	AN35	GTH
212	MGTHTXP1_212	AP41	GTH
212	MGTHRXP1_212	AM41	GTH
212	MGTHTXN1_212	AP42	GTH
212	MGTHRXN1_212	AM42	GTH
212	MGTHTXP0_212	AR43	GTH
212	MGTHRXP0_212	AN39	GTH
212	MGTHTXN0_212	AR44	GTH
212	MGTHRXN0_212	AN40	GTH
213	MGTHTXP3_213	AG43	GTH
213	MGTHRXP3_213	AE39	GTH
213	MGTHTXN3_213	AG44	GTH
213	MGTHRXN3_213	AE40	GTH
213	MGTHTXP2_213	AH41	GTH
213	MGTHRXP2_213	AG39	GTH
213	MGTHTXN2_213	AH42	GTH
213	MGTREFCLK0P_213	AF37	GTH
213	MGTHRXN2_213	AG40	GTH
213	MGTREFCLK0N_213	AF38	GTH
213	MGTREFCLK1N_213	AH38	GTH
213	MGTREFCLK1P_213	AH37	GTH

Bank	Pin name	Pin	I/O Type
213	MGTHTXP1_213	AJ43	GTH
213	MGTHRXP1_213	AJ39	GTH
213	MGTHTXN1_213	AJ44	GTH
213	MGTHRXN1_213	AJ40	GTH
213	MGTHTXP0_213	AK41	GTH
213	MGTHRXP0_213	AK37	GTH
213	MGTHTXN0_213	AK42	GTH
213	MGTHRXN0_213	AK38	GTH
214	MGTHTXP3_214	AC43	GTH
214	MGTHRXP3_214	Y37	GTH
214	MGTHTXN3_214	AC44	GTH
214	MGTHRXN3_214	Y38	GTH
214	MGTHTXP2_214	AD41	GTH
214	MGTHRXP2_214	AA39	GTH
214	MGTHTXN2_214	AD42	GTH
214	MGTREFCLK0P_214	AA35	GTH
214	MGTHRXN2_214	AA40	GTH
214	MGTREFCLK0N_214	AA36	GTH
214	MGTREFCLK1N_214	AB38	GTH
214	MGTREFCLK1P_214	AB37	GTH
214	MGTHTXP1_214	AE43	GTH
214	MGTHRXP1_214	AC39	GTH
214	MGTHTXN1_214	AE44	GTH
214	MGTHRXN1_214	AC40	GTH
214	MGTHTXP0_214	AF41	GTH
214	MGTHRXP0_214	AD37	GTH
214	MGTHTXN0_214	AF42	GTH
214	MGTHRXN0_214	AD38	GTH
215	MGTHTXP3_215	W43	GTH
215	MGTHRXP3_215	T37	GTH
215	MGTHTXN3_215	W44	GTH
215	MGTHRXN3_215	T38	GTH
215	MGTHTXP2_215	Y41	GTH
215	MGTHRXP2_215	U39	GTH
215	MGTHTXN2_215	Y42	GTH
215	MGTREFCLK0P_215	U35	GTH
215	MGTHRXN2_215	U40	GTH
215	MGTAVTTRCAL_215	AC36	GTH
215	MGTREFCLK0N_215	U36	GTH
215	MGTRREF_215	AC35	GTH

Bank	Pin name	Pin	I/O Type
215	MGTREFCLK1N_215	W36	GTH
215	MGTREFCLK1P_215	W35	GTH
215	MGTHTXP1_215	AA43	GTH
215	MGTHRXP1_215	V37	GTH
215	MGTHTXN1_215	AA44	GTH
215	MGTHRXN1_215	V38	GTH
215	MGTHTXP0_215	AB41	GTH
215	MGTHRXP0_215	W39	GTH
215	MGTHTXN0_215	AB42	GTH
215	MGTHRXN0_215	W40	GTH
216	MGTHTXP3_216	R43	GTH
216	MGTHRXP3_216	M37	GTH
216	MGTHTXN3_216	R44	GTH
216	MGTHRXN3_216	M38	GTH
216	MGTHTXP2_216	T41	GTH
216	MGTHRXP2_216	N39	GTH
216	MGTHTXN2_216	T42	GTH
216	MGTREFCLK0P_216	N35	GTH
216	MGTHRXN2_216	N40	GTH
216	MGTREFCLK0N_216	N36	GTH
216	MGTREFCLK1N_216	R36	GTH
216	MGTREFCLK1P_216	R35	GTH
216	MGTHTXP1_216	U43	GTH
216	MGTHRXP1_216	P37	GTH
216	MGTHTXN1_216	U44	GTH
216	MGTHRXN1_216	P38	GTH
216	MGTHTXP0_216	V41	GTH
216	MGTHRXP0_216	R39	GTH
216	MGTHTXN0_216	V42	GTH
216	MGTHRXN0_216	R40	GTH
217	MGTHTXP3_217	L43	GTH
217	MGTHRXP3_217	H37	GTH
217	MGTHTXN3_217	L44	GTH
217	MGTHRXN3_217	H38	GTH
217	MGTHTXP2_217	M41	GTH
217	MGTHRXP2_217	J39	GTH
217	MGTHTXN2_217	M42	GTH
217	MGTREFCLK0P_217	J35	GTH
217	MGTHRXN2_217	J40	GTH
217	MGTREFCLK0N_217	J36	GTH

Bank	Pin name	Pin	I/O Type
217	MGTREFCLK1N_217	L36	GTH
217	MGTREFCLK1P_217	L35	GTH
217	MGTHTXP1_217	N43	GTH
217	MGTHRXP1_217	K37	GTH
217	MGTHTXN1_217	N44	GTH
217	MGTHRXN1_217	K38	GTH
217	MGTHTXP0_217	P41	GTH
217	MGTHRXP0_217	L39	GTH
217	MGTHTXN0_217	P42	GTH
217	MGTHRXN0_217	L40	GTH
218	MGTHTXP3_218	G43	GTH
218	MGTHRXP3_218	D37	GTH
218	MGTHTXN3_218	G44	GTH
218	MGTHRXN3_218	D38	GTH
218	MGTHTXP2_218	H41	GTH
218	MGTHRXP2_218	E39	GTH
218	MGTHTXN2_218	H42	GTH
218	MGTREFCLK0P_218	E35	GTH
218	MGTHRXN2_218	E40	GTH
218	MGTREFCLK0N_218	E36	GTH
218	MGTREFCLK1N_218	G36	GTH
218	MGTREFCLK1P_218	G35	GTH
218	MGTHTXP1_218	J43	GTH
218	MGTHRXP1_218	F37	GTH
218	MGTHTXN1_218	J44	GTH
218	MGTHRXN1_218	F38	GTH
218	MGTHTXP0_218	K41	GTH
218	MGTHRXP0_218	G39	GTH
218	MGTHTXN0_218	K42	GTH
218	MGTHRXN0_218	G40	GTH
219	MGTHTXP3_219	B41	GTH
219	MGTHRXP3_219	A39	GTH
219	MGTHTXN3_219	B42	GTH
219	MGTHRXN3_219	A40	GTH
219	MGTHTXP2_219	C43	GTH
219	MGTHRXP2_219	B37	GTH
219	MGTHTXN2_219	C44	GTH
219	MGTREFCLK0P_219	A35	GTH
219	MGTHRXN2_219	B38	GTH
219	MGTREFCLK0N_219	A36	GTH

Bank	Pin name	Pin	I/O Type
219	MGTREFCLK1N_219	C36	GTH
219	MGTREFCLK1P_219	C35	GTH
219	MGTHTXP1_219	E43	GTH
219	MGTHRXP1_219	C39	GTH
219	MGTHTXN1_219	E44	GTH
219	MGTHRXN1_219	C40	GTH
219	MGTHTXP0_219	F41	GTH
219	MGTHRXP0_219	D41	GTH
219	MGTHTXN0_219	F42	GTH
219	MGTHRXN0_219	D42	GTH
NA	MGTAVCC_G10	AA8	NA
NA	MGTAVCC_G10	AC7	NA
NA	MGTAVCC_G10	AE8	NA
NA	MGTAVCC_G10	AG8	NA
NA	MGTAVCC_G10	AJ7	NA
NA	MGTAVCC_G10	R8	NA
NA	MGTAVCC_G10	U8	NA
NA	MGTAVCC_G10	W8	NA
NA	MGTAVCC_G10	Y10	NA
NA	MGTAVCC_G11	B10	NA
NA	MGTAVCC_G11	D10	NA
NA	MGTAVCC_G11	F10	NA
NA	MGTAVCC_G11	H10	NA
NA	MGTAVCC_G11	K10	NA
NA	MGTAVCC_G11	M10	NA
NA	MGTAVCC_G20	Y35	NA
NA	MGTAVCC_G20	AA37	NA
NA	MGTAVCC_G20	AC38	NA
NA	MGTAVCC_G20	AE37	NA
NA	MGTAVCC_G20	AG37	NA
NA	MGTAVCC_G20	AJ38	NA
NA	MGTAVCC_G20	R37	NA
NA	MGTAVCC_G20	U37	NA
NA	MGTAVCC_G20	W37	NA
NA	MGTAVCC_G21	B35	NA
NA	MGTAVCC_G21	D35	NA
NA	MGTAVCC_G21	F35	NA
NA	MGTAVCC_G21	H35	NA
NA	MGTAVCC_G21	K35	NA
NA	MGTAVCC_G21	M35	NA

Bank	Pin name	Pin	I/O Type
NA	MGTAVTT_G10	AB5	NA
NA	MGTAVTT_G10	AC3	NA
NA	MGTAVTT_G10	AD5	NA
NA	MGTAVTT_G10	AF5	NA
NA	MGTAVTT_G10	AG3	NA
NA	MGTAVTT_G10	AH5	NA
NA	MGTAVTT_G10	AJ3	NA
NA	MGTAVTT_G10	R3	NA
NA	MGTAVTT_G10	T5	NA
NA	MGTAVTT_G10	V5	NA
NA	MGTAVTT_G10	W3	NA
NA	MGTAVTT_G10	Y5	NA
NA	MGTAVTT_G11	B5	NA
NA	MGTAVTT_G11	C3	NA
NA	MGTAVTT_G11	D5	NA
NA	MGTAVTT_G11	F5	NA
NA	MGTAVTT_G11	G3	NA
NA	MGTAVTT_G11	H5	NA
NA	MGTAVTT_G11	K5	NA
NA	MGTAVTT_G11	L3	NA
NA	MGTAVTT_G11	M5	NA
NA	MGTAVTT_G11	P5	NA
NA	MGTAVTT_G20	AB40	NA
NA	MGTAVTT_G20	AC42	NA
NA	MGTAVTT_G20	AD40	NA
NA	MGTAVTT_G20	AF40	NA
NA	MGTAVTT_G20	AG42	NA
NA	MGTAVTT_G20	AH40	NA
NA	MGTAVTT_G20	AJ42	NA
NA	MGTAVTT_G20	R42	NA
NA	MGTAVTT_G20	T40	NA
NA	MGTAVTT_G20	V40	NA
NA	MGTAVTT_G20	W42	NA
NA	MGTAVTT_G20	Y40	NA
NA	MGTAVTT_G21	B40	NA
NA	MGTAVTT_G21	C42	NA
NA	MGTAVTT_G21	D40	NA
NA	MGTAVTT_G21	F40	NA
NA	MGTAVTT_G21	G42	NA
NA	MGTAVTT_G21	H40	NA

Bank	Pin name	Pin	I/O Type
NA	MGTAVTT_G21	K40	NA
NA	MGTAVTT_G21	L42	NA
NA	MGTAVTT_G21	M40	NA
NA	MGTAVTT_G21	P40	NA
NA	MGTAVCC_G9	AL8	NA
NA	MGTAVCC_G9	AN8	NA
NA	MGTAVCC_G9	AP10	NA
NA	MGTAVCC_G9	AR8	NA
NA	MGTAVCC_G9	AU8	NA
NA	MGTAVCC_G9	AW8	NA
NA	MGTAVCC_G9	BA8	NA
NA	MGTAVCC_G9	BC8	NA
NA	MGTAVCC_G19	AL37	NA
NA	MGTAVCC_G19	AN37	NA
NA	MGTAVCC_G19	AP35	NA
NA	MGTAVCC_G19	AR37	NA
NA	MGTAVCC_G19	AU37	NA
NA	MGTAVCC_G19	AW37	NA
NA	MGTAVCC_G19	BA37	NA
NA	MGTAVCC_G19	BC37	NA
NA	MGTAVTT_G9	AL3	NA
NA	MGTAVTT_G9	AM5	NA
NA	MGTAVTT_G9	AP5	NA
NA	MGTAVTT_G9	AR3	NA
NA	MGTAVTT_G9	AT5	NA
NA	MGTAVTT_G9	AV5	NA
NA	MGTAVTT_G9	AW3	NA
NA	MGTAVTT_G9	AY5	NA
NA	MGTAVTT_G9	BB5	NA
NA	MGTAVTT_G9	BC3	NA
NA	MGTAVTT_G19	AL42	NA
NA	MGTAVTT_G19	AM40	NA
NA	MGTAVTT_G19	AP40	NA
NA	MGTAVTT_G19	AR42	NA
NA	MGTAVTT_G19	AT40	NA
NA	MGTAVTT_G19	AV40	NA
NA	MGTAVTT_G19	AW42	NA
NA	MGTAVTT_G19	AY40	NA
NA	MGTAVTT_G19	BB40	NA
NA	MGTAVTT_G19	BC42	NA

Bank	Pin name	Pin	I/O Type
NA	MGTVCCAUX_G9	AM10	NA
NA	MGTVCCAUX_G19	AM35	NA
NA	MGTVCCAUX_G10	T10	NA
NA	MGTVCCAUX_G10	V10	NA
NA	MGTVCCAUX_G11	P10	NA
NA	MGTVCCAUX_G20	T35	NA
NA	MGTVCCAUX_G20	V35	NA
NA	MGTVCCAUX_G21	P35	NA
NA	GND	A11	NA
NA	GND	A12	NA
NA	GND	A22	NA
NA	GND	A3	NA
NA	GND	A32	NA
NA	GND	A34	NA
NA	GND	A37	NA
NA	GND	A38	NA
NA	GND	A4	NA
NA	GND	A41	NA
NA	GND	A42	NA
NA	GND	A7	NA
NA	GND	A8	NA
NA	GND	AA11	NA
NA	GND	AA12	NA
NA	GND	AA14	NA
NA	GND	AA16	NA
NA	GND	AA18	NA
NA	GND	AA20	NA
NA	GND	AA22	NA
NA	GND	AA24	NA
NA	GND	AA26	NA
NA	GND	AA28	NA
NA	GND	AA3	NA
NA	GND	AA30	NA
NA	GND	AA32	NA
NA	GND	AA34	NA
NA	GND	AA38	NA
NA	GND	AA4	NA
NA	GND	AA41	NA
NA	GND	AA42	NA
NA	GND	AA7	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AB1	NA
NA	GND	AB10	NA
NA	GND	AB11	NA
NA	GND	AB13	NA
NA	GND	AB15	NA
NA	GND	AB17	NA
NA	GND	AB19	NA
NA	GND	AB2	NA
NA	GND	AB21	NA
NA	GND	AB25	NA
NA	GND	AB27	NA
NA	GND	AB29	NA
NA	GND	AB31	NA
NA	GND	AB33	NA
NA	GND	AB34	NA
NA	GND	AB35	NA
NA	GND	AB36	NA
NA	GND	AB39	NA
NA	GND	AB43	NA
NA	GND	AB44	NA
NA	GND	AB6	NA
NA	GND	AB9	NA
NA	GND	AC11	NA
NA	GND	AC12	NA
NA	GND	AC14	NA
NA	GND	AC16	NA
NA	GND	AC18	NA
NA	GND	AC20	NA
NA	GND	AC24	NA
NA	GND	AC26	NA
NA	GND	AC28	NA
NA	GND	AC30	NA
NA	GND	AC32	NA
NA	GND	AC34	NA
NA	GND	AC37	NA
NA	GND	AC4	NA
NA	GND	AC41	NA
NA	GND	AC8	NA
NA	GND	AD1	NA
NA	GND	AD10	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AD11	NA
NA	GND	AD13	NA
NA	GND	AD15	NA
NA	GND	AD17	NA
NA	GND	AD19	NA
NA	GND	AD2	NA
NA	GND	AD21	NA
NA	GND	AD25	NA
NA	GND	AD27	NA
NA	GND	AD29	NA
NA	GND	AD31	NA
NA	GND	AD33	NA
NA	GND	AD34	NA
NA	GND	AD35	NA
NA	GND	AD36	NA
NA	GND	AD39	NA
NA	GND	AD43	NA
NA	GND	AD44	NA
NA	GND	AD6	NA
NA	GND	AD9	NA
NA	GND	AE14	NA
NA	GND	AE16	NA
NA	GND	AE18	NA
NA	GND	AE20	NA
NA	GND	AE24	NA
NA	GND	AE26	NA
NA	GND	AE28	NA
NA	GND	AE3	NA
NA	GND	AE30	NA
NA	GND	AE32	NA
NA	GND	AE36	NA
NA	GND	AE38	NA
NA	GND	AE4	NA
NA	GND	AE41	NA
NA	GND	AE42	NA
NA	GND	AE7	NA
NA	GND	AE9	NA
NA	GND	AF1	NA
NA	GND	AF11	NA
NA	GND	AF13	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AF15	NA
NA	GND	AF17	NA
NA	GND	AF19	NA
NA	GND	AF2	NA
NA	GND	AF21	NA
NA	GND	AF23	NA
NA	GND	AF25	NA
NA	GND	AF27	NA
NA	GND	AF29	NA
NA	GND	AF31	NA
NA	GND	AF33	NA
NA	GND	AF36	NA
NA	GND	AF39	NA
NA	GND	AF43	NA
NA	GND	AF44	NA
NA	GND	AF6	NA
NA	GND	AF9	NA
NA	GND	AG14	NA
NA	GND	AG16	NA
NA	GND	AG18	NA
NA	GND	AG20	NA
NA	GND	AG22	NA
NA	GND	AG24	NA
NA	GND	AG26	NA
NA	GND	AG28	NA
NA	GND	AG30	NA
NA	GND	AG32	NA
NA	GND	AG36	NA
NA	GND	AG38	NA
NA	GND	AG4	NA
NA	GND	AG41	NA
NA	GND	AG7	NA
NA	GND	AG9	NA
NA	GND	AH1	NA
NA	GND	AH10	NA
NA	GND	AH11	NA
NA	GND	AH13	NA
NA	GND	AH15	NA
NA	GND	AH17	NA
NA	GND	AH19	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AH2	NA
NA	GND	AH21	NA
NA	GND	AH23	NA
NA	GND	AH25	NA
NA	GND	AH27	NA
NA	GND	AH29	NA
NA	GND	AH31	NA
NA	GND	AH33	NA
NA	GND	AH34	NA
NA	GND	AH35	NA
NA	GND	AH36	NA
NA	GND	AH39	NA
NA	GND	AH43	NA
NA	GND	AH44	NA
NA	GND	AH6	NA
NA	GND	AH9	NA
NA	GND	AJ11	NA
NA	GND	AJ12	NA
NA	GND	AJ18	NA
NA	GND	AJ20	NA
NA	GND	AJ24	NA
NA	GND	AJ28	NA
NA	GND	AJ34	NA
NA	GND	AJ37	NA
NA	GND	AJ4	NA
NA	GND	AJ41	NA
NA	GND	AJ8	NA
NA	GND	AK1	NA
NA	GND	AK10	NA
NA	GND	AK15	NA
NA	GND	AK2	NA
NA	GND	AK25	NA
NA	GND	AK35	NA
NA	GND	AK36	NA
NA	GND	AK39	NA
NA	GND	AK40	NA
NA	GND	AK43	NA
NA	GND	AK44	NA
NA	GND	AK5	NA
NA	GND	AK6	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AK9	NA
NA	GND	AL11	NA
NA	GND	AL12	NA
NA	GND	AL22	NA
NA	GND	AL32	NA
NA	GND	AL34	NA
NA	GND	AL38	NA
NA	GND	AL4	NA
NA	GND	AL41	NA
NA	GND	AL7	NA
NA	GND	AM1	NA
NA	GND	AM11	NA
NA	GND	AM19	NA
NA	GND	AM2	NA
NA	GND	AM29	NA
NA	GND	AM34	NA
NA	GND	AM36	NA
NA	GND	AM39	NA
NA	GND	AM43	NA
NA	GND	AM44	NA
NA	GND	AM6	NA
NA	GND	AM9	NA
NA	GND	AN11	NA
NA	GND	AN16	NA
NA	GND	AN26	NA
NA	GND	AN3	NA
NA	GND	AN34	NA
NA	GND	AN38	NA
NA	GND	AN4	NA
NA	GND	AN41	NA
NA	GND	AN42	NA
NA	GND	AN7	NA
NA	GND	AP1	NA
NA	GND	AP11	NA
NA	GND	AP13	NA
NA	GND	AP2	NA
NA	GND	AP23	NA
NA	GND	AP33	NA
NA	GND	AP34	NA
NA	GND	AP36	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AP39	NA
NA	GND	AP43	NA
NA	GND	AP44	NA
NA	GND	AP6	NA
NA	GND	AP9	NA
NA	GND	AR11	NA
NA	GND	AR20	NA
NA	GND	AR30	NA
NA	GND	AR34	NA
NA	GND	AR38	NA
NA	GND	AR4	NA
NA	GND	AR41	NA
NA	GND	AR7	NA
NA	GND	AT1	NA
NA	GND	AT10	NA
NA	GND	AT11	NA
NA	GND	AT17	NA
NA	GND	AT2	NA
NA	GND	AT27	NA
NA	GND	AT34	NA
NA	GND	AT35	NA
NA	GND	AT36	NA
NA	GND	AT39	NA
NA	GND	AT43	NA
NA	GND	AT44	NA
NA	GND	AT6	NA
NA	GND	AT9	NA
NA	GND	AU14	NA
NA	GND	AU24	NA
NA	GND	AU3	NA
NA	GND	AU34	NA
NA	GND	AU36	NA
NA	GND	AU38	NA
NA	GND	AU4	NA
NA	GND	AU41	NA
NA	GND	AU42	NA
NA	GND	AU7	NA
NA	GND	AU9	NA
NA	GND	AV1	NA
NA	GND	AV11	NA

Bank	Pin name	Pin	I/O Type
NA	GND	AV2	NA
NA	GND	AV21	NA
NA	GND	AV31	NA
NA	GND	AV36	NA
NA	GND	AV39	NA
NA	GND	AV43	NA
NA	GND	AV44	NA
NA	GND	AV6	NA
NA	GND	AV9	NA
NA	GND	AW18	NA
NA	GND	AW28	NA
NA	GND	AW36	NA
NA	GND	AW38	NA
NA	GND	AW4	NA
NA	GND	AW41	NA
NA	GND	AW7	NA
NA	GND	AW9	NA
NA	GND	AY1	NA
NA	GND	AY15	NA
NA	GND	AY2	NA
NA	GND	AY25	NA
NA	GND	AY35	NA
NA	GND	AY36	NA
NA	GND	AY39	NA
NA	GND	AY43	NA
NA	GND	AY44	NA
NA	GND	AY6	NA
NA	GND	AY9	NA
NA	GND	B11	NA
NA	GND	B19	NA
NA	GND	B2	NA
NA	GND	B29	NA
NA	GND	B34	NA
NA	GND	B36	NA
NA	GND	B39	NA
NA	GND	B43	NA
NA	GND	B6	NA
NA	GND	B9	NA
NA	GND	BA12	NA
NA	GND	BA22	NA

Bank	Pin name	Pin	I/O Type
NA	GND	BA3	NA
NA	GND	BA32	NA
NA	GND	BA36	NA
NA	GND	BA38	NA
NA	GND	BA4	NA
NA	GND	BA41	NA
NA	GND	BA42	NA
NA	GND	BA7	NA
NA	GND	BA9	NA
NA	GND	BB1	NA
NA	GND	BB19	NA
NA	GND	BB2	NA
NA	GND	BB29	NA
NA	GND	BB36	NA
NA	GND	BB39	NA
NA	GND	BB43	NA
NA	GND	BB44	NA
NA	GND	BB6	NA
NA	GND	BB9	NA
NA	GND	BC16	NA
NA	GND	BC2	NA
NA	GND	BC26	NA
NA	GND	BC36	NA
NA	GND	BC38	NA
NA	GND	BC4	NA
NA	GND	BC41	NA
NA	GND	BC43	NA
NA	GND	BC7	NA
NA	GND	BC9	NA
NA	GND	BD13	NA
NA	GND	BD23	NA
NA	GND	BD33	NA
NA	GND	BD36	NA
NA	GND	BD39	NA
NA	GND	BD40	NA
NA	GND	BD5	NA
NA	GND	BD6	NA
NA	GND	BD9	NA
NA	GND	C11	NA
NA	GND	C16	NA

Bank	Pin name	Pin	I/O Type
NA	GND	C26	NA
NA	GND	C34	NA
NA	GND	C37	NA
NA	GND	C38	NA
NA	GND	C4	NA
NA	GND	C41	NA
NA	GND	C7	NA
NA	GND	C8	NA
NA	GND	D1	NA
NA	GND	D11	NA
NA	GND	D13	NA
NA	GND	D2	NA
NA	GND	D23	NA
NA	GND	D33	NA
NA	GND	D34	NA
NA	GND	D36	NA
NA	GND	D39	NA
NA	GND	D43	NA
NA	GND	D44	NA
NA	GND	D6	NA
NA	GND	D9	NA
NA	GND	E11	NA
NA	GND	E20	NA
NA	GND	E3	NA
NA	GND	E30	NA
NA	GND	E34	NA
NA	GND	E37	NA
NA	GND	E38	NA
NA	GND	E4	NA
NA	GND	E41	NA
NA	GND	E42	NA
NA	GND	E7	NA
NA	GND	E8	NA
NA	GND	F1	NA
NA	GND	F11	NA
NA	GND	F17	NA
NA	GND	F2	NA
NA	GND	F27	NA
NA	GND	F34	NA
NA	GND	F36	NA

Bank	Pin name	Pin	I/O Type
NA	GND	F39	NA
NA	GND	F43	NA
NA	GND	F44	NA
NA	GND	F6	NA
NA	GND	F9	NA
NA	GND	G11	NA
NA	GND	G14	NA
NA	GND	G24	NA
NA	GND	G34	NA
NA	GND	G37	NA
NA	GND	G38	NA
NA	GND	G4	NA
NA	GND	G41	NA
NA	GND	G7	NA
NA	GND	G8	NA
NA	GND	H1	NA
NA	GND	H11	NA
NA	GND	H2	NA
NA	GND	H21	NA
NA	GND	H31	NA
NA	GND	H34	NA
NA	GND	H36	NA
NA	GND	H39	NA
NA	GND	H43	NA
NA	GND	H44	NA
NA	GND	H6	NA
NA	GND	H9	NA
NA	GND	J11	NA
NA	GND	J18	NA
NA	GND	J28	NA
NA	GND	J3	NA
NA	GND	J34	NA
NA	GND	J37	NA
NA	GND	J38	NA
NA	GND	J4	NA
NA	GND	J41	NA
NA	GND	J42	NA
NA	GND	J7	NA
NA	GND	J8	NA
NA	GND	K1	NA

Bank	Pin name	Pin	I/O Type
NA	GND	K11	NA
NA	GND	K15	NA
NA	GND	K2	NA
NA	GND	K25	NA
NA	GND	K34	NA
NA	GND	K36	NA
NA	GND	K39	NA
NA	GND	K43	NA
NA	GND	K44	NA
NA	GND	K6	NA
NA	GND	K9	NA
NA	GND	L11	NA
NA	GND	L12	NA
NA	GND	L22	NA
NA	GND	L32	NA
NA	GND	L34	NA
NA	GND	L37	NA
NA	GND	L38	NA
NA	GND	L4	NA
NA	GND	L41	NA
NA	GND	L7	NA
NA	GND	L8	NA
NA	GND	M1	NA
NA	GND	M11	NA
NA	GND	M19	NA
NA	GND	M2	NA
NA	GND	M29	NA
NA	GND	M34	NA
NA	GND	M36	NA
NA	GND	M39	NA
NA	GND	M43	NA
NA	GND	M44	NA
NA	GND	M6	NA
NA	GND	M9	NA
NA	GND	N11	NA
NA	GND	N16	NA
NA	GND	N26	NA
NA	GND	N3	NA
NA	GND	N34	NA
NA	GND	N37	NA

Bank	Pin name	Pin	I/O Type
NA	GND	N38	NA
NA	GND	N4	NA
NA	GND	N41	NA
NA	GND	N42	NA
NA	GND	N7	NA
NA	GND	N8	NA
NA	GND	P1	NA
NA	GND	P11	NA
NA	GND	P13	NA
NA	GND	P2	NA
NA	GND	P23	NA
NA	GND	P33	NA
NA	GND	P34	NA
NA	GND	P36	NA
NA	GND	P39	NA
NA	GND	P43	NA
NA	GND	P44	NA
NA	GND	P6	NA
NA	GND	P9	NA
NA	GND	R11	NA
NA	GND	R20	NA
NA	GND	R30	NA
NA	GND	R34	NA
NA	GND	R38	NA
NA	GND	R4	NA
NA	GND	R41	NA
NA	GND	R7	NA
NA	GND	T1	NA
NA	GND	T11	NA
NA	GND	T17	NA
NA	GND	T2	NA
NA	GND	T27	NA
NA	GND	T34	NA
NA	GND	T36	NA
NA	GND	T39	NA
NA	GND	T43	NA
NA	GND	T44	NA
NA	GND	T6	NA
NA	GND	T9	NA
NA	GND	U11	NA

Bank	Pin name	Pin	I/O Type
NA	GND	U14	NA
NA	GND	U24	NA
NA	GND	U3	NA
NA	GND	U34	NA
NA	GND	U38	NA
NA	GND	U4	NA
NA	GND	U41	NA
NA	GND	U42	NA
NA	GND	U7	NA
NA	GND	V1	NA
NA	GND	V11	NA
NA	GND	V13	NA
NA	GND	V17	NA
NA	GND	V19	NA
NA	GND	V2	NA
NA	GND	V21	NA
NA	GND	V23	NA
NA	GND	V25	NA
NA	GND	V27	NA
NA	GND	V29	NA
NA	GND	V31	NA
NA	GND	V33	NA
NA	GND	V34	NA
NA	GND	V36	NA
NA	GND	V39	NA
NA	GND	V43	NA
NA	GND	V44	NA
NA	GND	V6	NA
NA	GND	V9	NA
NA	GND	W11	NA
NA	GND	W12	NA
NA	GND	W14	NA
NA	GND	W16	NA
NA	GND	W18	NA
NA	GND	W20	NA
NA	GND	W22	NA
NA	GND	W24	NA
NA	GND	W26	NA
NA	GND	W28	NA
NA	GND	W30	NA

Bank	Pin name	Pin	I/O Type
NA	GND	W32	NA
NA	GND	W34	NA
NA	GND	W38	NA
NA	GND	W4	NA
NA	GND	W41	NA
NA	GND	W7	NA
NA	GND	Y1	NA
NA	GND	Y11	NA
NA	GND	Y13	NA
NA	GND	Y15	NA
NA	GND	Y17	NA
NA	GND	Y19	NA
NA	GND	Y2	NA
NA	GND	Y21	NA
NA	GND	Y23	NA
NA	GND	Y25	NA
NA	GND	Y27	NA
NA	GND	Y29	NA
NA	GND	Y31	NA
NA	GND	Y33	NA
NA	GND	Y34	NA
NA	GND	Y36	NA
NA	GND	Y39	NA
NA	GND	Y43	NA
NA	GND	Y44	NA
NA	GND	Y6	NA
NA	GND	Y9	NA
NA	VCCINT	AA13	NA
NA	VCCINT	AA15	NA
NA	VCCINT	AA17	NA
NA	VCCINT	AA21	NA
NA	VCCINT	AA23	NA
NA	VCCINT	AA29	NA
NA	VCCINT	AA31	NA
NA	VCCINT	AA33	NA
NA	VCCINT	AB12	NA
NA	VCCINT	AB14	NA
NA	VCCINT	AB16	NA
NA	VCCINT	AB20	NA
NA	VCCINT	AB28	NA

Bank	Pin name	Pin	I/O Type
NA	VCCINT	AB30	NA
NA	VCCINT	AB32	NA
NA	VCCINT	AC13	NA
NA	VCCINT	AC15	NA
NA	VCCINT	AC17	NA
NA	VCCINT	AC21	NA
NA	VCCINT	AC29	NA
NA	VCCINT	AC31	NA
NA	VCCINT	AC33	NA
NA	VCCINT	AD12	NA
NA	VCCINT	AD14	NA
NA	VCCINT	AD16	NA
NA	VCCINT	AD20	NA
NA	VCCINT	AD28	NA
NA	VCCINT	AD30	NA
NA	VCCINT	AD32	NA
NA	VCCINT	AE13	NA
NA	VCCINT	AE15	NA
NA	VCCINT	AE17	NA
NA	VCCINT	AE21	NA
NA	VCCINT	AE29	NA
NA	VCCINT	AE31	NA
NA	VCCINT	AE33	NA
NA	VCCINT	AF12	NA
NA	VCCINT	AF14	NA
NA	VCCINT	AF16	NA
NA	VCCINT	AF20	NA
NA	VCCINT	AF22	NA
NA	VCCINT	AF28	NA
NA	VCCINT	AF30	NA
NA	VCCINT	AF32	NA
NA	VCCINT	AG13	NA
NA	VCCINT	AG15	NA
NA	VCCINT	AG17	NA
NA	VCCINT	AG21	NA
NA	VCCINT	AG23	NA
NA	VCCINT	AG29	NA
NA	VCCINT	AG31	NA
NA	VCCINT	AG33	NA
NA	VCCINT	AH12	NA

Bank	Pin name	Pin	I/O Type
NA	VCCINT	AH14	NA
NA	VCCINT	AH16	NA
NA	VCCINT	AH20	NA
NA	VCCINT	AH22	NA
NA	VCCINT	AH28	NA
NA	VCCINT	AH30	NA
NA	VCCINT	AH32	NA
NA	VCCINT	AJ15	NA
NA	VCCINT	AJ17	NA
NA	VCCINT	AJ33	NA
NA	VCCINT	V12	NA
NA	VCCINT	V14	NA
NA	VCCINT	V20	NA
NA	VCCINT	V22	NA
NA	VCCINT	V28	NA
NA	VCCINT	V30	NA
NA	VCCINT	V32	NA
NA	VCCINT	W13	NA
NA	VCCINT	W15	NA
NA	VCCINT	W17	NA
NA	VCCINT	W21	NA
NA	VCCINT	W23	NA
NA	VCCINT	W29	NA
NA	VCCINT	W31	NA
NA	VCCINT	W33	NA
NA	VCCINT	Y12	NA
NA	VCCINT	Y14	NA
NA	VCCINT	Y16	NA
NA	VCCINT	Y20	NA
NA	VCCINT	Y22	NA
NA	VCCINT	Y28	NA
NA	VCCINT	Y30	NA
NA	VCCINT	Y32	NA
NA	VCCAUX	AA27	NA
NA	VCCAUX	AB18	NA
NA	VCCAUX	AC27	NA
NA	VCCAUX	AD18	NA
NA	VCCAUX	AE27	NA
NA	VCCAUX	AF18	NA
NA	VCCAUX	AG27	NA

Bank	Pin name	Pin	I/O Type
NA	VCCAUX	AH18	NA
NA	VCCAUX	AJ27	NA
NA	VCCAUX	V18	NA
NA	VCCAUX	W27	NA
NA	VCCAUX	Y18	NA
NA	VCCAUX_IO_G3	AA19	NA
NA	VCCAUX_IO_G3	AC19	NA
NA	VCCAUX_IO_G3	W19	NA
NA	VCCAUX_IO_G2	AE19	NA
NA	VCCAUX_IO_G2	AG19	NA
NA	VCCAUX_IO_G2	AJ19	NA
NA	VCCAUX_IO_G1	AB26	NA
NA	VCCAUX_IO_G1	V26	NA
NA	VCCAUX_IO_G1	Y26	NA
NA	VCCAUX_IO_G0	AD26	NA
NA	VCCAUX_IO_G0	AF26	NA
NA	VCCAUX_IO_G0	AH26	NA
14	VCCO_14	AL27	NA
14	VCCO_14	AP28	NA
14	VCCO_14	AU29	NA
14	VCCO_14	AY30	NA
14	VCCO_14	BA27	NA
14	VCCO_14	BD28	NA
15	VCCO_15	AJ23	NA
15	VCCO_15	AM24	NA
15	VCCO_15	AR25	NA
15	VCCO_15	AV26	NA
15	VCCO_15	AW23	NA
15	VCCO_15	BB24	NA
16	VCCO_16	AK30	NA
16	VCCO_16	AN31	NA
16	VCCO_16	AT32	NA
16	VCCO_16	AW33	NA
16	VCCO_16	BB34	NA
16	VCCO_16	BC31	NA
17	VCCO_17	B24	NA
17	VCCO_17	E25	NA
17	VCCO_17	H26	NA
17	VCCO_17	J23	NA
17	VCCO_17	M24	NA

Bank	Pin name	Pin	I/O Type
17	VCCO_17	R25	NA
18	VCCO_18	C31	NA
18	VCCO_18	F32	NA
18	VCCO_18	J33	NA
18	VCCO_18	K30	NA
18	VCCO_18	N31	NA
18	VCCO_18	T32	NA
19	VCCO_19	A27	NA
19	VCCO_19	D28	NA
19	VCCO_19	G29	NA
19	VCCO_19	L27	NA
19	VCCO_19	P28	NA
19	VCCO_19	U29	NA
34	VCCO_34	AL17	NA
34	VCCO_34	AP18	NA
34	VCCO_34	AR15	NA
34	VCCO_34	AV16	NA
34	VCCO_34	BA17	NA
34	VCCO_34	BD18	NA
35	VCCO_35	AK20	NA
35	VCCO_35	AN21	NA
35	VCCO_35	AT22	NA
35	VCCO_35	AU19	NA
35	VCCO_35	AY20	NA
35	VCCO_35	BC21	NA
36	VCCO_36	AJ13	NA
36	VCCO_36	AM14	NA
36	VCCO_36	AT12	NA
36	VCCO_36	AW13	NA
36	VCCO_36	AY10	NA
36	VCCO_36	BB14	NA
36	VCCO_36	BC11	NA
37	VCCO_37	C21	NA
37	VCCO_37	F22	NA
37	VCCO_37	G19	NA
37	VCCO_37	K20	NA
37	VCCO_37	N21	NA
37	VCCO_37	T22	NA
37	VCCO_37	U19	NA
38	VCCO_38	B14	NA

Bank	Pin name	Pin	I/O Type
38	VCCO_38	E15	NA
38	VCCO_38	F12	NA
38	VCCO_38	J13	NA
38	VCCO_38	M14	NA
38	VCCO_38	T12	NA
39	VCCO_39	A17	NA
39	VCCO_39	D18	NA
39	VCCO_39	H16	NA
39	VCCO_39	L17	NA
39	VCCO_39	P18	NA
39	VCCO_39	R15	NA
39	VCCO_39	V16	NA
0	VCCO_0	AE12	NA
0	VCCO_0	AG12	NA
NA	VCCBRAM	AA25	NA
NA	VCCBRAM	AB24	NA
NA	VCCBRAM	AC25	NA
NA	VCCBRAM	AD24	NA
NA	VCCBRAM	AE25	NA
NA	VCCBRAM	AF24	NA
NA	VCCBRAM	AG25	NA
NA	VCCBRAM	AH24	NA
NA	VCCBRAM	V24	NA
NA	VCCBRAM	W25	NA
NA	VCCBRAM	Y24	NA
NA	NC	AJ9	NA
NA	NC	AJ10	NA
NA	NC	AJ35	NA
NA	NC	AJ36	NA

Service & Supply

Address： No.2, North Siyingmen Road, Donggaodi Street, Fengtai District, Beijing, P.R.China
Department： International Cooperation Department
Telephone： +86 (10) 68757343
Fax： +86 (10) 68757706
Post code： 100076