



DDR5 4800 / 5200 / 5600 / 6000 / 6400
32GB With 2Gbx8 ETT / 288 Pin SO-DIMM

NEO FORZA DDR5 16GB-4800 / 5200 / 5600 / 6000 / 6400
SO-DIMM

General Description

This chapter gives an overview of the 262-pin DDR5 small outline dual in-line memory modules product family and describes its main characteristics.

Features

1. 262-Pin SO-DIMM (Lead-Free) DDR5 SDRAM Memory Module.
2. Data transfer rates: PC5-38400 / 41600 / 44800 / 48000 / 51200.
3. Power supply: VDD: 1.067V ~ 1.166V.
4. DRAM organization: 2048Mb × 8.
5. 32 internal banks; 8 groups of 4 banks each.
6. 16-bit prefetch.
7. BL16, BC8 OTF, BL32, BL32 OTF supported.
8. DFE (Decision Feedback Equalization) for DQ.
9. On-Die ECC.
10. Same Bank Refresh.
11. On Die Termination(ODT) via Mode Register setting.
12. Connectivity Test (CT)

Ordering Information for Compliant Products

Part Number	Compliance Code	Number of Ranks	DRAM Organization	# of SDRAMs
MM5SBGF4PG-4800C-A00	32GB / PC5-38400 / 40-40-40	2	2Gb x8	16
MM5SBGF4PG-5200C-A00	32GB / PC5-41600 / 42-42-42	2	2Gb x8	16
MM5SBGF4PG-5600C-A00	32GB / PC5-44800 / 46-46-46	2	2Gb x8	16
MM5SBGF4PG-6000C-A00	32GB / PC5-48000 / 48-48-48	2	2Gb x8	16
MM5SBGF4PG-6400C-A00	32GB / PC5-51200 / 52-52-52	2	2Gb x8	16



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Pin Assignments

262-Pin DDR5 SO-DIMM							
Front Side		Back Side		Front Side		Back Side	
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vin_B ULK	2	H S A	67	V _{ss}	68	DQ21_ A
3	Vin_B ULK	4	H S C L	69	DQ22_ A	70	V _{ss}
5	RFU	6	H S D A	71	V _{ss}	72	DQ23_ A
7	PWR_ GO OD	8	PWR_EN	73	DQ24_ A	74	V _{ss}
9	V _{ss}	10	V S S	75	V _{ss}	76	DQ25_ A
11	DQ0_ A	12	D Q 1 - A	77	DQ26_ A	78	V _{ss}
13	V _{ss}	14	V S S	79	V _{ss}	80	DQ27_ A
15	DQ2_ A	16	D Q 3 - A	81	DQS3_ A_c	82	V _{ss}
17	V _{ss}	18	V S S	83	DQS3_ A_t	84	DM3_A _n
19	DM0_ A_n	20	DQS0_A_ _c	85	V _{ss}	86	V _{ss}
21	V _{ss}	22	DQS0_A_ _t	87	DQ28_ A	88	DQ29_ A
23	DQ4_ A	24	V S S	89	V _{ss}	90	V _{ss}
25	V _{ss}	26	D Q 5 - A	91	DQ30_ A	92	DQ31_ A
27	DQ6_ A	28	V S S	93	V _{ss}	94	V _{ss}
29	V _{ss}	30	D	95	CB0_	96	CB1_A



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			Q 7 - A		A		
31	DQ8_ A	32	V _{SS}	97	V _{SS}	98	V _{SS}
33	V _{SS}	34	DQ9_A	99	CB2_ A	10 0	DQS4_ A_c
35	DQ10_ A	36	V S S	101	V _{SS}	10 2	DQS4_ A_t
37	V _{SS}	38	DQ11_A	103	CB3_ A	10 4	V _{SS}
39	DQS1_ A_c	40	V S S	105	V _{SS}	10 6	CS0_A _n
41	DQS1_ A_t	42	DM1_A_n	107	CA0_ A	10 8	ALERT _n
43	V _{SS}	44	V S S	109	CA1_ A	11 0	CS1_A _n
45	DQ12_ A	46	DQ13_A	111	V _{SS}	11 2	V _{SS}
47	V _{SS}	48	V S S	113	CA2_ A	11 4	CA3_A
49	DQ14_ A	50	DQ15_A	115	CA4_ A	11 6	CA5_A
51	V _{SS}	52	V S S	117	V _{SS}	11 8	V _{SS}
53	DQ16_ A	54	DQ17_A	119	CA6_ A	12 0	CA7_A
55	V _{SS}	56	V S S	121	CA8_ A	12 2	CA9_A
57	DQ18_ A	58	DQ19_A	123	V _{SS}	12 4	V _{SS}
59	V _{SS}	60	V S S	125	CA10 _A	12 6	CA11_ A
61	DM2_ A_n	62	DQS2_A_ c	Key			
63	V _{SS}	64	DQS2_A_ t	127	CA12 _A	12 8	RFU
65	DQ20_ A	66	V S S	129	V _{SS}	13 0	V _{SS}



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Pin Assignments (Continued)

262-Pin DDR5 SO-DIMM							
Front Side		Back Side		Front Side		Back Side	
Pin	Symb ol	Pin	Symb ol	Pin	Symb ol	Pin	Symb ol
131	CK0_A_t	132	CK1_A_t	197	V _{SS}	198	DQ7_B
133	CK0_A_c	134	CK1_A_c	199	DQ8_B	200	V _{SS}
135	V _{SS}	136	V _{SS}	201	V _{SS}	202	DQ9_B
137	CK0_B_t	138	CK1_B_t	203	DQ10_B	204	V _{SS}
139	CK0_B_c	140	CK1_B_c	205	V _{SS}	206	DQ11_B
141	V _{SS}	142	V _{SS}	207	DQS1_B_c	208	V _{SS}
143	RFU	144	CA12_B	209	DQS1_B_t	210	DM1_B_n
145	CA11_B	146	CA10_B	211	V _{SS}	212	V _{SS}
147	V _{SS}	148	V _{SS}	213	DQ12_B	214	DQ13_B
149	CA9_B	150	CA8_B	215	V _{SS}	216	V _{SS}
151	CA7_B	152	CA6_B	217	DQ14_B	218	DQ15_B
153	V _{SS}	154	V _{SS}	219	V _{SS}	220	V _{SS}
155	CA5_B	156	CA4_B	221	DQ16_B	222	DQ17_B
157	CA3_B	158	CA2_B	223	V _{SS}	224	V _{SS}
159	V _{SS}	160	V _{SS}	225	DQ18_B	226	DQ19_B
161	CS0_B_n	162	CA1_B	227	V _{SS}	228	V _{SS}
163	RESE_T_n	164	CA0_B	229	DM2_B_n	230	DQS2_B_c
165	CS1_B_n	166	V _{SS}	231	V _{SS}	232	DQS2_B_t
167	V _{SS}	168	CB0_B	233	DQ20_B	234	V _{SS}
169	DQS4_B_c	170	V _{SS}	235	V _{SS}	236	DQ21_B
171	DQS4_B_t	172	CB1_B	237	DQ22_B	238	V _{SS}
173	V _{SS}	174	V _{SS}	239	V _{SS}	240	DQ23_B



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175	CB3_ B	176	CB2_B	241	DQ24_ B	242	Vss
177	Vss	178	Vss	243	Vss	244	DQ25_ B
179	DQ0_ B	180	DQ1_ B	245	DQ26_ B	246	Vss
181	Vss	182	Vss	247	Vss	248	DQ27_ B
183	DQ2_ B	184	DQ3_ B	249	DQS3_ B_c	250	Vss
185	Vss	186	Vss	251	DQS3_ B_t	252	DM3_ B_n
187	DM0_ B_n	188	DQS0_ B_c	253	Vss	254	Vss
189	Vss	190	DQS0_ B_t	255	DQ28_ B	256	DQ29_ B
191	DQ4_ B	192	Vss	257	VSS	258	Vss
193	Vss	194	DQ5_ B	259	DQ30_ B	260	DQ31_ B
195	DQ6_ B	196	Vss	261	Vss	262	Vss



Pin Descriptions

Symbol	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command / Address bus
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select
DQ0_A – DQ31_A, DQ0_B – DQ31_B,	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)

Symbol	Description
HSCL	SidebandBus clock
HSDA	SidebandBus data
HAS	SidebandBus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a known state
V _{in} _BULK	5V power input supply to the PMIC for analog circuits
V _{ss}	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

Note:

DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.

The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B



DIMM Voltage Requirements

Symbol	Parameter	Voltage Rating (V)			Maximum Expected Current (A)	Power State
		Min.	Typ.	Max.		
V _{IN_BULK}	Host Supply Voltage	4.25	5.0	5.5	2.5 / 2.0	Operational
SWA, SWB	PMIC Output Supply Voltage	-	1.1	-	6	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	12	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	2	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020	Operational

Note:

1. During first power on the input voltage supply must reach minimum 4.25V for PMIC to detect valid input supply.
2. The ramp up rate between 300 mV and 4.0V.
3. The ramp down rate between 4V and 300 mV.
4. The area under the curve above V_{IN_Bulk} = TBD V. V_{IN_Bulk_AC} spec must also be satisfied.
5. The minimum input current requirement is to deliver the maximum output current on V_{OUT_1.8V} and V_{OUT_1.0V} LDO plus the current.
6. V_{IN_Bulk} = 5.0V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR_EN signal is static.
7. V_{IN_Bulk} = 5.0V. Measured at room temperature. All output regulators and LDOs are on with 0 A output load.. VR_EN signal is static.
8. 20MHz bandwidth limited measurement for all voltage in the table.
9. Voltages are measured at the DIMM gold fingers and at PMIC output pins.
10. The SDRAM specification must be met and take precedence over this document.
11. Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances.
12. Typical voltage is platform dependent. This is a suggested value only.
13. Follow JEDEC specification.

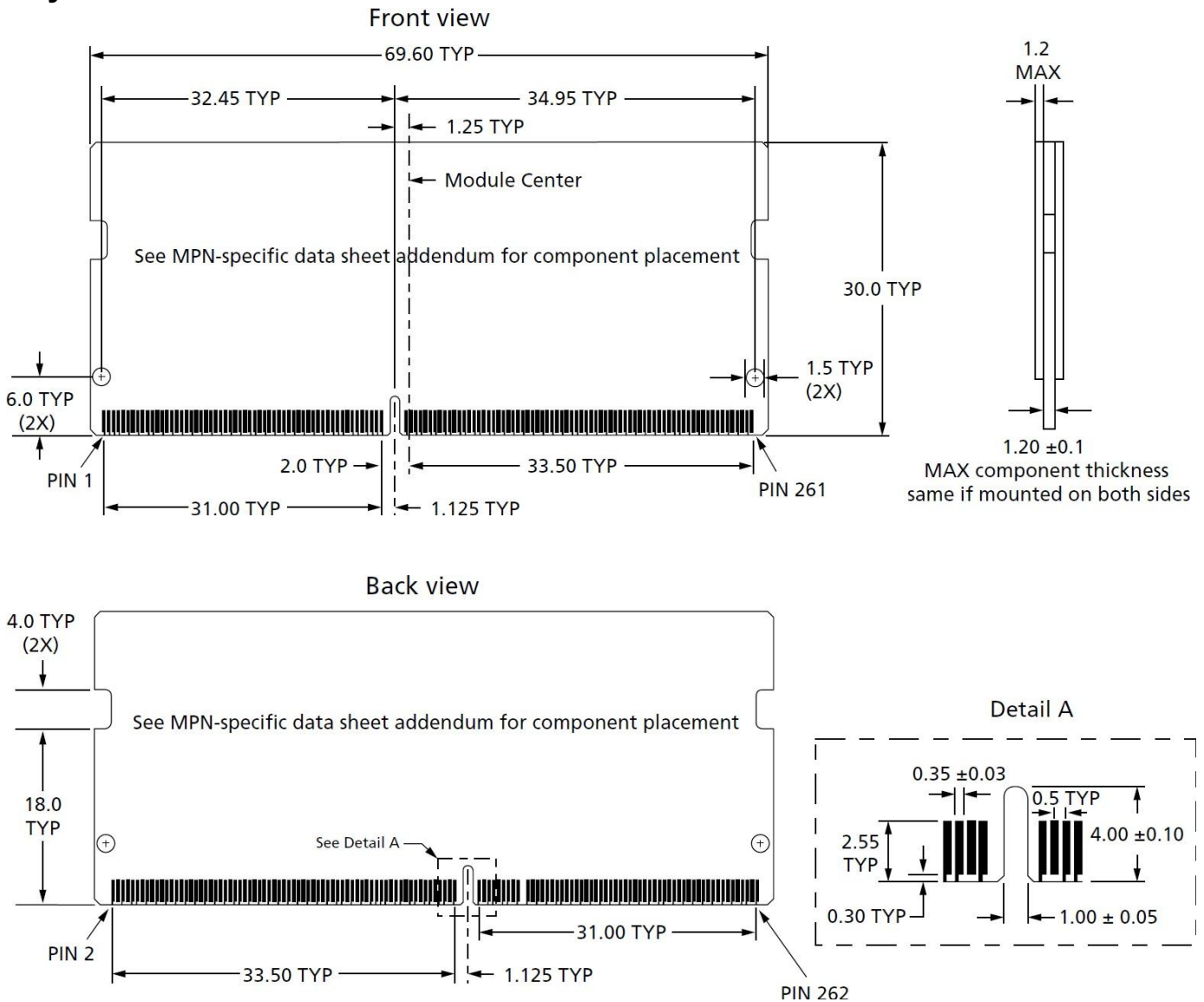
Recommended Operating Temperature Ranges

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,3

Note:

- The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer to JESD51-2.
- Normal is the maximum limit when device is operating in the Normal Temperature Mode.
- Extended is the maximum limit when device is operating in the Extended Temperature Mode.

Physical Dimensions



- Note: 1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
 2. Tolerance on all dimensions ±0.15 unless otherwise specified.
 3. The dimensional diagram is for reference only.



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Part Number Rule

① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪ ⑫ ⑬ ⑭ ⑮ ⑯ ⑰ ⑱ ⑲ ⑳

MM4U8GF3PG-2400C-A00

