SDR Series

CR-P159

User Manual

Version Records:

Data	Version	Description
2025.01.25	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

Content

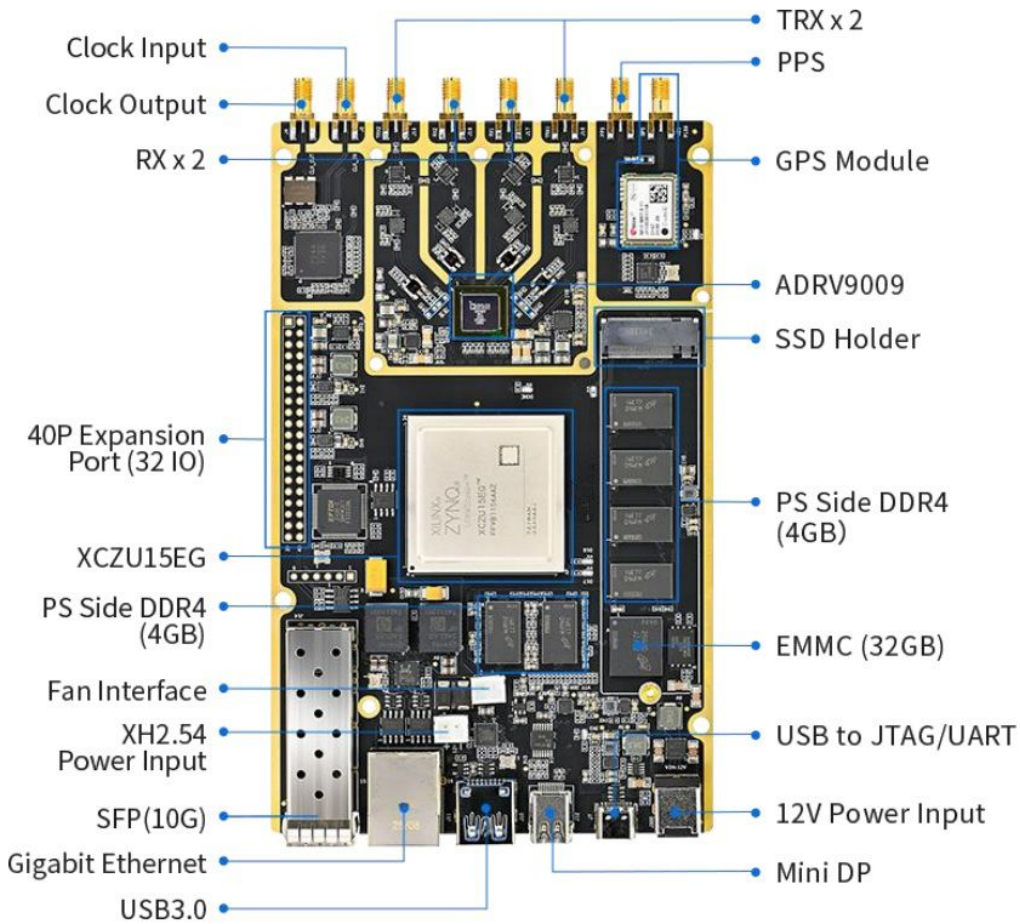
Part 1: Product Overview

Part 1.1: Product Overview

This article introduces the CR-P159, used AMD's the FPGA Chip XCZU15EG-2FFVB1156I from AMD as the main controller, equipped with ADI's ADRV9009BBCZ RF chip constitutes the main structure of the product. The CR-P159 integrates multiple RF and other hardware interfaces, which is rich in resources and easy to use. Refer to the picture below for details.

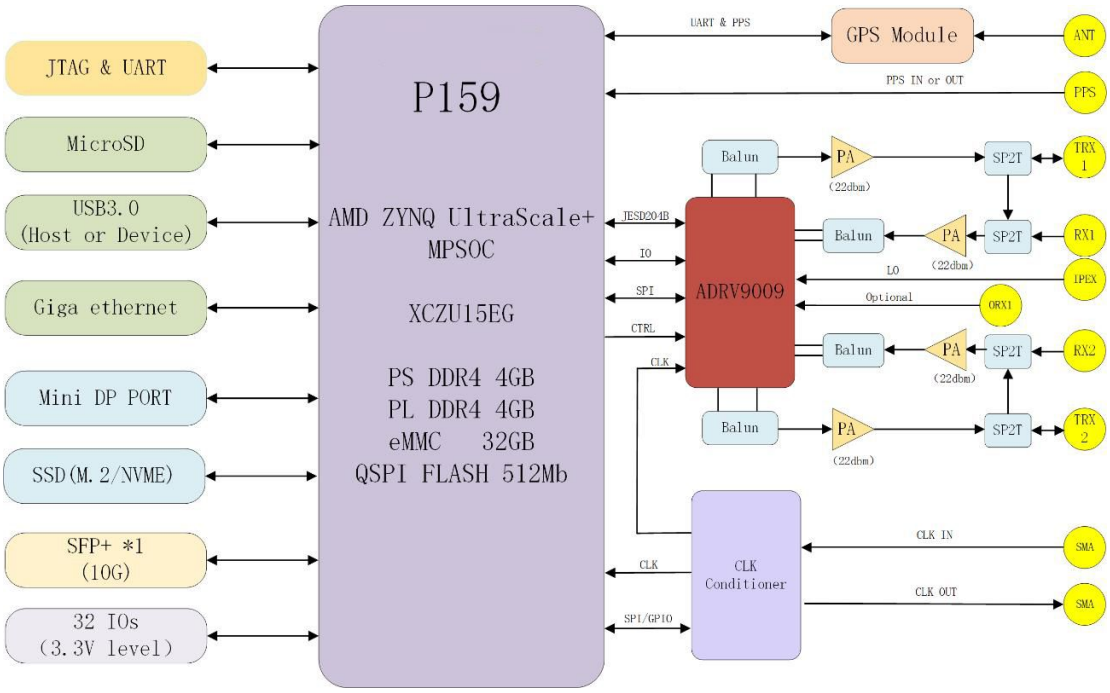
The CR-P159 PCBA Form Factors is 6.30 inch x3.94 inch (160 mm x 100mm). Several fixing holes are reserved on the PCB, which is convenient for users to integrate into the device directly. In addition, we have equipped the product with a beautiful shell, the whole shell plays the role of heat dissipation, to ensure the stable operation of the product.

The product is designed in accordance with industrial-grade standards, operating temperature -40℃-85 ℃, high-precision clock, all interfaces are made of static electricity protection.



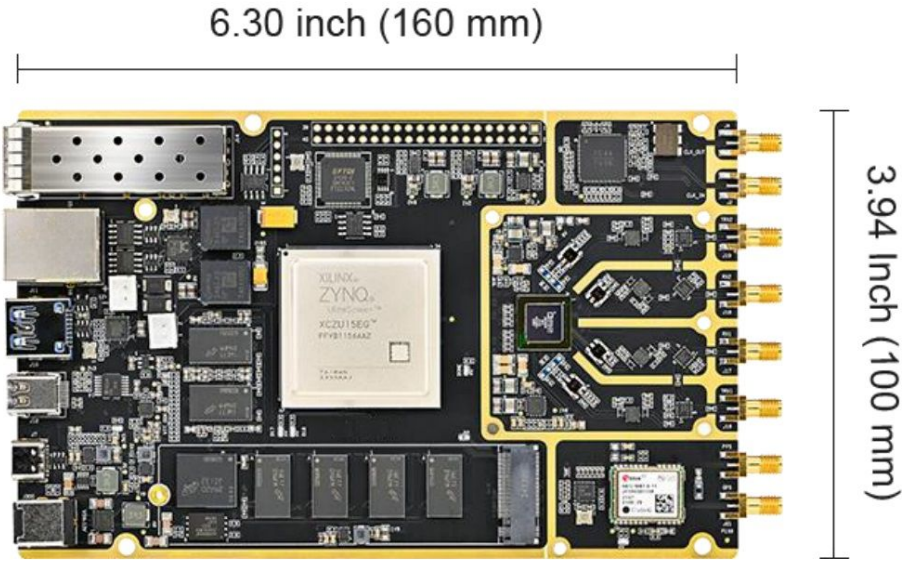
Part 1.2: Product Function Block Diagram

In this section, we will show the configuration details of the product in detail through the product block diagram and product specifications, as shown below.



Part 1.3: Form Factors

The form factors is 6.30 inch x3.94 inch (160 mm x 100mm)



Part 2: Hardware Introduction

Part 2.1: CR-P159 Introduction

The following table lists the parameters and peripheral interfaces of CR-P159. The board uses a single ADRV9009BBCZ to design 2T2R RF channels and multiple high-speed data transmission interfaces to complete the transceiver function of the entire RF link. Refer to the schematic for more details.

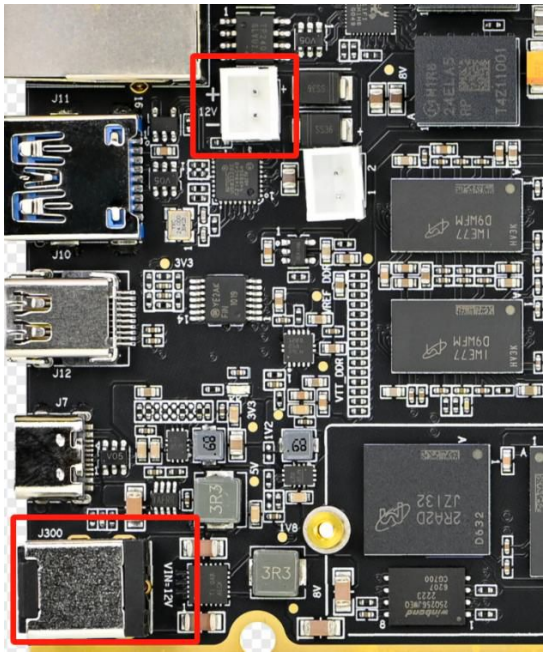
SDR Module	P159
RF Chip	ADRV9009BBCZ
Frequency Range	75MHz-6Ghz
Bit Width	ADC 16bit，DAC 14bit
Signal Bandwidths	TX 450Mhz,RX 200Mhz
Power Amplifier	TX and RX Support Full Bandwidth High Linearity 22dbm (Maximum Transmit Success Rate 25dbm)
FPGA Chip	XCZU15EG-2FFVB1156I
Processor Core	Quad-Core ARM Cortex-A53 (1.333Ghz) Dual-Core ARM Cortex-R5F(533Mhz)
DDR4	PS Side 4GB, PL Side4GB
QSPI FLASH	256Mb + 256Mb
EMMC	32GB
RF Clock	1 Output, 1 Input
USB3.0	1
Gigabit Ethernet	1
Mini DP	1
SSD(Nvme)	1
UART	1
JTAG	1
SD Card Slot	1
GPS	1
Expansion Port IOs	32 IOs
Power Supply	12V/ 3A
Working Temperature	-40°C ~ +85°C
Form Factors	6.30 inch x3.94 inch (160 mm x 100mm)

Part 2.2: About Power Supply

The product provides two kinds of power supply mode: XH2.54 interface, DC-007B interface, two kinds of power supply mode for customers to choose to use in different use mode.

XH2.54: If the product is integrated into the device, it can be powered through the XH2.54 interface, the power supply voltage range is 12V/3A.

DC-007B: This interface can be connected to the 12V/3A power adapter to supply power to the device, plug and play. DC-007B is connected to XH2.54, and only one of the two can be connected to prevent the two power supplies from affecting each other.



Part 2.3: System Clock

The CR-P159 board is designed with multiple clocks to meet different functions, refer to the schematic for more details.

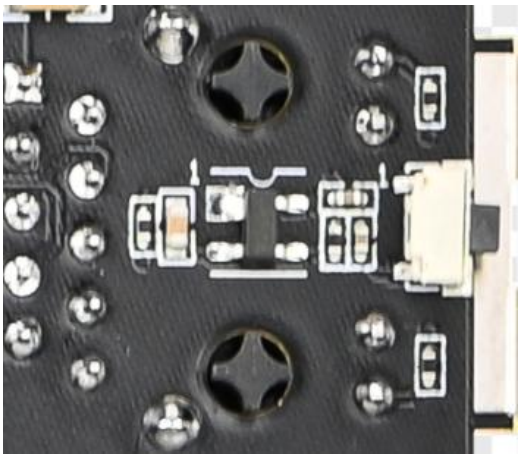
1) A **33.33Mhz** clock input is designed for the PS side, the input pin location is **PS_REF_CLK**, This clock provides a clock source for the ARM side, the pin location is **U24**.
2) Provide **200Mhz** clock for **PL** side, the input pin position is **IO_L13P_GC_66** and **IO_L13N_GC_66**, this clock provides clock source for PL side, the pin position is **Y4/Y3**.
3) Two clocks are provided for MGT, **125Mhz** and **156.25Mhz** respectively, the clock input pin correspondence is **125Mhz** connects to **MGT_REF_CLK_P0_230** and **MGT_REF_CLK_N0_230**, pin position is **C8/C7**; **156.25Mhz** connects to **MGT_REF_CLK_P1_230** and **MGT_REF_CLK_N1_230**, pin position is **B10/B9**.
4) **26Mhz/27Mhz/100hz** are provided for the **GTR** part for the three peripheral interfaces

USB3.0/ Mini DP / SSD respectively.

5) For the RF circuit provides a special clock chip **HMC7044LP10BE**, the output of multiple clocks, provided to the **JESD204B** interface to use. Clock corresponding to the interface can refer to our drawings.

Part 2.4: Reset KEY

The CR-P159 board provides an **nGST** reset KEY near the board edge for a system reset KEY, active low. This pin is connected to the PS_POR_B (V23) on the PS side and the IO_12P_44 (AE15) pin on the PL side, respectively.

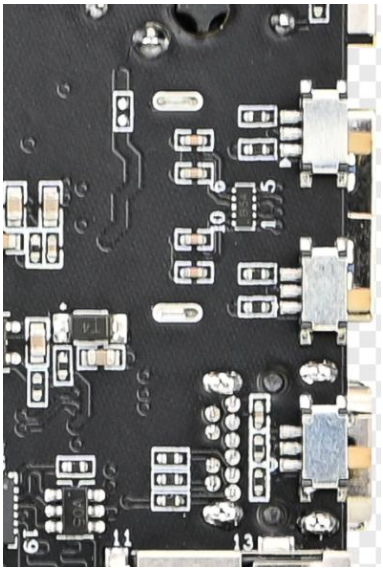


Part 2.5: Boot Mode Selection

The CR-P159 supports four boot modes, namely JTAG, QSPI Flash, EMMC, and SD card. Four startup methods can be selected through the onboard DIP switch. The following figure has listed the position of each mode DIP switch.

The switching of the startup mode can be selected by the DIP switch on the side of the CR-P159, the following figure shows the three toggle switches M2/M1/M0, which can be used to select the corresponding startup mode according to the startup truth table, and the M3 has been fixed to 0.

Boot Mode	Mode Pins [3:0]	Pin Location	CSU Mode	Description
PS JTAG	0000	JTAG	Slave	PSJTAG interface, PS dedicated pins.
Quad-SPI (24b)	0001	MIO[12:0]	Master	24-bit addressing (QSPI24).
Quad-SPI (32b)	0010	MIO[12:0]	Master	32-bit addressing (QSPI32).
SD0 (2.0)	0011	MIO[25:21, 16:13]	Master	SD 2.0.
NAND	0100	MIO[25:09]	Master	Requires 8-bit data bus width.
SD1 (2.0)	0101	MIO[51:43]	Master	SD 2.0.
eMMC (1.8V)	0110	MIO[22:13]	Master	eMMC version 4.5 at 1.8V.
USB0 (2.0)	0111	MIO[52:63]	Slave	USB 2.0 only.
PJTAG (MIO #0)	1000	MIO[29:26]	Slave	PJTAG connection 0 option.
PJTAG (MIO #1)	1001	MIO[15:12]	Slave	PJTAG connection 1 option.
SD1 LS (3.0)	1110	MIO[51:39]	Master	SD 3.0 with a required SD 3.0 compliant voltage level shifter.



Part 2.6: DDR4

PS side is designed with four industrial grade DDR4 chips, single capacity 1GB, four total capacity 4GB, PL side is also designed with four industrial grade DDR4 chips, single capacity 1GB, four total capacity 4GB. The DDR4 part number is MT40A512M16LY-062E IT:E, it is an industrial grade chip.

PS side DDR4 pin assignment directly call the system to assign it, PL side DDR4 pin assignment can refer to the following table, you can also refer to the routine provided by our company. PL side DDR4 pin assignment can refer to the following table, also can refer to the routine provided by our company.

DDR4 Pin	Pin Name	Pin Position
DDR4_DQ0	IO_L17N_64	AN4
DDR4_DQ1	IO_L17P_64	AM4
DDR4_DQ2	IO_L15P_64	AP5
DDR4_DQ3	IO_L14N_64	AM5
DDR4_DQ4	IO_L14P_64	AM6
DDR4_DQ5	IO_L18N_64	AK4
DDR4_DQ6	IO_L15N_64	AP4
DDR4_DQ7	IO_L18P_64	AK5
DDR4_DM0	IO_L13P_64	AL6
DDR4_DQS_P0	IO_L16P_64	AN6
DDR4_DQS_N0	IO_L16N_64	AP6
DDR4_DQ8	IO_L21N_64	AN1
DDR4_DQ9	IO_L23P_64	AK1
DDR4_DQ10	IO_L21P_64	AM1
DDR4_DQ11	IO_L24N_64	AK2

DDR4_DQ12	IO_L20N_64	AP3
DDR4_DQ13	IO_L24P_64	AK3
DDR4_DQ14	IO_L20P_64	AN3
DDR4_DQ15	IO_L23N_64	AL1
DDR4_DM1	IO_L19P_64	AN2
DDR4_DQS_P1	IO_L22P_64	AL3
DDR4_DQS_N1	IO_L22N_64	AL2
DDR4_DQ16	IO_L6N_64	AK10
DDR4_DQ17	IO_L3N_64	AM10
DDR4_DQ18	IO_L5P_64	AN9
DDR4_DQ19	IO_L2N_64	AM11
DDR4_DQ20	IO_L6P_64	AJ10
DDR4_DQ21	IO_L2P_64	AL11
DDR4_DQ22	IO_L5N_64	AP9
DDR4_DQ23	IO_L3P_64	AL10
DDR4_DM2	IO_L1P_64	AJ12
DDR4_DQS_P2	IO_L4P_64	AP11
DDR4_DQS_N2	IO_L4N_64	AP10
DDR4_DQ24	IO_L9P_64	AJ9
DDR4_DQ25	IO_L12P_64	AL8
DDR4_DQ26	IO_L11P_64	AK8
DDR4_DQ27	IO_L8P_64	AM9
DDR4_DQ28	IO_L11N_64	AK7
DDR4_DQ29	IO_L9N_64	AK9
DDR4_DQ30	IO_L12N_64	AL7
DDR4_DQ31	IO_L8N_64	AM8
DDR4_DM3	IO_L7P_64	AN8
DDR4_DQS_P3	IO_L10P_64	AN7
DDR4_DQS_N3	IO_L10N_64	AP7
DDR4_DQ32	IO_L15P_65	AH4
DDR4_DQ33	IO_L17P_65	AE3
DDR4_DQ34	IO_L14P_65	AG5
DDR4_DQ35	IO_L17N_65	AF3
DDR4_DQ36	IO_L15N_65	AJ4
DDR4_DQ37	IO_L18N_65	AE4
DDR4_DQ38	IO_L14N_65	AG4
DDR4_DQ39	IO_L18P_65	AD4
DDR4_DM4	IO_L13P_65	AE5
DDR4_DQS_P4	IO_L16P_65	AJ6
DDR4_DQS_N4	IO_L16N_65	AJ5
DDR4_DQ40	IO_L11N_65	AG6
DDR4_DQ41	IO_L12P_65	AE7

DDR4_DQ42	IO_L12N_65	AF7
DDR4_DQ43	IO_L9N_65	AD6
DDR4_DQ44	IO_L8N_65	AH8
DDR4_DQ45	IO_L9P_65	AD7
DDR4_DQ46	IO_L8P_65	AG8
DDR4_DQ47	IO_L11P_65	AF6
DDR4_DM5	IO_L7P_65	AH7
DDR4_DQS_P5	IO_L10P_65	AE8
DDR4_DQS_N5	IO_L10N_65	AF8
DDR4_DQ48	IO_L3N_65	AF12
DDR4_DQ49	IO_L5P_65	AG10
DDR4_DQ50	IO_L6P_65	AD10
DDR4_DQ51	IO_L5N_65	AG9
DDR4_DQ52	IO_L3P_65	AE12
DDR4_DQ53	IO_L2P_65	AH12
DDR4_DQ54	IO_L6N_65	AE9
DDR4_DQ55	IO_L2N_65	AH11
DDR4_DM6	IO_L1P_65	AE10
DDR4_DQS_P6	IO_L4P_65	AF11
DDR4_DQS_N6	IO_L4N_65	AG11
DDR4_DQ56	IO_L23N_65	AD1
DDR4_DQ57	IO_L20N_65	AH3
DDR4_DQ58	IO_L24N_65	AE1
DDR4_DQ59	IO_L21P_65	AF2
DDR4_DQ60	IO_L23P_65	AD2
DDR4_DQ61	IO_L20P_65	AG3
DDR4_DQ62	IO_L24P_65	AE2
DDR4_DQ63	IO_L21N_65	AF1
DDR4_DM7	IO_L19P_65	AH2
DDR4_DQS_P7	IO_L22P_65	AH1
DDR4_DQS_N7	IO_L22N_65	AJ1
DDR4_A0	IO_L15P_66	W5
DDR4_A1	IO_L20P_66	AB3
DDR4_A2	IO_L16N_66	AC4
DDR4_A3	IO_L17P_66	V4
DDR4_A4	IO_L15N_66	W4
DDR4_A5	IO_L21N_66	AA1
DDR4_A6	IO_L18P_66	U5
DDR4_A7	IO_L17N_66	V3
DDR4_A8	IO_L21P_66	AA2
DDR4_A9	IO_L19P_66	AC2
DDR4_A10	IO_L11N_66	Y7

DDR4_A11	IO_L22P_66	Y2
DDR4_A12	IO_L8P_66	AB8
DDR4_A13	IO_L23P_66	V2
DDR4_A14	IO_L10P_66	AB6
DDR4_A15	IO_L10N_66	AB5
DDR4_A16	IO_L7N_66	AC6
DDR4_A17	IO_L20N_66	AC3
DDR4_BA0	IO_L9N_66	W6
DDR4_BA1	IO_L12N_66	AA6
DDR4_BG0	IO_L16P_66	AB4
DDR4_nCS	IO_L11P_66	Y8
DDR4_ODT	IO_L8N_66	AC8
DDR4_nRESET	IO_L9P_66	W7
DDR4_CLK_P	IO_L14P_66	Y5
DDR4_CLK_N	IO_L14N_66	AA5
DDR4_CKE	IO_L6P_66	Y10
DDR4_nACT	IO_L12P_66	AA7
DDR4_nALERT	IO_L22N_66	Y1
DDR4_PARITY	IO_L19N_66	AC1

Part 2.7: EMMC Pin Definition

The CR-P159 is designed with a 32GB EMMC for storing boot and user files. The pin definitions are listed in the table below.

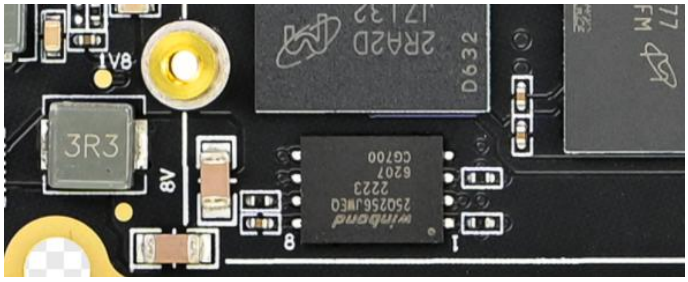
EMMC Pin	Pin Name	Pin Position
EMMC_D0	MIO13	AK17
EMMC_D1	MIO14	AL16
EMMC_D2	MIO15	AN16
EMMC_D3	MIO16	AM16
EMMC_D4	MIO17	AP16
EMMC_D5	MIO18	AE18
EMMC_D6	MIO19	AL17
EMMC_D7	MIO20	AD18
EMMC_CLK	MIO22	AD20
EMMC_CMD	MIO21	AF18
EMMC_nRST	MIO23	AD19

Part 2.8: QSPI FLASH Introduction

The CR-P159 is designed with two 256Mb QSPI FLASHs, totally 512Mb in x8 mode. It can be used to store startup files and user files. The pin definitions are listed in the table below.

QSPI0 FLASH	Pin Name	Pin Position
QSPI0_DQ0	MIO2	AH16
QSPI0_DQ1	MIO3	AJ16
QSPI0_DQ2	MIO4	AD16
QSPI0_DQ3	MIO5	AG16
QSPI0_CS	MIO1	AM15
QSPI0_CLK	MIO6	AF16

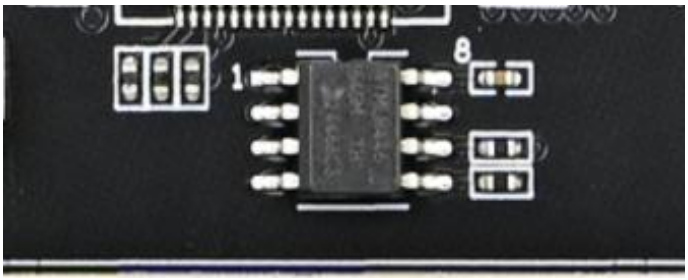
QSPI1 FLASH	Pin Name	Pin Position
QSPI1_DQ0	MIO2	AE17
QSPI1_DQ1	MIO3	AP15
QSPI1_DQ2	MIO4	AH17
QSPI1_DQ3	MIO5	AF17
QSPI1_CS	MIO1	AD17
QSPI1_CLK	MIO6	AJ17



Part 2.9: E2PROM Introduction

The CR-P159 is designed with E2PROM , Capacity is 256Kb. The pin definitions are listed in the table below.

E2PROM Pin	Pin Name	Pin Position
E2PROM_I2C_SCL	IO_L8N_HDGC_50	G13
E2PROM_I2C_SDA	IO_L9N_50	G14

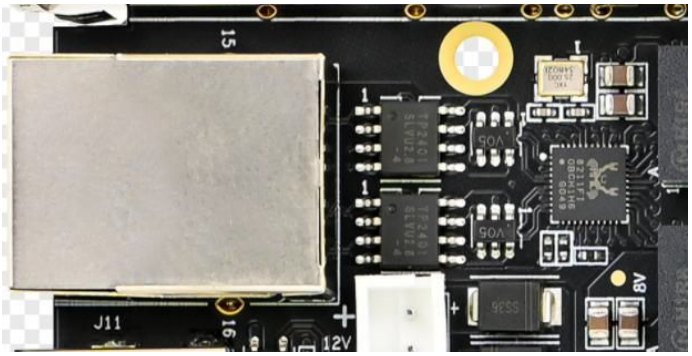


Part 2.10: Gigabit Ethernet

The CR-P159 is designed with one Gigabit Ethernet on the PS Side. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface, connecting the corresponding pins as shown in the following table Chip address PHY_AD[2:0]=010.

RMGII Signal	Pin Name	Pin Position
GPHY_GTX_CLK	MIO26_501	P21
GPHY_TXD0	MIO27_501	M21
GPHY_TXD1	MIO28_501	N21
GPHY_TXD2	MIO29_501	K22
GPHY_TXD3	MIO30_501	L21
GPHY_TX_EN	MIO31_501	J22
GPHY_RX_CLK	MIO32_501	H22
GPHY_RXD0	MIO33_501	H23

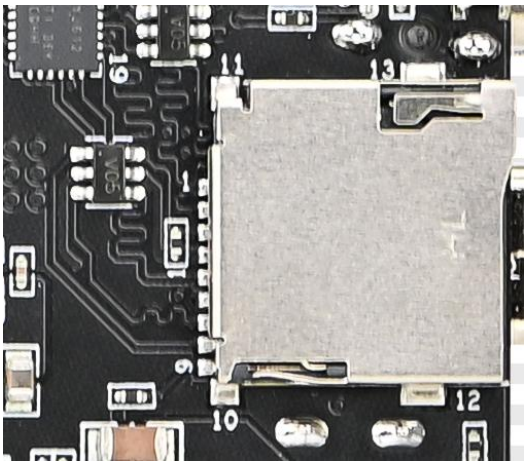
GPHY_RXD1	MIO34_501	L22
GPHY_RXD2	MIO35_501	P22
GPHY_RXD3	MIO36_501	K23
GPHY_RX_DV	MIO37_501	N22
GPHY_MDC	MIO76_502	H25
GPHY_MDIO	MIO77_502	F25



Part 2.11: SD Card Slot Interface

The SD card holder is placed on the board, which is connected to the BANK501 on the PS side of ZYNQ, because the level of BANK501 is 1.8V, but the data level of SD is 3.3V, We use the TXS02612RTWR for level shifting. The following is the pin assignment and schematic diagram of SD card interface, details refer to the schematic.

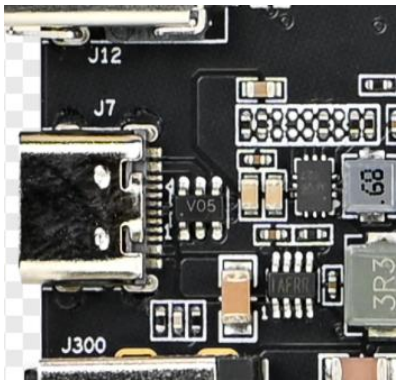
SD Card Slot	Pin Name	Pin Position
SD_CLK	MIO51	N25
SD_CMD	MIO50	P25
SD_DATA0	MIO46	J25
SD_DATA1	MIO47	L25
SD_DATA2	MIO48	M25
SD_DATA3	MIO49	K25



Part 2.12: USB to JTAG and UART Card

The CR-P159 is designed with a USB to JTAG/UART interface, the JTAG is connected to the JTAG interface of the FPGA, and the UART is connected to the UART0 pin of the FPGA. The following is the UART0 pin assignment, more details refer to the schematic.

UART0	Pin Name	Pin Position
UART0_TX	MIO43	K24
UART0_RX	MIO42	M24

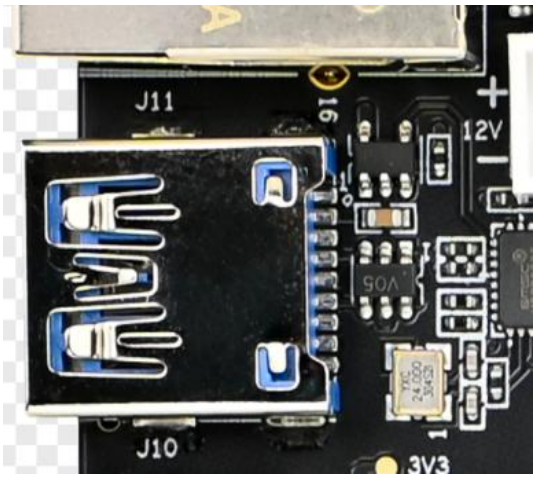


Part 2.13: USB3.0 Interface

The **CR-P159** is designed with a **USB3.0** interface, the interface type is Type-A, which can be flexibly defined as Host mode or Device mode, the following table lists the correspondence between the USB PHY and the host chip. For more details, please refer to the schematic diagram of the base board.

USB Signal	Pin Name	Pin Position
USBPHY_DATA0	MIO56	C23
USBPHY_DATA1	MIO57	A23

USBPHY_DATA2	MIO54	F23
USBPHY_DATA3	MIO59	B24
USBPHY_DATA4	MIO60	E24
USBPHY_DATA5	MIO61	C24
USBPHY_DATA6	MIO62	G24
USBPHY_DATA7	MIO63	D24
USBPHY_STP	MIO58	G23
USBPHY_NXT	MIO55	B23
USBPHY_DIR	MIO53	E23
USBPHY_CLKOUT	MIO52	F22
USB_nRSET	MIO64	A25
GT2_USB3_SSTXP	PS_MGTRTXP2_505	W31
GT2_USB3_SSTXN	PS_MGTRTXN2_505	W32
GT2_USB3_SSRXP	PS_MGTRRXP2_505	Y33
GT2_USB3_SSRXN	PS_MGTRRXN2_505	Y34
CLK_FPGA_26M_P	MGT_505_TX_P2	U27
CLK_FPGA_26M_N	MGT_505_TX_N2	U28

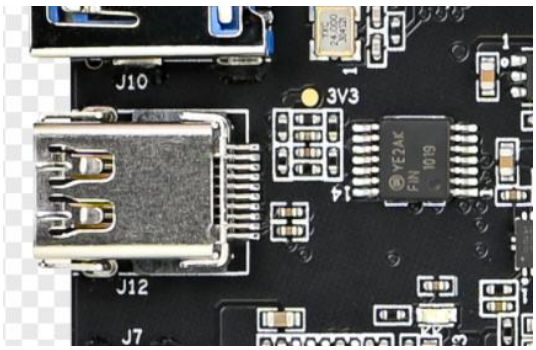


Part 2.14: Mini DP Interface

The **CR-P159** is designed with a **Mini DP** output interface, the interface signal is connected to the **BANK50/BANK505** of the FPGA. The following is the pin assignment of Mini DP, for more details refer to the schematic.

Mini DP Pin	Pin Name	Pin Position
GT3_DP_LINE_P0	MGT_505_TX_P3	V29
GT3_DP_LINE_N0	MGT_505_TX_N3	V30
DP_HPD	IO_L7P_HDGC_50	J12
DP_AUX_OUT	IO_L12N_50	J15
DP_OE	IO_L10P_50	J14
DP_AUX_IN	IO_L12P_50	J16

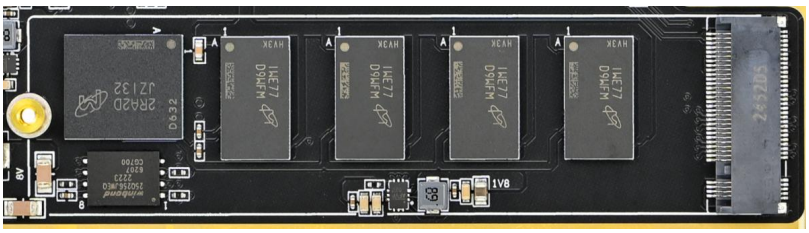
DP_CLK_P_27M	MGT_505_CLK_P2	U31
DP_CLK_N_27M	MGT_505_CLK_N2	U32



Part 2.15: SSD Interface

The **CR-P159** is designed with a SSD (x2 Mode) on the PS Side, the interface type is M.2, comply with NVME Protocol. The following is the pin assignment of SSD Interface, for more details refer to the schematic.

SSD Interface	Pin Name	Pin Position
SSD_nRST	MIO70	C26
CLK_FPGA_100M_P	MGT_505_CLK_P0	AA27
CLK_FPGA_100M_N	MGT_505_CLK_N0	AA28
GT0_SSD_TX_P0	MGT_505_TX_P0	AB29
GT0_SSD_TX_N0	MGT_505_TX_N0	AB30
GT0_SSD_RX_P0	MGT_505_RX_P0	AB33
GT0_SSD_RX_N0	MGT_505_RX_N0	AB34
GT0_SSD_TX_P1	MGT_505_TX_P1	Y29
GT0_SSD_TX_N1	MGT_505_TX_N1	Y30
GT0_SSD_RX_P1	MGT_505_RX_P1	AA31
GT0_SSD_RX_N1	MGT_505_RX_N1	AA32

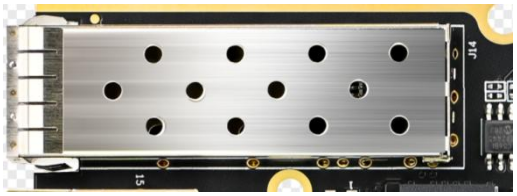


Part 2.16: SFP Interface

The **CR-P159** is designed with one 10G SFP Interface, the interface is connected with BANK230 of MPSOC. The following is the pin assignment of SFP Interface, for more details

refer to the schematic.

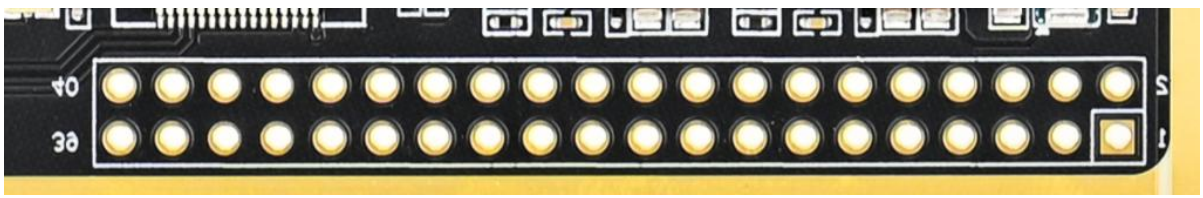
QSFP1 Pin	Pin Name	Pin Position
SFP1-TX-P	MGT_TX_P2_230	B6
SFP1-TX-N	MGT_TX_N2_230	B5
SFP1-RX-P	MGT_TX_P2_230	B2
SFP1-RX-N	MGT_TX_N2_230	B1



Part 2.17: 40P 2.54mm Expansion Port

The **CR-P159** is designed with one 40P 2.54mm pitch simple horn sockets, which are used to expand the signal connection. The signals are connected to BANK49/50 of the FPGA at a level of 3.3 V. The table below identifies the chip locations where the signals are located. For the detailed connection relationship, please refer to the schematic diagram.

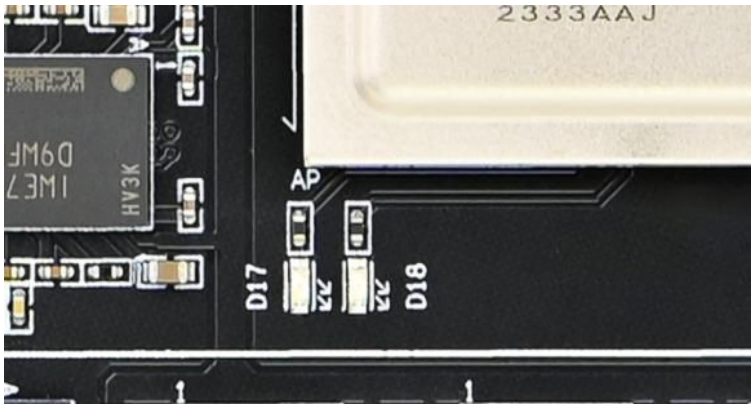
JM1 Signal Sequence	Pin Name	Pin Position	JM1 Signal Sequence	Pin Name	Pin Position
7	IO_L3N_49	A16	8	IO_L1N_49	F15
9	IO_L4P_49	B15	10	IO_L2P_49	D16
11	IO_L4N_49	A15	12	IO_L2N_49	C16
13	IO_L7P_49	C14	14	IO_L5P_49	E15
15	IO_L7N_49	B14	16	IO_L5N_49	D15
17	IO_L8P_49	C13	18	IO_L6P_49	E14
19	IO_L8N_49	B13	20	IO_L6N_49	D14
21	IO_L10P_49	C12	22	IO_L12P_49	F13
23	IO_L10N_49	B12	24	IO_L12N_49	E13
25	IO_L1P_50	J11	26	IO_L9P_49	A13
27	IO_L1N_50	J10	28	IO_L9N_49	A12
29	IO_L3P_50	F10	30	IO_L11P_49	E12
31	IO_L3N_50	E10	32	IO_L11N_49	D12
37	IO_L2P_50	H10	38	IO_L4P_50	D11
39	IO_L2N_50	G10	40	IO_L4N_50	D10



Part 2.18: LED Indicator

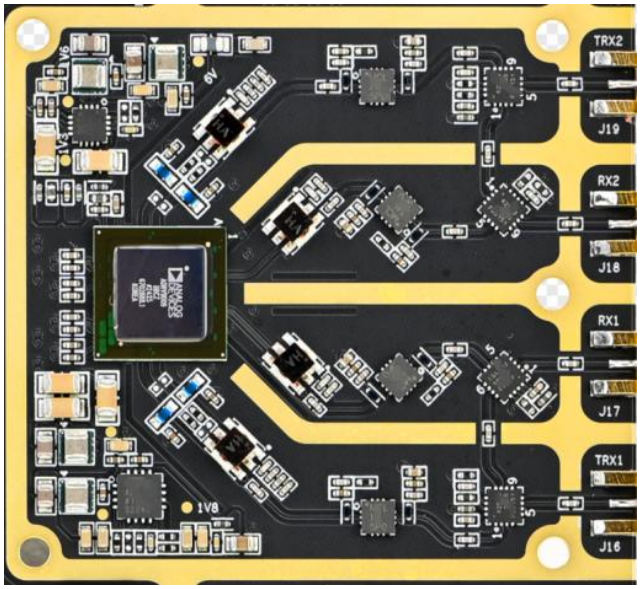
The **CR-P159** is designed with two LEDs, high level on and low level off. For more details, please refer to the schematic.

LED Bits	Pin Name	Pin Position
LED1(D17)	IO_L3N_44	AP12
LED2(D18)	IO_L1N_44	AP14



Part 2.19: ADRV9009 Introduction

The RF part of the **CR-P159** uses ADI's ADRV9009, and in this subsection will introduce in details, from the RF link, data channel, and clock part.



Part 2.19.1: RF Front-end Circuits

The RF front-end circuit involves three parts: balun, amplifier, and RF switch. The bandwidth of the balun is 10M-8Ghz, which covers the communication bandwidth of the ADRV9009.

The bandwidth of the amplifier is 10M-10Ghz, which also covers the communication bandwidth of ADRV9009, but the gain flatness of the amplifier in the whole communication bandwidth is slightly different. The following table can see the amplifier's indicators for each frequency point in detail.

FREQ	Gain	Isolation	Input Return Loss	Output Return Loss	Stability		IP-3 Output	1dB Comp. Output	Noise Figure
(MHz)	(dB)	(dB)	(dB)	(dB)	K	Measure	(dBm)	(dBm)	(dB)
10	20.46	27.17	9.18	14.25	1.15	0.87	25.43	19.41	8.92
100	22.20	25.13	22.46	21.95	1.05	0.50	30.65	22.45	1.37
200	22.28	25.07	23.42	23.85	1.04	0.48	28.68	22.50	1.06
300	22.29	25.08	23.27	24.74	1.05	0.49	29.17	22.55	1.02
400	22.29	25.15	22.98	25.12	1.05	0.50	27.58	22.54	0.97
500	22.29	25.19	22.58	25.57	1.05	0.50	29.99	22.55	0.96
1000	22.28	25.22	19.66	27.67	1.05	0.52	29.94	22.67	0.94
1200	22.28	25.25	18.42	27.51	1.05	0.52	31.22	22.78	0.96
1400	22.27	25.35	17.29	26.20	1.06	0.54	29.62	22.80	0.91
1600	22.26	25.42	16.20	24.55	1.06	0.55	29.97	22.83	0.94
1800	22.25	25.45	15.30	22.84	1.06	0.55	31.54	22.80	0.96
2000	22.23	25.55	14.44	21.32	1.06	0.57	32.31	22.68	0.97
2200	22.21	25.62	13.69	20.06	1.07	0.58	33.26	22.75	0.93
2400	22.18	25.67	13.06	19.05	1.07	0.58	29.73	22.78	1.07
2600	22.17	25.86	12.58	18.29	1.08	0.60	28.43	22.65	0.98
2800	22.16	25.88	12.19	17.80	1.08	0.61	30.87	22.38	1.05
3000	22.16	25.94	11.94	17.47	1.08	0.62	29.72	22.10	0.99
3200	22.16	26.04	11.74	17.30	1.08	0.63	28.81	21.77	1.06
3400	22.16	26.12	11.63	17.22	1.09	0.64	28.42	21.40	1.04
3600	22.16	26.20	11.60	17.21	1.09	0.64	28.39	21.13	1.06
3800	22.18	26.24	11.60	17.36	1.09	0.65	28.66	21.56	1.05
4000	22.20	26.27	11.70	17.64	1.09	0.65	29.25	21.51	1.16
4200	22.22	26.35	11.87	18.05	1.10	0.66	30.11	21.70	1.14
4400	22.24	26.42	12.10	18.50	1.10	0.67	28.80	21.74	1.19
4600	22.27	26.45	12.36	19.04	1.10	0.67	29.16	21.61	1.14
4800	22.32	26.55	12.67	19.61	1.11	0.68	29.37	21.83	1.19
5000	22.37	26.55	13.02	20.26	1.11	0.68	30.08	21.69	1.21
5200	22.43	26.66	13.44	20.86	1.12	0.69	28.61	21.57	1.22
5400	22.48	26.67	13.87	21.44	1.12	0.68	29.58	21.33	1.27
5600	22.55	26.67	14.42	21.98	1.12	0.68	28.42	21.15	1.23
5800	22.61	26.80	15.06	22.61	1.12	0.69	29.99	21.12	1.22
6000	22.66	26.85	15.80	23.09	1.13	0.69	28.20	21.28	1.22
6200	22.73	26.92	16.75	23.01	1.13	0.69	28.94	21.09	1.10
6400	22.77	26.98	17.74	22.66	1.14	0.69	29.82	21.04	1.20
6600	22.81	27.06	19.02	21.83	1.15	0.69	30.01	21.24	1.14
6800	22.86	27.19	20.71	20.64	1.16	0.70	29.50	21.05	1.15
7000	22.91	27.25	22.82	19.57	1.16	0.70	28.62	20.90	1.17
7200	22.94	27.35	24.91	18.68	1.17	0.70	29.79	20.90	1.14
7400	22.94	27.41	26.72	17.99	1.18	0.70	28.14	20.60	1.16
7600	22.93	27.57	26.69	17.33	1.20	0.71	30.13	20.20	1.15
7800	22.92	27.73	25.02	16.70	1.22	0.72	28.81	20.10	1.19
8000	22.89	27.96	23.01	16.34	1.25	0.74	29.42	19.59	1.23
8200	22.84	28.11	20.99	16.14	1.27	0.75	28.14	19.10	1.23
8400	22.78	28.34	19.42	16.02	1.30	0.77	28.40	18.78	1.23
8600	22.70	28.59	18.18	16.27	1.34	0.79	27.50	18.22	1.25
8800	22.59	28.83	17.09	16.71	1.39	0.82	27.89	18.12	1.33
9000	22.46	29.19	16.24	17.37	1.45	0.84	28.51	18.14	1.45
9200	22.31	29.42	15.50	18.23	1.51	0.87	28.63	17.44	1.59
9400	22.13	29.81	14.75	19.22	1.60	0.89	27.39	17.01	1.65
9600	21.89	30.15	14.06	20.07	1.69	0.92	28.06	16.83	1.83
9800	21.59	30.58	13.41	20.21	1.80	0.94	26.04	16.17	2.00
10000	21.25	31.03	12.70	19.46	1.94	0.96	27.73	16.12	2.14

The RF switch adopts SPDT one-in-two-out, with a bandwidth of 9K-8G, and the RF

switch has an internal integrated electrostatic protection circuit, which effectively protects the RF port. The switching logic of the corresponding RF switch can be referred to the following table, for the TX/RX switching of ADRV9009, you can refer to the schematic for the actual connection relationship to correspond to the adjustment.

LS	CTRL	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

Part 2.19.2: ADRV9009 Communication Ports

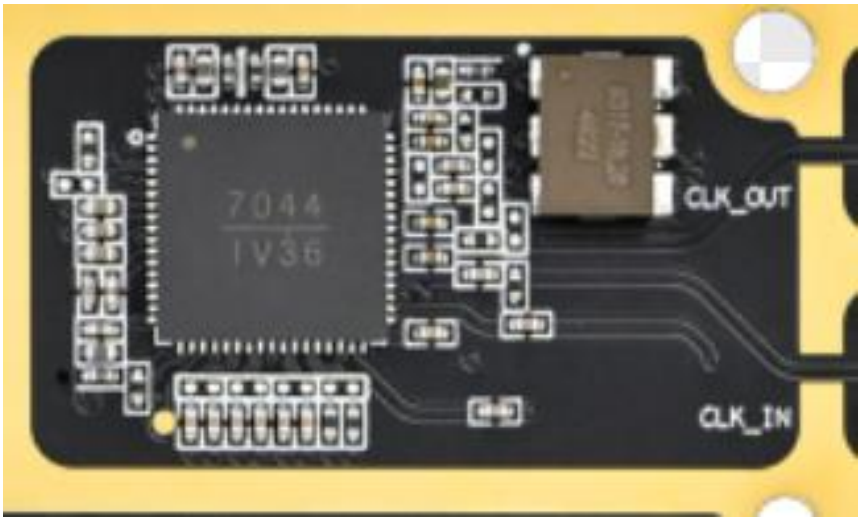
The ADRV9009 digital port is divided into data port and control port. The following table lists the pin correspondence, you can also refer to the schematic.

ADRV9009 Interface	Pin Name	Pin Position
ADRV9009_SERDIN_P0	MGT_TX_P0_128	T29
ADRV9009_SERDIN_N0	MGT_TX_N0_128	T30
ADRV9009_SERDIN_P1	MGT_TX_P2_128	P29
ADRV9009_SERDIN_N1	MGT_TX_N2_128	P30
ADRV9009_SERDIN_P2	MGT_TX_P1_128	R31
ADRV9009_SERDIN_N2	MGT_TX_N1_128	R32
ADRV9009_SERDIN_P3	MGT_TX_P3_128	M29
ADRV9009_SERDIN_N3	MGT_TX_N3_128	M30
ADRV9009_SYNCIN_P0	IO_L4P_67	T12
ADRV9009_SYNCIN_N0	IO_L4N_67	R12
ADRV9009_SYNCIN_P1	IO_L3P_67	U10
ADRV9009_SYNCIN_N1	IO_L3N_67	T10
ADRV9009_SERDOUT_P0	MGT_RX_P0_128	T33
ADRV9009_SERDOUT_N0	MGT_RX_N0_128	T34
ADRV9009_SERDOUT_P1	MGT_RX_P2_128	N31
ADRV9009_SERDOUT_N1	MGT_RX_N2_128	N32
ADRV9009_SERDOUT_P2	MGT_RX_P1_128	P33
ADRV9009_SERDOUT_N2	MGT_RX_N1_128	P34
ADRV9009_SERDOUT_P3	MGT_RX_P3_128	M33
ADRV9009_SERDOUT_N3	MGT_RX_N3_128	M34
ADRV9009_SYNCOUT_P0	IO_L2P_67	T13
ADRV9009_SYNCOUT_N0	IO_L2N_67	R13
ADRV9009_SYNCOUT_P1	IO_L1P_67	W12
ADRV9009_SYNCOUT_N1	IO_L1N_67	W11
ADRV9009_SYSREFCLK_IN_P	Come from CLK IC HMC7044LP10BE	
ADRV9009_SYSREFCLK_IN_N	Come from CLK IC HMC7044LP10BE	
ADRV9009_DEVCLK_IN_P	Come from CLK IC HMC7044LP10BE	
ADRV9009_DEVCLK_IN_N	Come from CLK IC HMC7044LP10BE	
ADRV9009_TX_ENABLE1	IO_L6N_47	F20
ADRV9009_TX_ENABLE2	IO_L4P_47	J19

ADRV9009_RX_ENABLE1	IO_L6P_47	G20
ADRV9009_RX_ENABLE2	IO_L4N_47	J20
ADRV9009_SPI_CLK	IO_L6P_48	F17
ADRV9009_SPI_CS	IO_L6N_48	F18
ADRV9009_SPI_DI	IO_L8N_48	E18
ADRV9009_SPI_DO	IO_L12P_48	A17
ADRV9009_nRST	IO_L10P_48	B18
ADRV9009_GP_INT	IO_L7P_47	E22
ADVR9009_GPIO_0	IO_L7P_48	E19
ADVR9009_GPIO_1	IO_L7N_48	D19
ADVR9009_GPIO_2	IO_L9N_48	C17
ADVR9009_GPIO_3	IO_L9P_48	D17
ADVR9009_GPIO_4	IO_L11N_48	C19
ADVR9009_GPIO_5	IO_L10N_48	B19
ADVR9009_GPIO_6	IO_L11P_48	C18
ADVR9009_GPIO_7	IO_L8P_48	E17
ADVR9009_GPIO_8	IO_L2N_48	H17
ADVR9009_GPIO_9	IO_L2P_48	J17
ADVR9009_GPIO_10	IO_L4N_48	K17
ADVR9009_GPIO_11	IO_L4P_48	L17
ADVR9009_GPIO_12	IO_L3P_48	L18
ADVR9009_GPIO_13	IO_L3N_48	K18
ADVR9009_GPIO_14	IO_L5P_48	G18
ADVR9009_GPIO_15	IO_L1N_48	H19
ADVR9009_GPIO_16	IO_L1P_48	H18
ADVR9009_GPIO_17	IO_L5N_48	G19
ADVR9009_GPIO_18	IO_L12N_48	A18

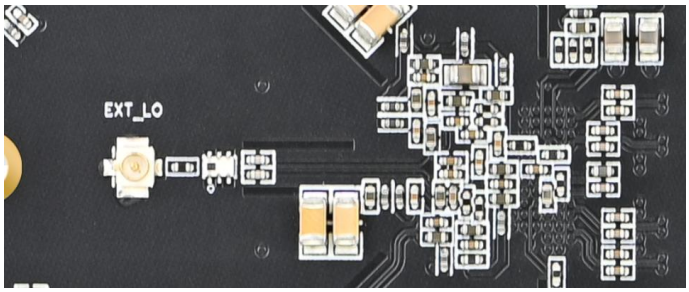
Part 2.19.3: ADRV9009 Clock Circuit

The input clock of ADRV9009 adopts a high-precision VCXO clock, the frequency of 122.88Mhz, through a dedicated clock chip to generate the required multi-channel clock, while the CR-P159 reserved clock input and output interfaces, such as the user needs a higher precision clock, you can pour in the clock from the outside, you can output the required clock. For the detailed use of the clock you can refer to the schematic and project code provided.



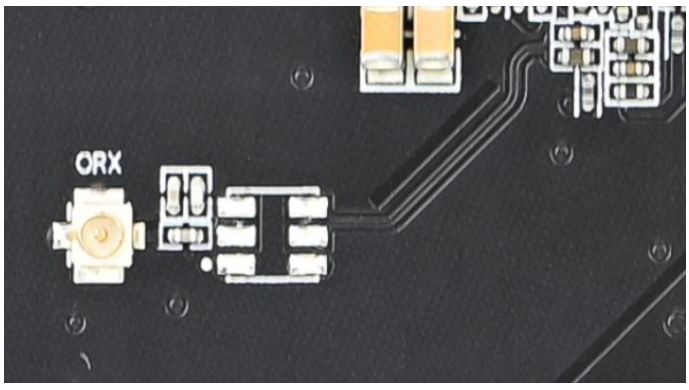
Part 2.19.4: ADRV9009 External Local Oscillator Input

One external local oscillator input is reserved on the **CR-P159**, the interface type is a generation of IPEX interface, details refer to the picture below and schematic provided.



Part 2.19.15: ADRV9009 ORX1 Input

One ORX1 input is reserved on the **CR-P159**, the interface type is a generation IPEX interface, and the output BALUN is not soldered by default. If you need to use this circuit, need to be informed in advance. , details refer to the picture below and schematic provided.



Part 2.20: PPS Interface

One way PPS is designed on on the **CR-P159** .The PPS signal can be configured as a PPS input through the direction pin, or as a PPS output through the direction pin, and the default is PPS input, which the user can choose according to the actual need. The PPS and direction pins are connected to the following pins of the FPGA respectively:

Signal Name	Pin Name	Pin Position
PPS_IN_OUT	IO_11N_44	AG15
PPS_DIR	IO_11P_44	AF15

Part 2.20: GPS Module

One GPS Module is designed on on the **CR-P159**, which enables GPS and BeiDou positioning function. We can configure and read the GPS module data through UART, in addition the module provides PPS signal. The following table lists the pin correspondences of the GPS module, for a more details refer to the schematic provided.

GPS Module	Pin Name	Pin Position
GPS_UART_TXD	IO_6P_44	AK13
GPS_UART_RXD	IO_2N_44	AN13
GPS_nRESET	IO_6P_44	AM13
GPS_PPS	IO_6P_44	AH13