RoHS Compliant
1310 nm Single-mode Transceiver (L1.1)
2×5, LC Duplex Connector, 3.3 V
155 Mbps ATM/SONET OC-3/SDH STM-1/Fast Ethernet

Features

- Compliant with 155 Mbps ATM and SONET OC-3 SDH STM-1 (L1.1)
- Industry standard 2×5 footprint
- LC duplex connector
- Single power supply 3.3 V
- Differential LVPECL inputs and outputs
- Compatible with solder and aqueous wash processes
- Class 1 laser product complies with EN 60825-1

Ordering Information

PART NUMBER	INPUT/OUTPUT	SIGNAL DETECT	VOLTAGE	TEMPERATURE
LS34-A3L-PC-N	DC/DC	LVPECL	3.3 V	0°C to 70 °C
LS34-A3L-PI-N	DC/DC	LVPECL	3.3 V	–40°C to 85°C

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	–40	85	°C	
Supply Voltage	*Vcc*	–0.5	4.0	V	
Input Voltage	V_{IN}	–0.5	*Vcc*	V	
Output Current	I_o	---	50	mA	
Operating Current	I_{OP}	---	400	mA	
Soldering Temperature	T_{SOLD}	---	260	°C	10 seconds on leads

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Operating Environment

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Case Operating Temperature (LS34-A3L-PC-N)	T_C	0	70	°C	
Case Operating Temperature (LS34-A3L-PI-N)	T_C	–40	85	°C	
Supply Voltage	*Vcc*	3.1	3.5	V	

Transmitter Electro-optical Characteristics

(*Vcc* = 3.1 V to 3.5 V, T_C = 0 °C to 70 °C (–40 °C to 85°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate	*B*	50	155	200	Mb/s	
Output Optical Power 9/125 μm fiber	*Pout*	–5	---	0	dBm	Average
Extinction Ratio	*ER*	10	---	---	dB	
Center Wavelength	λ_C	1261	1310	1360	nm	
Spectral Width (RMS)	$\Delta\lambda$	---	---	4	nm	
Rise/Fall Time (10–90%)	$T_{r,\,f}$	---	1	2	ns	
Output Eye	Compliant with Telcordia GR-253-CORE Issue 3 and ITU-T recommendation G-957					
Power Supply Current	I_{CC}	---	---	120	mA	Note 1
Disable input voltage-High	T_{dis}	2.2	---	---	V	
Disable input voltage-Low	T_{dis}	---	---	0.6	V	
Transmitter Data Input Voltage-High	$V_{IH} - V_{CC}$	–1.1	---	–0.74	V	Note 2
Transmitter Data Input Voltage-Low	$V_{IL} - V_{CC}$	–2.0	---	–1.58	V	Note 2

Note 1: Not including the terminations.
Note 2: These inputs are compatible with 10K, 10KH and 100K ECL and PECL input.

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Receiver Electro-optical Characteristics

(Vcc = 3.1 V to 3.5 V, T_C = 0 °C to 70 °C (–40 °C to 85 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Rate	B	50	155	200	Mb/s	
Optical Input Power -maximum	P_{IN}	0	---	---	dBm	Note 1
Optical Input Power –minimum (Sensitivity)	P_{IN}	---	---	–35	dBm	Note 1
Operating Center Wavelength	λ_C	1260	---	1610	nm	
Signal Detect-Asserted	P_A	---	---	–35	dBm	Average
Signal Detect-Deasserted	P_D	–45	---	---	dBm	Average
Signal Detect-Hysteresis	$P_A – P_D$	1.0	---	---	dB	
Signal Detect Output voltage - High	$V_{OH} – V_{CC}$	–1.1	---	–0.74	V	Note 2
Signal Detect Output voltage - Low	$V_{OL} – V_{CC}$	–2.0	---	–1.58	V	Note 2
Power Supply Current	I_{CC}	---	---	100	mA	Note 3
Data Output Rise, Fall Time (10%~90%)	$T_{r,f}$	---	1	2	ns	
Data Output Voltage-High	$V_{OH} – V_{CC}$	–1.1	---	–0.74	V	Note 2
Data Output Voltage-Low	$V_{OL} – V_{CC}$	–2.0	---	–1.58	V	Note 2

Note 1: The input data is at 155.52 Mbps, 2^{23}–1 PRBS data pattern with 72 “1”s and 72 “0”s inserted per the ITU-T recommendation G.958 Appendix 1. The receiver is guaranteed to provide output data with Bit Error Rate (BER) better than or equal to 1×10^{-10}.
Note 2: These outputs are compatible with 10K, 10KH and 100K ECL and PECL input.
Note 3: The current excludes the output load current.

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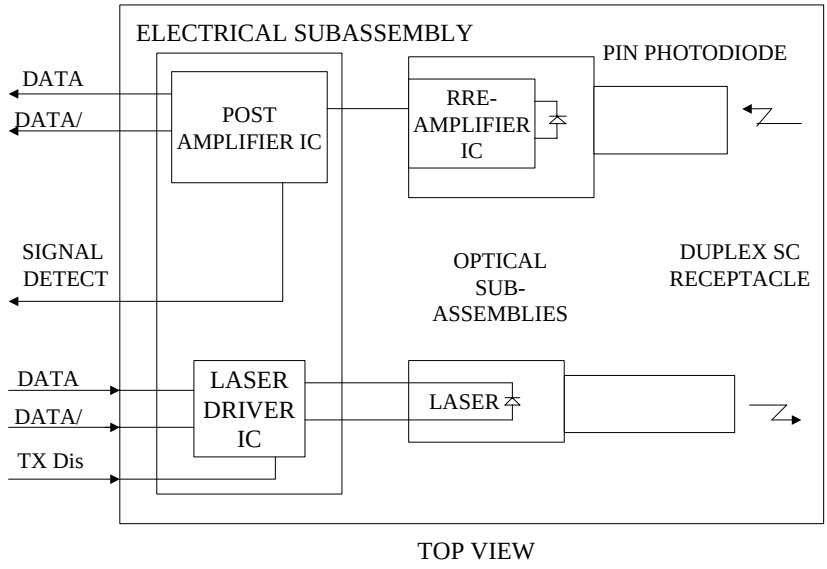
Block Diagram of Transceiver



TOP VIEW

Transmitter Section

The transmitter section consists of a 1310 nm InGaAsP laser in an eye safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LD driver IC which converts differential input LVPECL logic signals into an analog laser driving current.

Transmitter Disable

Transmitter Disable is a TTL control pin. To disable the module, connect this pin to +3.3 V TTL logic high “1”. While, to enable module connect to TTL logic low “0”.

Receiver Section

The receiver utilizes an InGaAs PIN photodiode mounted together with a trans-impedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

Receiver Signal Detect

Signal Detect is a basic fiber failure indicator. This is a single-ended LVPECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 1.0 dB higher than the deassert level.

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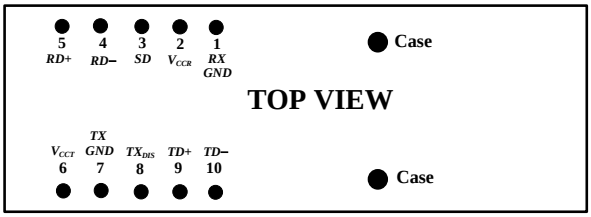
Connection Diagram

Pin-Out



PIN	SYMBOL	DESCRIPTION
1	*RX GND*	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	V_{CCR}	Receiver Power Supply Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
3	*SD*	Signal Detect. Normal optical input levels to the receiver result in a logic "1" output, V_{OH}, asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic "0" output V_{OL}, deasserted Signal Detect is a single-ended LVPECL output. *SD* can be terminated with LVPECL techniques via 50Ω to V_{CCR} – 2 V. Alternatively, *SD* can be loaded with a 180 Ω resistor to *RX GND* to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a LVPECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
4	*RD–*	*RD–* is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
5	*RD+*	*RD+* is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
6	V_{CCT}	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	*TX GND*	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.
8	TX_{DIS}	Transmitter Disable. Connect this pin to +3.3V TTL logic high "1" to disable transmitter. To enable module connect to TTL logic low "0" or open.
9	*TD+*	Transmitter Data In. Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)
10	*TD–*	Transmitter Data In-Bar. Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)

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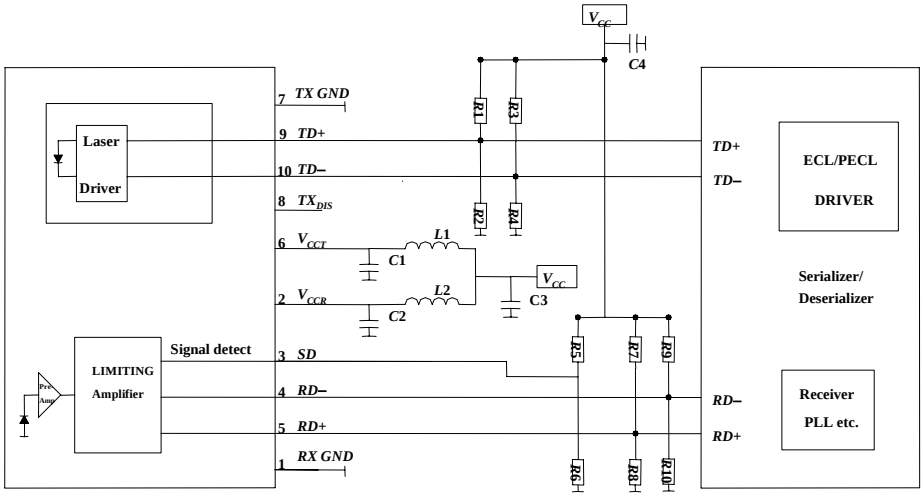
Recommended Circuit Schematic

DC/DC Coupling



$C1/C2/C4 = 0.1\ \mu F$ $C3 = 4.7\ \mu F$

$L1/L2 = 1\ \mu H$

$R1/R3/R5/R7/R9 = 130\ \Omega$ $R2/R4/R6/R8/R10 = 82\ \Omega$

In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

(1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.

(2) For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.

(3) Multi layer plane PCB is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.

(4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress V_{CC} noise over a broad frequency range, this prevents receiver sensitivity degradation due to V_{CC} noise.

(5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 μF capacitors and a surface-mount coil inductor for 1 μH inductor. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter.

(6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

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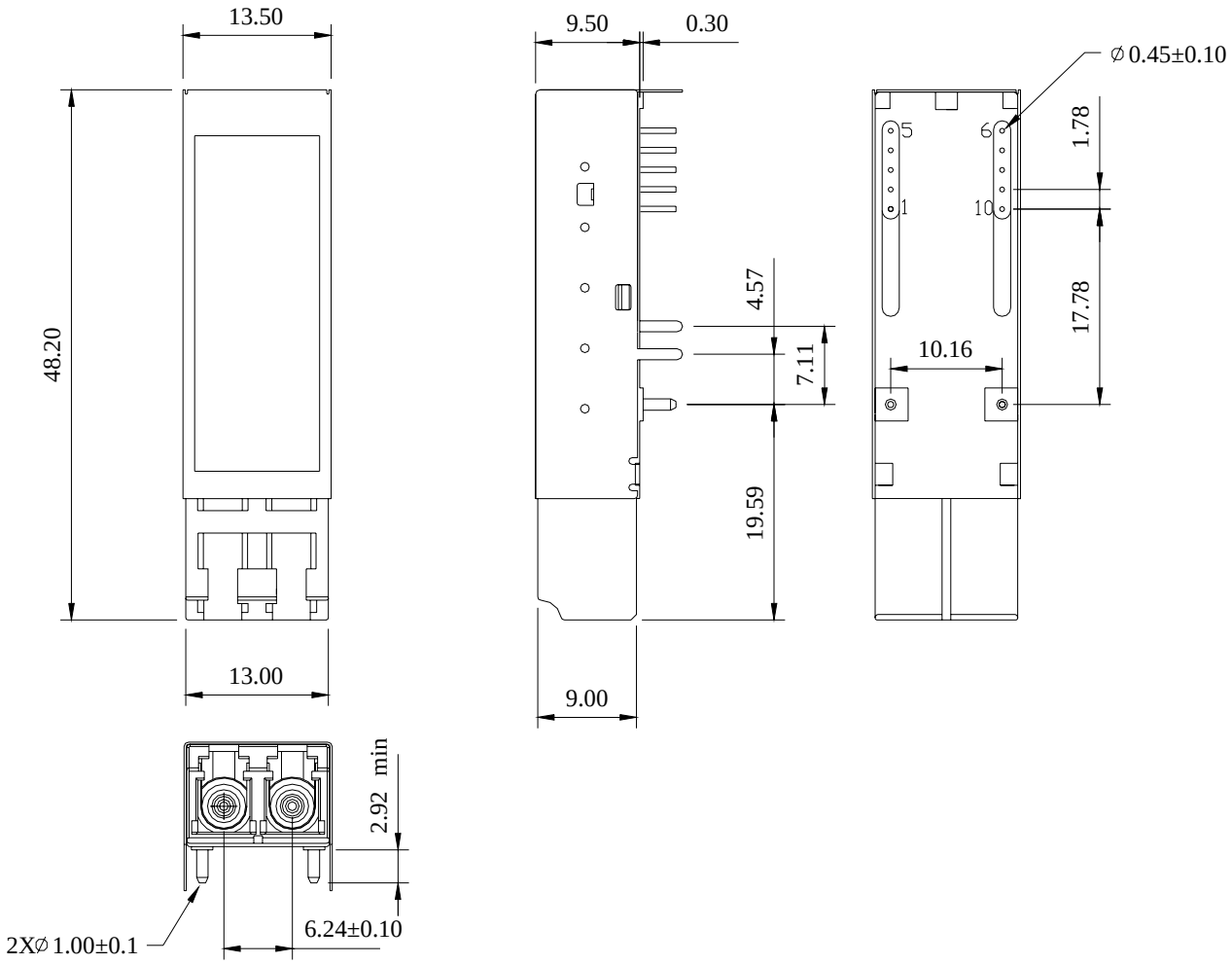
Drawing Dimensions



ALL DIMENSIONS ARE±0.20mm UNLESS OTHERWISE SPECIFIED

Unit: mm

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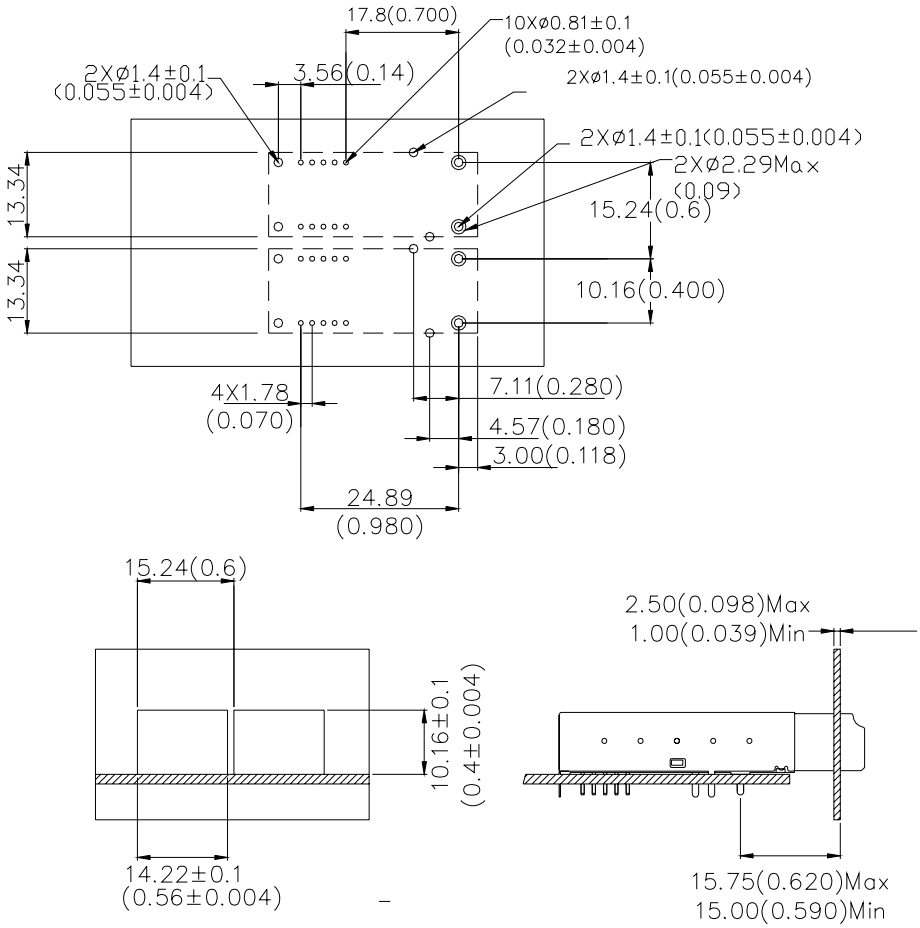
Recommended Board Layout Hole Pattern



Unit: mm (inches)

This transceiver is compatible with industry standard wave or hand solder processes. After wash process, all moisture must be completely remove from the module. The transceiver is supplied with a process plug to prevent contamination during wave solder and aqueous rinse as well as during handling, shipping or storage.

Solder fluxes should be water-soluble, organic solder fluxes. Recommended cleaning and degreasing chemicals for these transceivers are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing.

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Eye Safety Mark

The LS3 series Singlemode transceiver is a class 1 laser product. It complies with EN 60825-1 and FDA 21 CFR 1040.10 and 1040.11. In order to meet laser safety requirements the transceiver shall be operated within the Absolute Maximum Ratings. **Caution** **All adjustments have been done at the factory before the shipment of the devices. No maintenance and user serviceable part is required. Tampering with and modifying the performance of the device will result in voided product warranty.**	

Note : All information contained in this document is subject to change without notice.

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