High performance multi-mode PWM Controller

General Description

The AP8268 is a highly integrated current mode PWM control IC for high performance, low standby power and cost effective offline flyback converter applications. QR-PWM, QR-PFM, Burst-mode operation and low consumption device help to meet the standby energy saving standards and achieve higher efficiency. Excellent EMI performance is achieved with frequency modulation. The AP8268 offers complete protections including pin open/short protection, cycle-by-cycle current limiting, VDD over voltage protection, under voltage lockout, on-chip/external over temperature protection, output over voltage protection, over load protection, output diode short protection, etc.

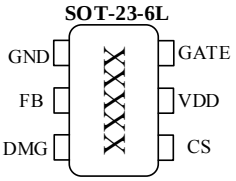
Features

- Soft start-up function
- multi-mode operation to achieve higher efficiency
- Proprietary Frequency Jitter for EMI
- Internal Slope and line input Compensation
- Adaptive PWM switching frequency
- Adaptive line Input Compensation
- Excellent Protection Coverage
  - ✧ Over Temperature Protection（OTP）
  - ✧ Output over voltage protection
  - ✧ Adjustable Over Current Protection（OCP）
  - ✧ Output Open/short Protection
  - ✧ Patented DMG resistor open/short protection（Latch）
  - ✧ Secondary Rectifier Short Protection
  - ✧ Over Load Protection（OLP）

Applications

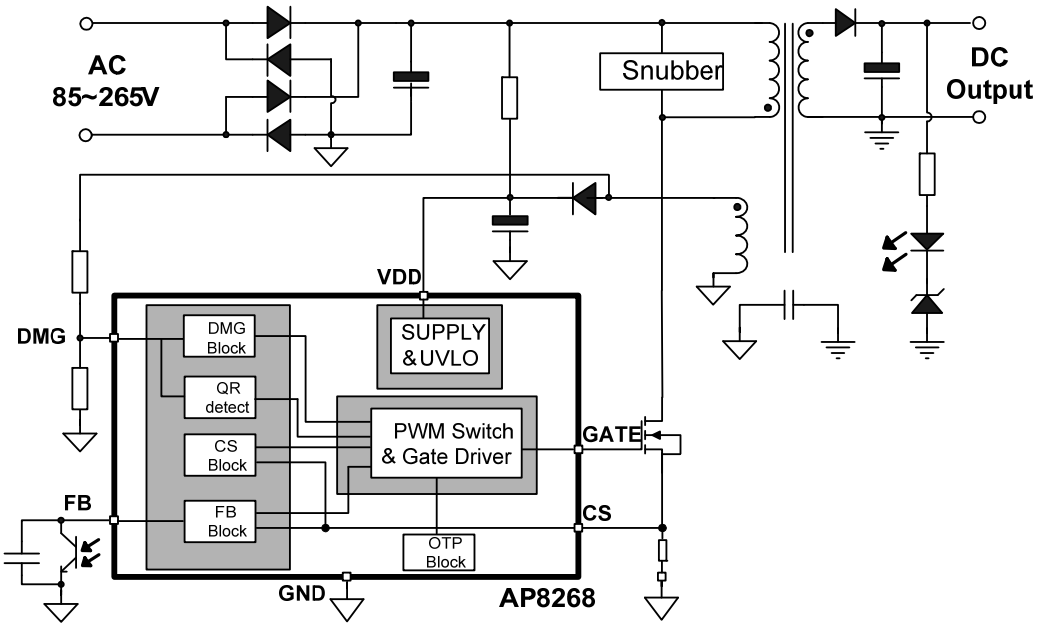
- Stand-by power
- Open-frame SMPS
- Adapter

Package/Order Information



Order codes	Package	Function
AP8268ATCC-R1	SOT-23-6L	QR
AP8268BTCC-R1	SOT-23-6L	No QR

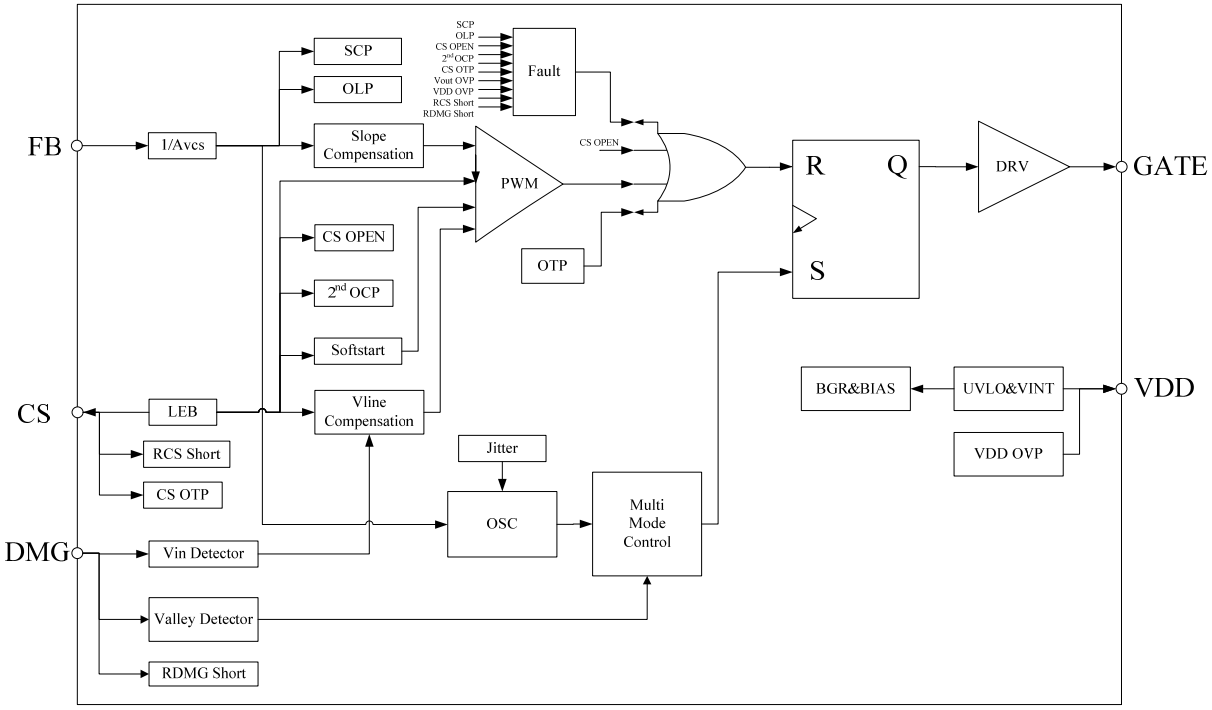
Typical Circuit



Pin Definitions

Pin Name	Pin Number	Pin Function Description
GND	1	Ground
FB	2	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and CS pin input.
DMG	3	Demagnetization pin. Input and output voltage detection by the voltage divider resistors.
CS	4	Current Sense Input
VDD	5	Positive Supply voltage Input
GATE	6	Totem-pole gate drive output for the power MOSFET.

Block Diagram



Absolute Maximum Ratings

Pin VDD……-0.3~45V

Pin DMG (I_{DMG}≤10mA)……-1~7V

Pin FB, CS……-0.3~7V

Pin GATE……-0.3~15V

Storage Temperature Range……-55~150℃

Lead Temperature (Soldering, 10Secs)……260℃

Package Thermal Resistance θ_{JA} （SOT-23-6L）…200℃/W

HBM ESD Protection (1)…… ±4kV

MM ESD Protection (2)…… 300V

Note：1.Test standard: JEDEC JDS-001-2014

2.Test standard:JESD22-A115C-2010

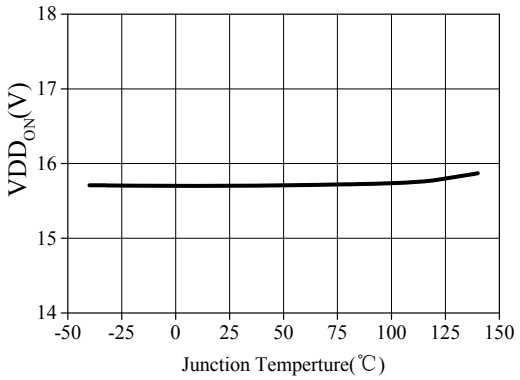
Electrical Characteristics

(T_A = 25°C,VDD=15V, unless otherwise specified)

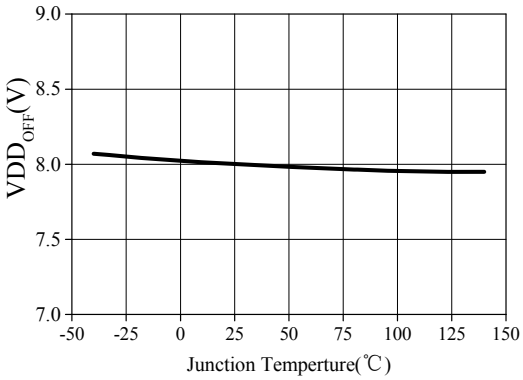
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD Supply Voltage Section						
VDD start up threshold	VDD_{ON}		15.0	15.7	17.0	V
VDD under voltage shutdown threshold	VDD_{OFF}		7.0	8.0	9.0	V
VDD OVP Voltage	V_{OVP}		37.0	40.5	43.0	V
Pull-up PMOS active	Vpull-up			10.0		V
VDD Supply Current Section						
Start up charging current	I_{VDD_ST}	VDD=VDD_{ON} - 1V		7.0	10.0	uA
Operating supply current, switching	I_{VDD0}	VFB=3.0V,CS=0.3V	1.0	2.2	3.5	mA
Operating supply current, under burst mode	I_{VDD1}	VFB=0.5V,CS=0.3V	0.4	0.5	1.0	mA
Operating supply current, with protection tripping	I_{VDD_Fault}		0.2	0.5	1.5	mA
Oscillator Section						
Switching Frequency	F_{OSC}	IDMG>330uA	60.0	65.0	70.0	kHz
		IDMG<330uA	80.0	90.0	100.0	kHz
Burst Mode Frequency	Fosc_BM	VFB=1.5V,CS=0.3V	20.0	25.0	28.0	kHz
Jitter Frequency	F_jitter			30		Hz
Frequency Modulation range	△Fosc			±6		%
FB Section						
FB Loop Voltage	V_{FB}		4.8	5.1	5.4	V
FB Short Current	I_{FB_SHORT}		0.17	0.2	0.23	mA
Maximum duty cycle	Dmax		70.0	80.0	90.0	%
Green Mode Entry Voltage	$V_{FB\_PFM\_L}$	IDMG>330uA		2.3		V
		IDMG<330uA		1.75		V
Green Mode Ending	$V_{FB\_PFM\_H}$	IDMG>330uA		2.7		V

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage		IDMG<330uA		2.0		V
Burst Mode Entry Voltage	$V_{FB\_BM\_L}$			1.15		V
Burst Mode Ending Voltage	$V_{FB\_BM\_H}$			1.25		V
OLP threshold voltage	Vth_OLP		4.1	4.4	4.7	V
OLP De-Bounce time	Td_OLP			60.0		ms
Current Sense Section						
Soft-start time	Tss			6.0		ms
Leading edge blanking time	TLEB			400		ns
Internal Current Limiting threshold Voltage	Vth_OCP		0.7	0.75	0.8	V
Threshold voltage of Secondary Rectifier Short Protection	V_{DSP}			1.1		V
De-Bounce time of SRCP	Td_DSP			7		cycles
CS OTP threshold Voltage	V_CSOTP			0.8		V
CS OTP De-Bounce time	Td_CSOTP			48.0		ms
DMG Section						
DMG OVP voltage	Vth_DOVP		2.7	3.0	3.3	V
De-Bounce time of DMG OVP	Td_DOVP			7.0		cycles
Maximum hold time	Thold			5.0		us
Minimum duty cycle of slope compensation	Duty_Slope	Fosc=65kHz		35.0		%
Minimum turn ON time	Ton_max		10.0	12.0	14.0	us
GATE Section						
Output Low Level	V_{OL}				1.0	V
Output High Level	V_{OH}		6.0			V
Output Clamp Voltage Level	V_clamping	CS=0.3V,FB=3V		12.0		V
Output Rising Time	T_r	1.2V~10.8V@CL=1000pF		60.0		ns
Output Falling Time	T_f	10.8V~1.2V@CL=1000pF		20.0		ns
Thermal Section						
Thermal shutdown temperature	T_{SD}		135	150		°C
Thermal shutdown hysteresis	T_{HYST}			30		°C

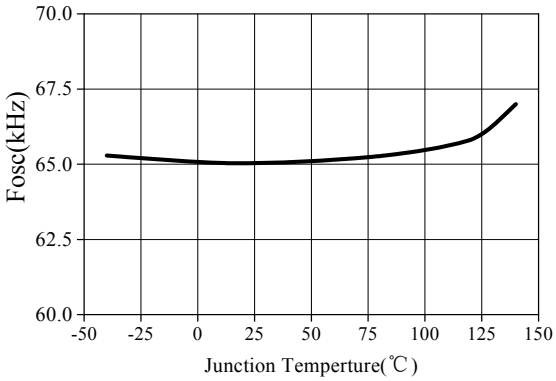
Typical Characteristics Plots



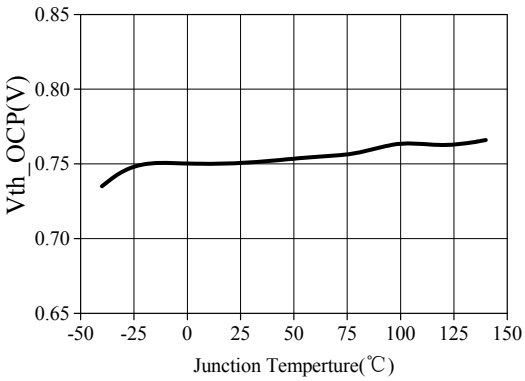
(a) VDD_{ON} vs T_j



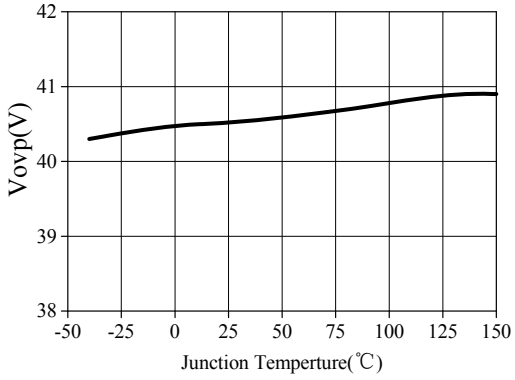
(b) VDD_{OFF} vs T_j



(c) F_{OSC} vs T_j



(d) Vth_OCP vs T_j



(e) V_{OVP} vs T_j

Functional Description

1. Start-up

The startup current of AP8268 is designed to be very low so that VDD could be charged up above VDD_{ON} threshold level and device starts up quickly. Also a large value startup resistor can be used to minimize the power loss.

When the VDD voltage reaches VDD_{ON}, the chip starts to work. After the start-up process, the auxiliary winding of the transformer provides energy to the VDD capacitor.

2. Soft Start-up

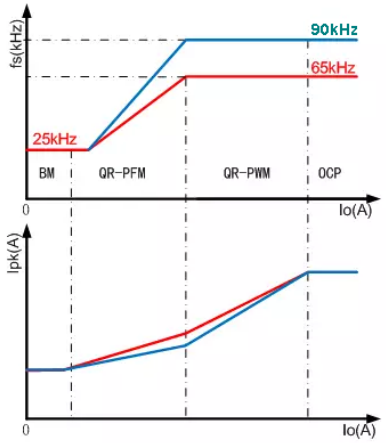
In the process of start up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and prevent the transformer turning into the saturation state. Typically, the duration of soft-start is 6ms.

3. Oscillator

The switching frequency of AP8268 is internally fixed. When the input voltage is high (I_{DMG}>330uA), the frequency is 65kHz. When the input voltage is low (I_{DMG}<330uA), the frequency is 90kHz.The AP8268 can ease the design of the transformer.

4. PFM Mode

PFM operation helps to meet the standby energy saving standards and achieve higher efficiency. When FB is less than $V_{FB\_PFM\_L}$, the AP8268 enter PFM. Lighter the load, less the switching frequency. The minimum switching frequency is closed at 25kHz.



5. Quasi-Resonant Switching（AP8268A）

The AP8268 can calculate the frequency of the Lm and Clump oscillator. The valley detection is realized by DMG pin to achieve accurate valley opening, and improve the conversion efficiency under DCM。

6. Burst-mode Operation

The AP8268 enters burst-mode operation in order to minimize the power dissipation in standby mode. As the load decreases, the feedback voltage decreases. When the voltage on FB pin falls below $V_{FB\_BM\_L}$ (1.15V typically), the device enters burst mode and power MOSFET stops switching. It can be switched on again once the voltage on FB pin exceeds $V_{FB\_BM\_H}$.

7. Gate Driver

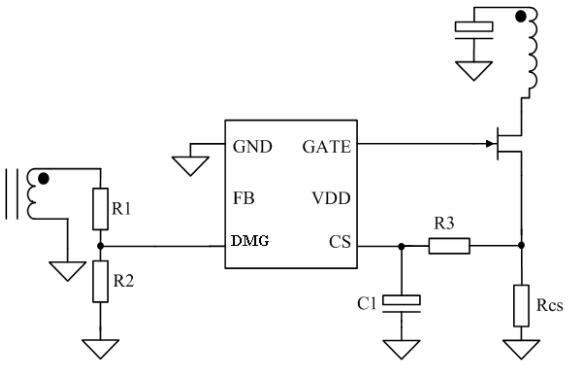
The output stage of AP8268 is a fast totem pole gate driver. Dead time has been added to minimize heat dissipation, increases efficiency and enhances reliability. The output driver is clamped by an internal 12V zener diode in order to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

8. Internal Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the feedback voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

9. Line Input Compensation

The AP8268 offers Line Input Compensation; this feature improves the power limit constant output. The PN8268 detects the input voltage across DMG pin and generate the compensated current. Thus the compensated current can be calculated as $I_{LC}=K*I_{DMG}$, where K is the compensated coefficient. I_{LC} multiplied R3 equals the compensated voltage that can limit the pulse-by-pulse current.



10. Over Voltage Protection

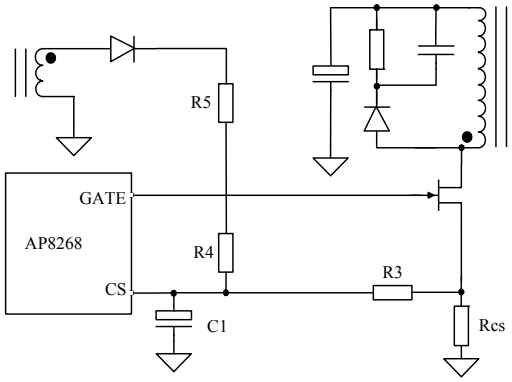
AP8268 realizes accurate over voltage protection by sampling auxiliary winding voltage in degaussing phase. When the voltage of the sampled DMG platform is greater than 3V and lasts for 7 PWM cycles, the output OVP protection is triggered and the output is closed. The protection point of DMG OVP is set by selecting the pull down resistance R2 of DMG.

11. Over Load Protection (OLP)

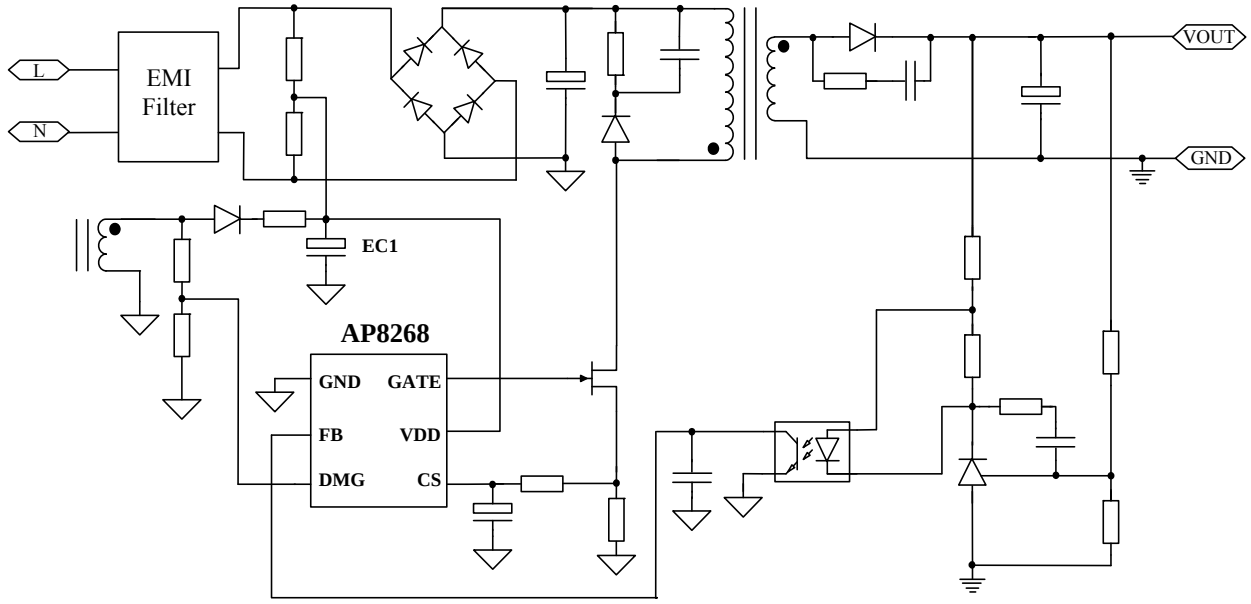
Overload is defined as the load current exceeding a pre-set level due to an accident event as a fault. If FB exceeds 4.4V for more than 60ms (de-bounce time of OLP), the protection circuit should be activated to protect the SMPS.

12. Over Temperature Protection

Both an internal OTP circuit and an external OTP circuit are embedded inside the AP8268 to prevent the system from hot damage. If the temperature exceeds about 150℃, OTP fault is activated. Simultaneously, an NTC resistor is implemented to sense whether there is any hot-spot of power circuit. If the voltage exceeds the external OTP trip level VCS>V_CSOTP (typical 0.8V), an internal counter has been added to prevent incorrect OTP detection. However, if Td_CSOTP of subsequent OTP events are detected, the external OTP protection is tripped.



Typical Application

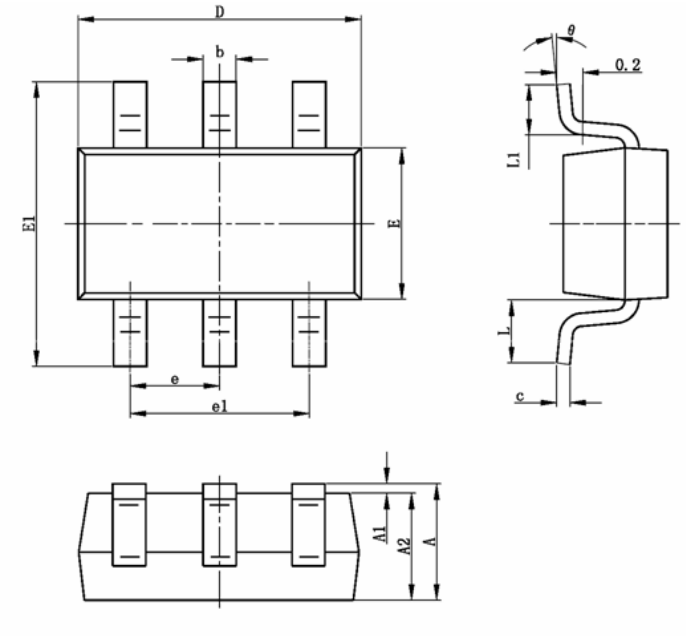


Component Parameter and Layout Considerations:

1. VDD capacitor EC1 should be placed at the nearest place from the VDD pin and the GND pin.

Package Information

SOT-23-6L Package Information



Size / Symbol	Min. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Max. (mm)
A	1.050	1.250	E1	1.500	1.700
A1	0.000	0.100	E	2.650	2.950
A2	1.050	1.150	e	0.950(BSC)	
b	0.300	0.500	e1	1.800	2.000
c	0.100	0.200	L1	0.300	0.600
D	2.820	3.020	Θ	0°	8°

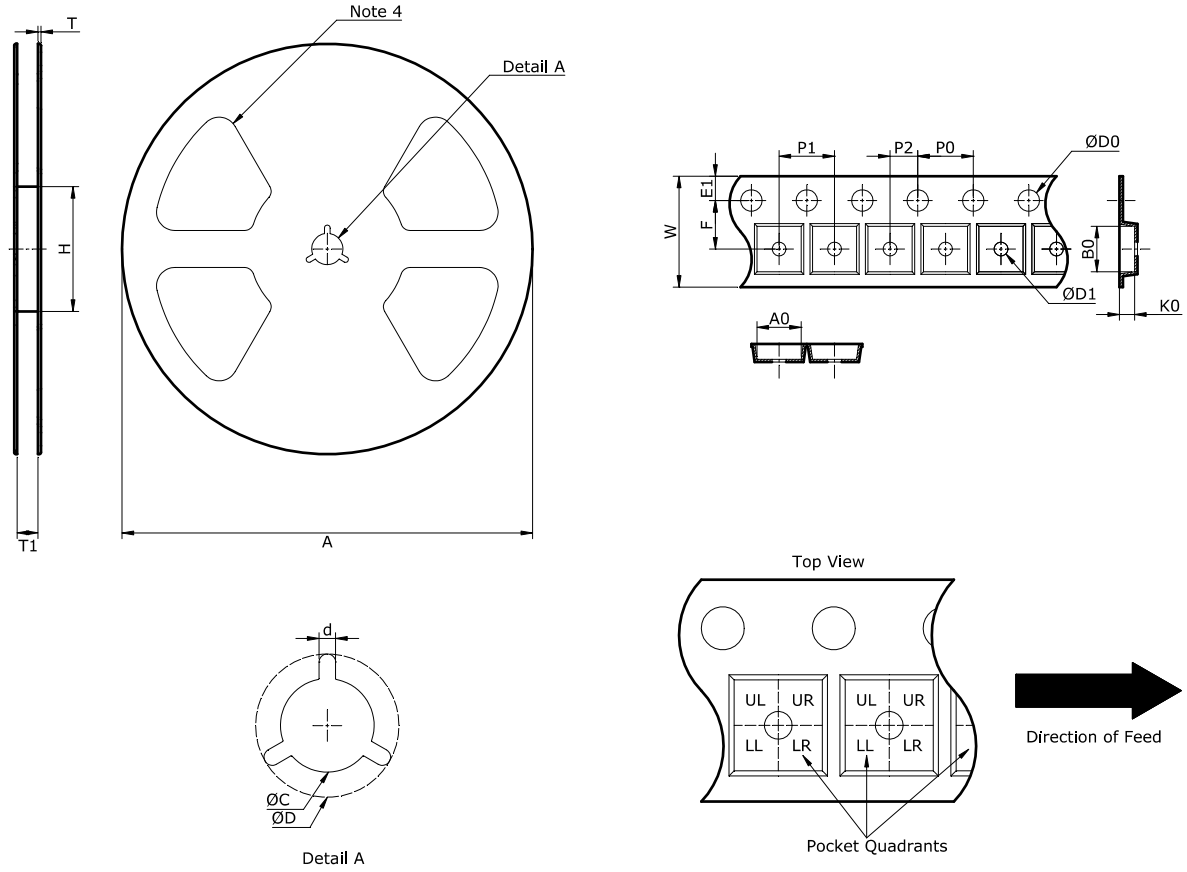
Order codes	Top mark	Package
AP8268A	69XXX	SOT-23-6L
AP8268B	68XXX	

Note:：XXX: Internal Code

Notes:

1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Tape and Reel Information



SOT-23-6L Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
180 +0/−3	1.4 ±0.3	9.5 ±1.0	60 ±0.5	13.00 ±0.20	18.70 ±0.40	2.30 ±0.10	3.17 ±0.10	3.10 ±0.1	1.10 ±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
8.0 +0.3/−0.1	3.5 ±0.1	1.75 ±0.1	4.0 ±0.10	4.0 ±0.1	2.0 ±0.05	1.5 +0.1/−0	1.0 +0.25/−0	LL	

Notes:

1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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