Shenzhen Leadtek Electronics Co.,Ltd

PRODUCT SPECIFICATION

TFT-LCD MODULE

Module No：LTK069WXBCT11-V0

☑ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
		

Final Approval by Customer

Approved by	Comment

※The specification of “TBD” should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

Contents

Document Revision History

Change No.	Date	Subject And Reason	Version No.	Responser
1	2023.02.20	New	V0	

1.0General Description

1.1 Introduction

LTK069WXBCT11-V0 Display model 6.86” LCM is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel and a driving circuit.This TFT LCD has a 6.86(6:16) inch diagonally measured active display area with (480 horizontal by1280 vertical pixel) resolution.

1.2. Features

- 6.86 (6:16 diagonal) inch configuration
- MIPI interface
- 16.7M color
- RoHS Compliance
- Halogen Free

1.3. General information

Item	Specification	Unit
Outline Dimension	67.00 (H) x 181.40 (V) x6.28(D)	mm
Display area	60.22(H)*160.59(V)	mm
Number of Pixel	480 RGB (H) x1280 (V)	pixels
Pixel Size	0.12546x0.12546	mm
Pixel arrangement	RGB Vertical stripe	
Display mode	Normally Black	
Color Filter Array	RGB vertical stripes	
Backlight	12 White LED	
Interface	MIPI	
Luminance	350	cd/m2
Weight	TBD	g

2.0 Absolute Maximum Ratings

2.1 Electrical Absolute Rating

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VCC	-0.3	+3.6	V	GND=0
	IOVCC	+0.3	+3.3	V	GND=0

2.2 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	Topa	-20	70	℃	
Storage Temperature	Tstg	-30	80	℃	

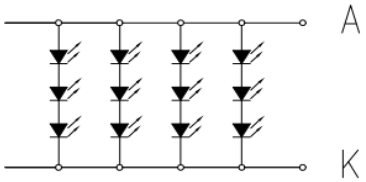
2.3 Back-light Unit:

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
LED Current	IF	–	120	–	mA	–	–
LED Voltage	VF	8.4	9.6	9.9	V	I=120mA	–
Brightness			350		Nits	I=120mA	
Color temperature		6500K	7500K	8300K		@CA310	
Life Time		–	50000	–	Hr.	I=120mA	–
Color	White						

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2)Ta=25±2℃

(3)Test condition: LED Current 120mA



CURRENT IF=120mA, VF=9.9V (Reference)
3C*4B=12LED

3.0 Optical Characteristics

3.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	1000	1500	—		(1)(2)(4)
Response time		Tr+ Tf		—	30	35	msec	(1)(3)
Color chromaticity (CIE1931)		White	W_x	-0.030	0.293	+0.030		(1)(4) CF Glass C light
			W_y		0.322			
		Red	Rx		0.656			
			Ry		0.255			
		Green	Gx		0.360			
			Gy		0.576			
		Blue	Bx		0.137			
			By		0.098			
Viewing angle	Hor.	Θ_L	CR>10	-	80	—		
		Θ_R		-	80	—		
	Ver.	Θ_U		-	80	—		
		Θ_D		-	80	—		
NTSC					60%	--	%	
Luminance Uniformity		YU		70	75		%	

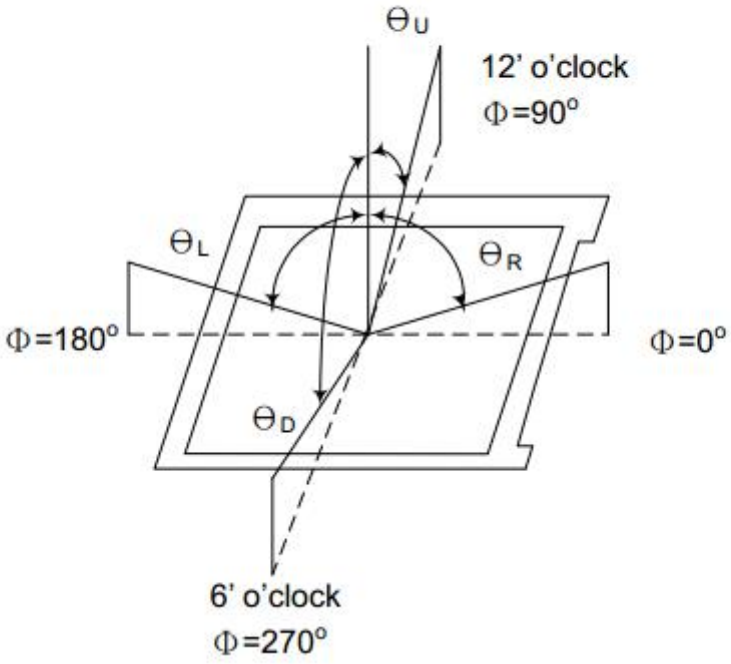
3.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2℃
- 15min. warm-up time.

3.3 Measuring Equipment

- TOPCON BM-7
- Measuring spot size : field 2°

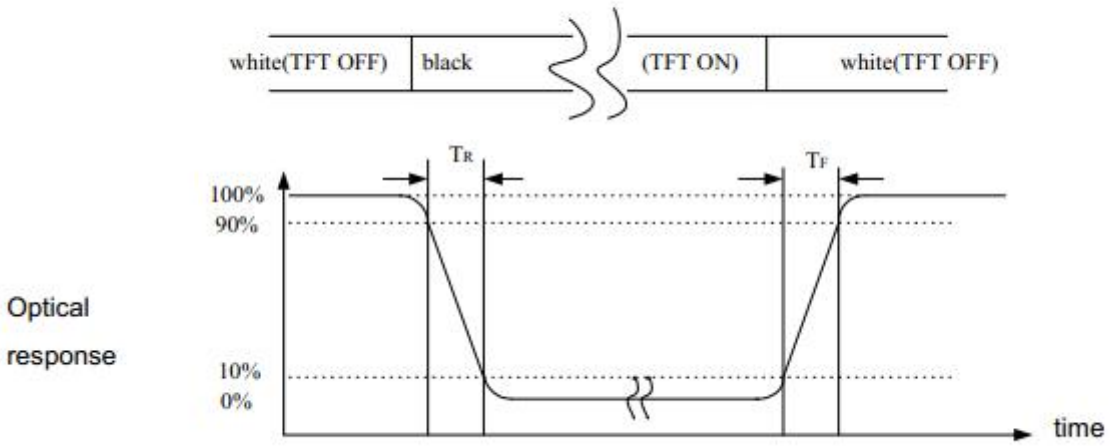
Note (1) Definition of Viewing Angle:



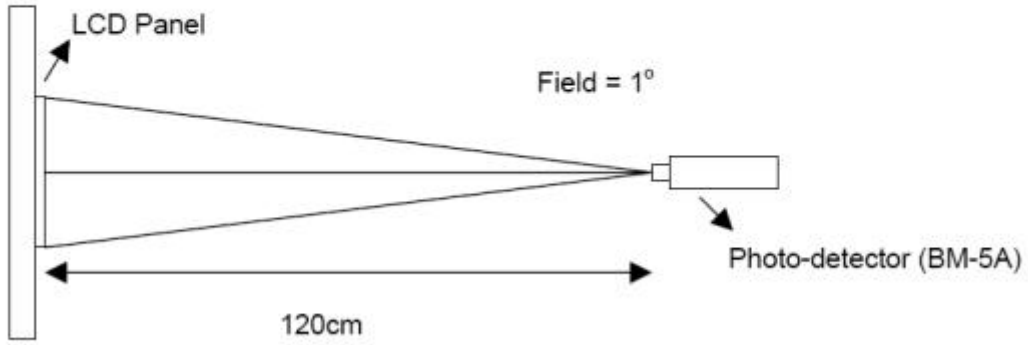
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

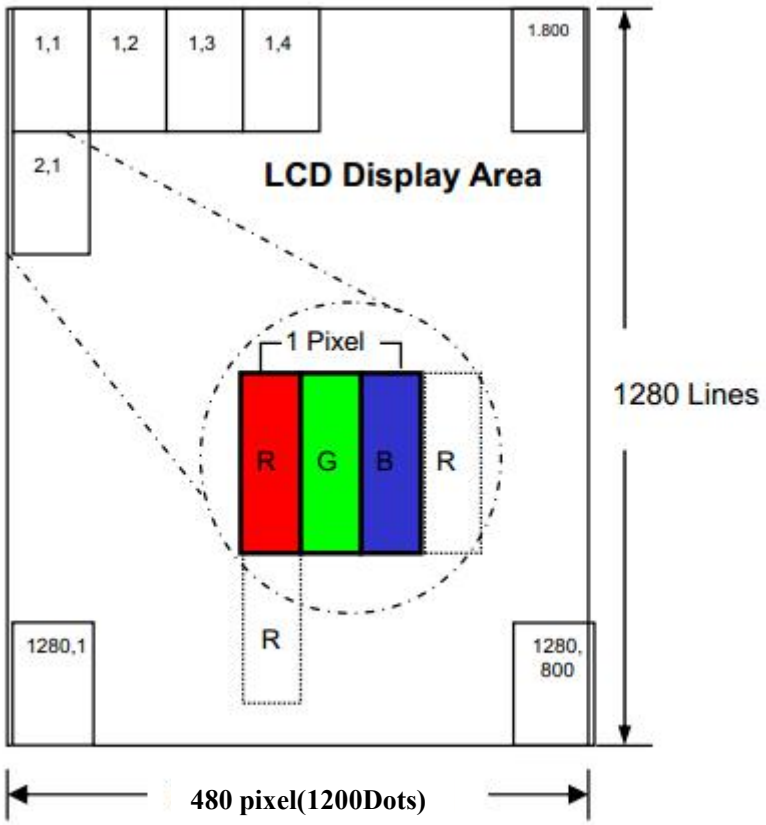
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



4.0Pixel Format



5.0 Interface Pin Connection

	Symbol	Function
1	GND	Power ground.
2	MIPI_D0+	MIPI_DP0+ are differential data signal line
3	MIPI_D0-	MIPI_DP0- are differential data signal line
4	GND	Power ground.
5	MIPI_D1+	MIPI_DP1+ are differential data signal line
6	MIPI_D1-	MIPI_DP1- are differential data signal line
7	GND	Power ground.
8	MIPI_CLK+	CLOCK Lane positive-end input pin
9	MIPI_CLK-	CLOCK Lane engative-end input pin
10	GND	Power ground.
11	MIPI_D2+	MIPI_DP2+ are differential data signal line
12	MIPI_D2-	MIPI_DP2- are differential data signal line
13	GND	Power ground.
14	MIPI_D3+	MIPI_DP3+ are differential data signal line
15	MIPI_D3-	MIPI_DP3- are differential data signal line
16	GND	Power ground.
17	GND	Power ground.
18	IOVCC(1.8V)	A supply voltage to the digital circuit. (1.8V)
19	IOVCC(1.8V)	A supply voltage to the digital circuit. (1.8V)
20	TP-VDD	Power supply for CTP.
21	TP-SDA	SDA pin for CTP
22	TP-SCL	SCL pin for CTP
23	TP-GND	GND pin for CTP
24	RSTB	Reset signal（Low: Active).
25	STBYB	Not connect
26	TP-INT	INT pin for CTP
27	GND	Power ground.
28	LED-	LED cathode.

29	LED-	LED cathode.
30	GND	Power ground.
31	NC	Not connect
32	GND	Power ground.
33	GND	Power ground.
34	NC	Not connect
35	LED+	LED anode.
36	LED+	LED anode.
37	GND	Power ground.
38	VCC(3.3V)	A supply voltage to the digital circuit. (3.3V)
39	VCC(3.3V)	A supply voltage to the digital circuit. (3.3V)
40	TP-RESET	Reset pin for TP

5.1 Absolute Maximum Ratings

Electrical Maximum Ratings (VSS=0V)

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VCI	+0.3	+3.6	V	GND=0
	IOVCC	+0.3	+3.3	V	GND=0

Table 1: Electrical Maximum Ratings – for IC

Note:

1. VCC,IOVCC, GND must be maintained.

2. The modules may be destroyed if they are used beyond the absolute maximum ratings.

3.Ta=25+/-2℃

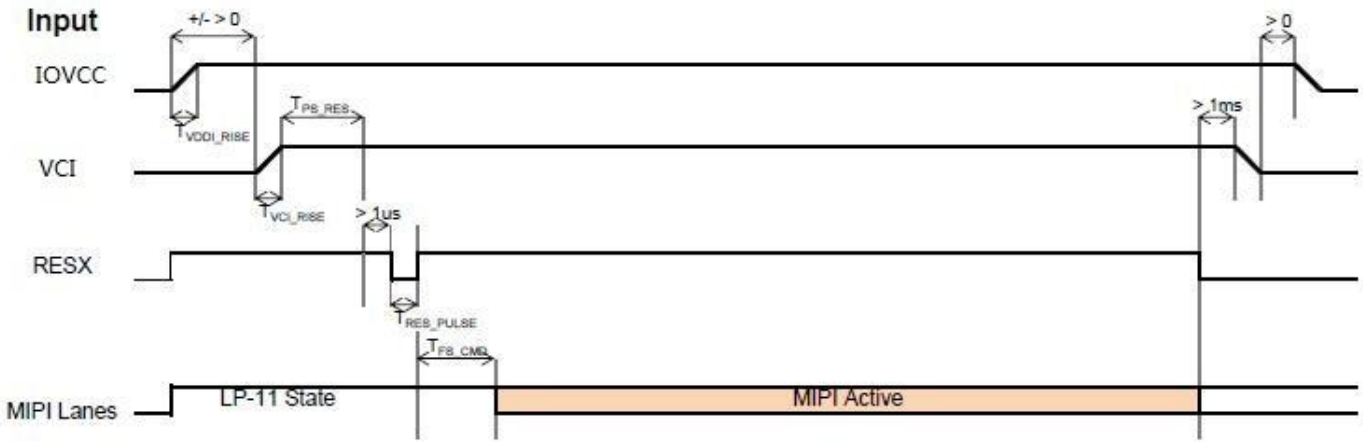
5.2. Electrical Specifications(Typical Operation Conditions, At Ta = 25 °C)

Table 2

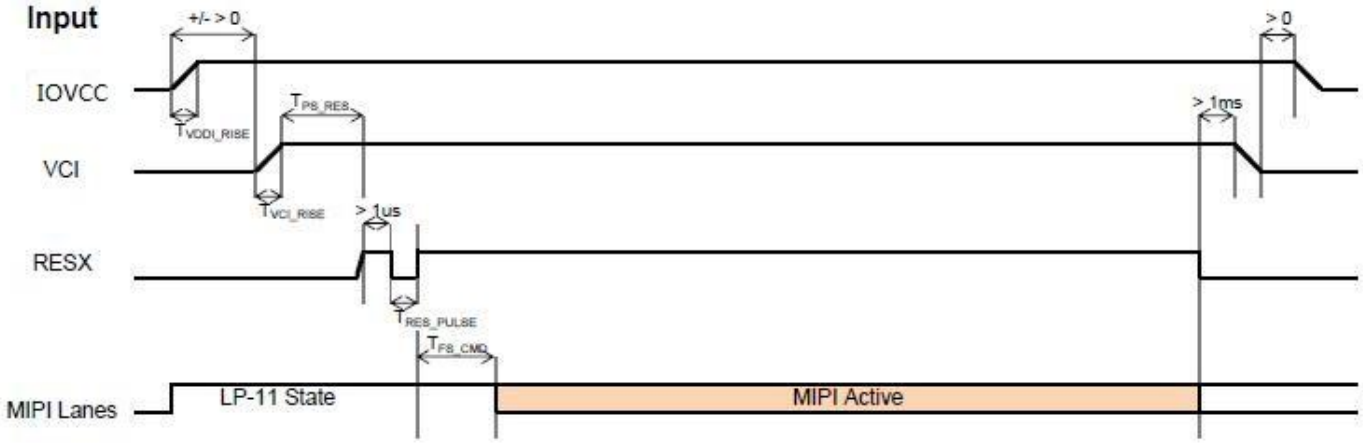
ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Power Supply Voltage	**VCI**	**3.0**	**3.3**	**3.6**	**V**	**-**
	IOVCC	**1.65**	**1.8**	**3.3**	**V**	**-**

5.2.1 Power Sequence

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{IOVCC_RISE}	IOVCC Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	IOVCC /VCI on to Reset high	10	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

5.03 AC Characteristics

5.03.1 DSI Timing Characteristics

High Speed Mode – Clock Channel Timing

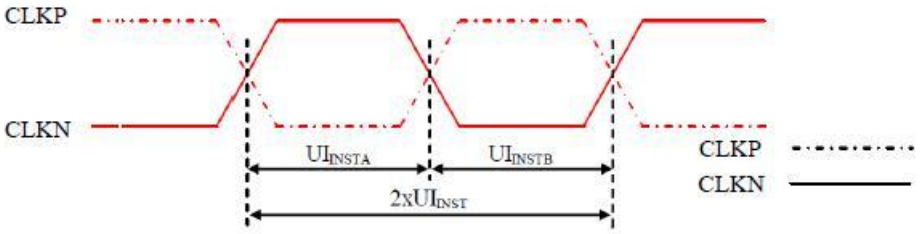


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

High Speed Mode – Data Clock Channel Timing

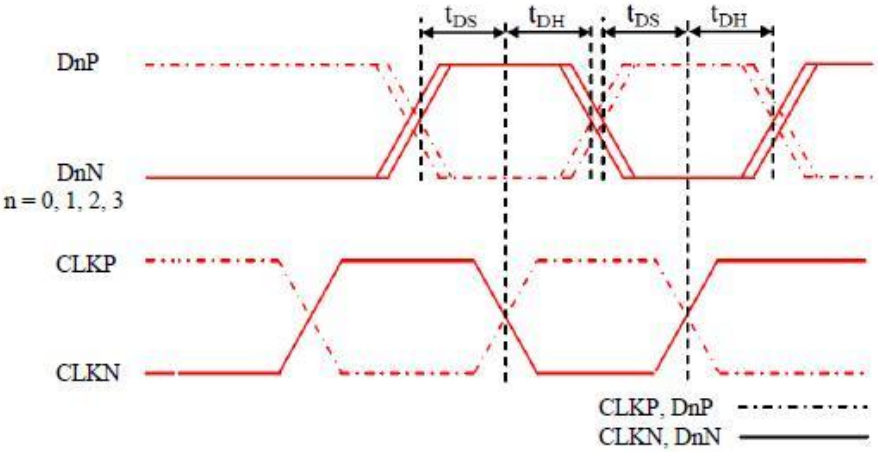


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rising and Falling Timings

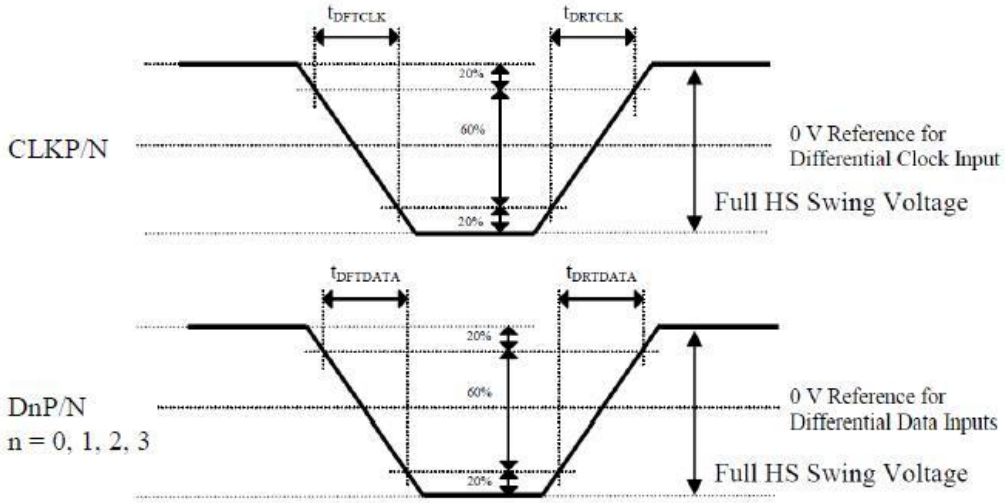


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-04) are illustrated for reference purposes below.

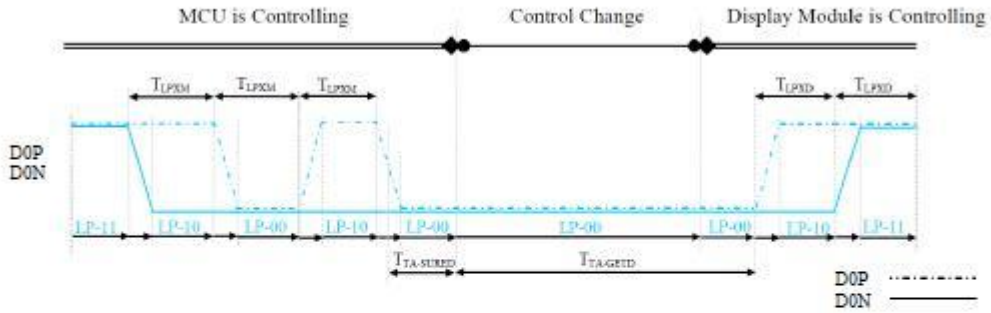


Figure 108: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-04) to the MCU are illustrated for reference purposes below.

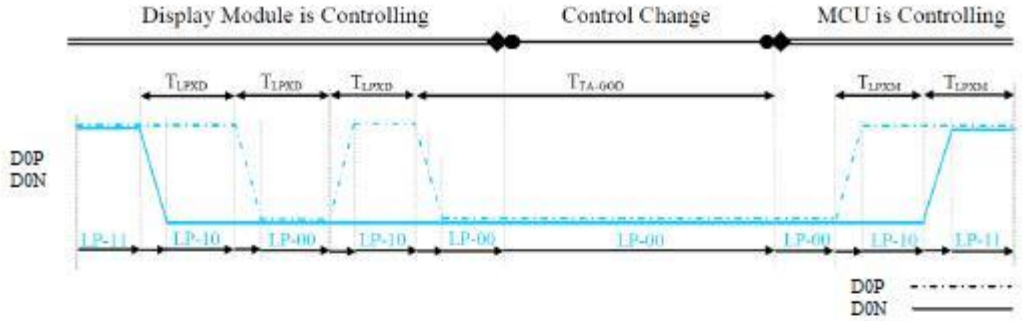


Figure 109: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C-04)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-04) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-04) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-04)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

Data Lanes from Low Power Mode to High Speed Mode

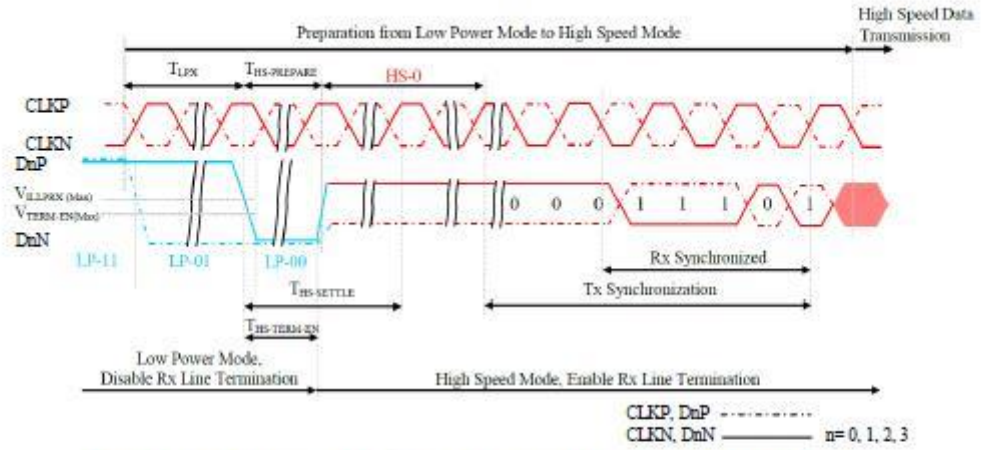
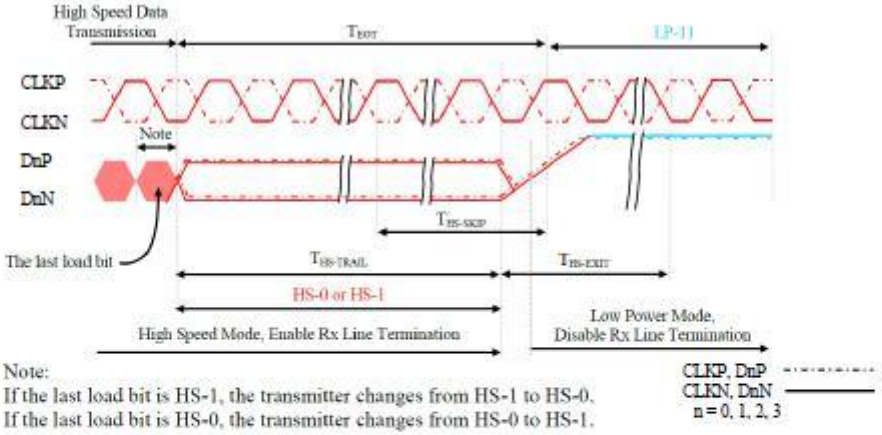


Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	T_{HS-EOT}	Time to driver LP-11 after HS burst	100	-	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

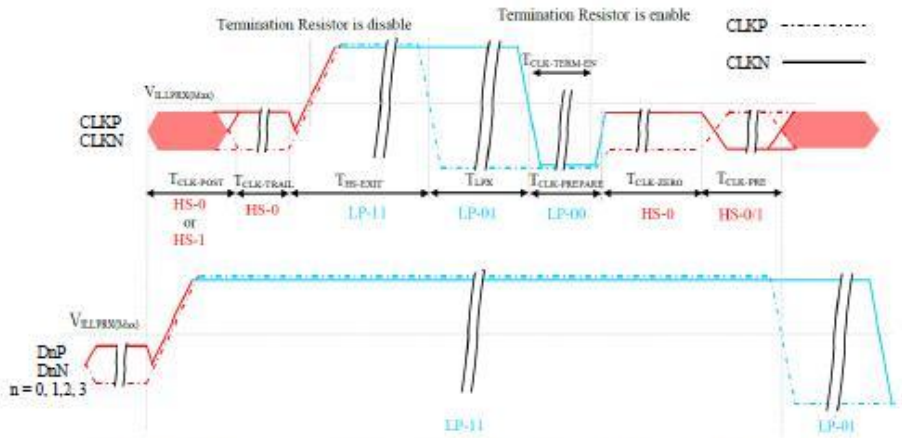
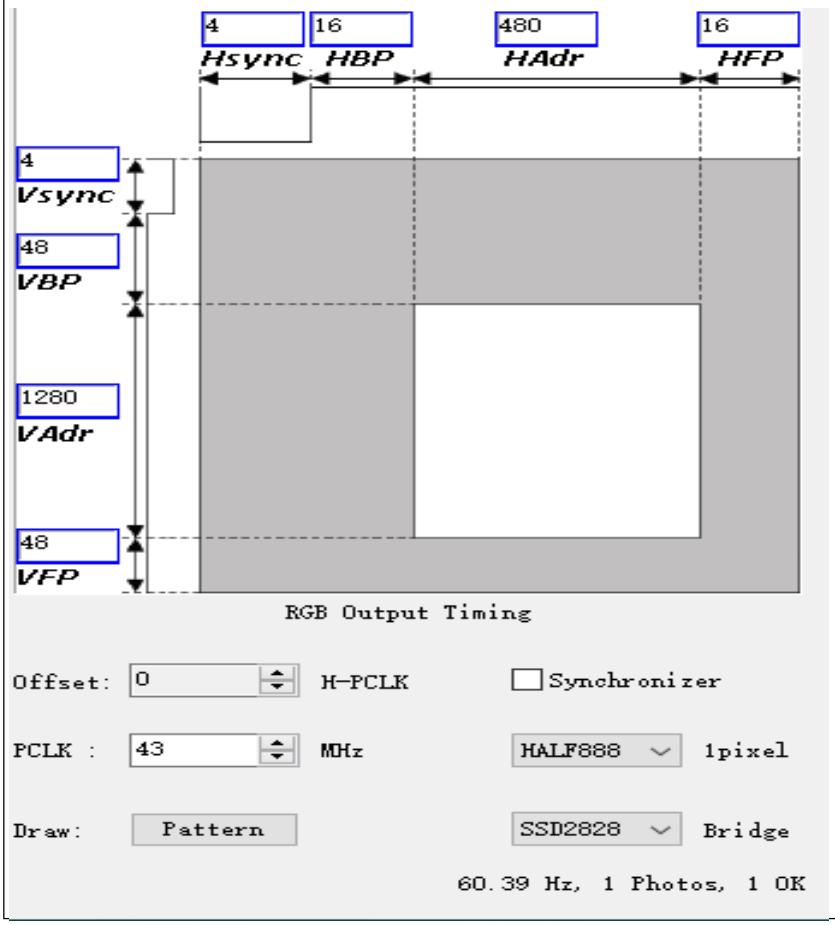


Figure 112: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

5.04.3 Timing for MIPI Characteristics.



6.0 Reliability test items

NO	Item	Conditions	Remark
1	High Temperature Storage	Ta=+80℃,48hrs	
2	Low Temperature Storage	Ta=-30℃,48hrs	
3	High Temperature Operation	Ta=+70℃,48hrs	
4	Low Temperature Operation	Ta=-20℃,48hrs	
5	High Temperature and High Humidity (operation)	Ta=+60℃,80%RH,48hrs	
6	Thermal Cycling Test (non operation)	-10℃(0.5hr)→+60℃(30min),100cycles	

Note: （1）All tests above are practiced at module type.
（2）There is no display function NG issue occurred, All the cosmetic specification is judged before the reliability stress.

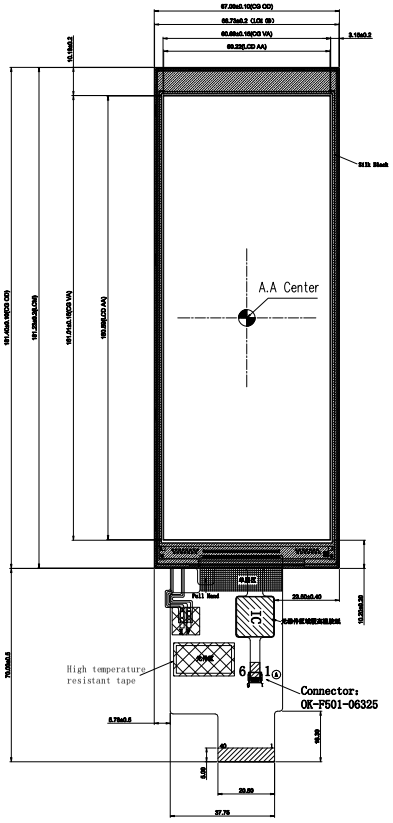
7. Mechanical Drawing

抗高温胶带
High temperature resistant tape

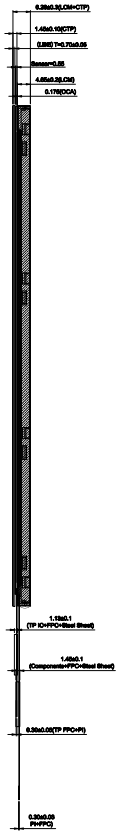
PI补强

钢片补强
Steel sheet

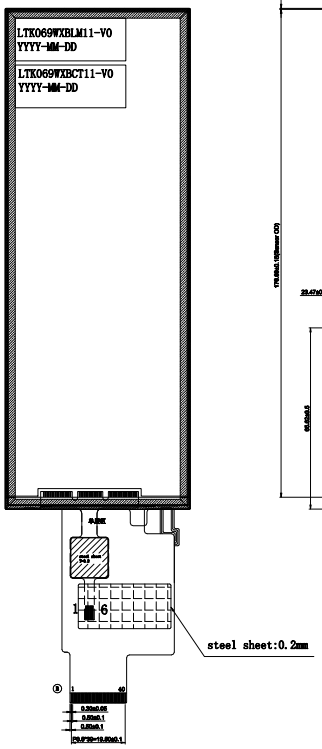
Front View

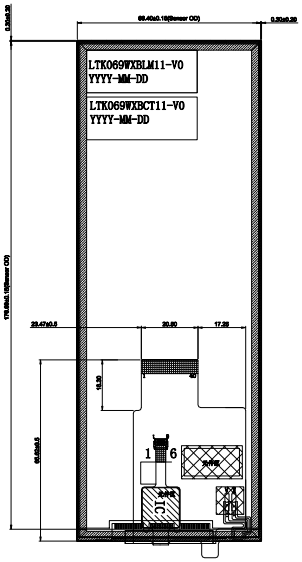


Side View



Back View





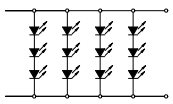
PIN	DESCRIPTION
1	GND
2	DOP
3	DON
4	GND
5	D1P
6	D1N
7	GND
8	CLKP
9	CLKN
10	GND
11	D2P
12	D2N
13	GND
14	D3P
15	D3N
16	GND
17	GND
18	VCC-1.8V
19	VCC-1.8V
20	CTP-VDD-3.3V
21	CTP-SDA-1.8V
22	CTP-SCL-1.8V
23	CTP-GND
24	RSTB
25	STBYB(GND)
26	CTP-INT
27	GND
28	K
29	K
30	GND
31	NC
32	GND
33	GND
34	NC
35	A
36	A
37	GND
38	VDD-3.3V
39	VDD-3.3V
40	CTP-RESET

B

PIN	NAME
1	VDD-3.3V
2	SDA-1.8V
3	SCL-1.8V
4	GND
5	INT
6	RESET

A

Notes:
1. Display : 6.86″, TFT
2. Resolution: 480xRGBx1280
3. LCD Viewing Direction: ALL
4. Driver IC: NV3051F
5. Display Mode: Normally Black
6. LCM+CTP Bringhtness: 350cd/㎡(TYP)
7. unmark Tolerance:±0.3
8. OPERATING TEMP:
9. STORAGE TEMP:
10. Requirements on Environmental Protection: ROHS



CURRENT IF=120mA,VF=9.9V (Reference)
3C*4B=12LED

skills requirement:
1. Structure: G+G
2. Transmittance: ≥85%
3. All unmarked tolerances: ±0.1mm
4. IC: GT9271
5. Tempering degree: 110g steel ball, drop from 30cm high without breaking, surface hardness test: 7H (pencil hardness test)
6. All materials comply with ROHS

REV	DESCRIPTION	DATE	NAME
3			
2			
1			
0	NEW	2023.02.15	IAN

LEADTEK COMPANY LIMITED

LEADTEK DISPLAY

SCALE:1/1	UNIT:mm	PAGE:1/1		Approve	Check	Drawn
Part No:	LTK069WXBCT11		VER:V0		JONA	IAN
Customer No:						

8.0 Packing form

8.1 TBD

9.0 GENERAL PRECAUTION

9.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

9.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

9.3 Breakage of LCD Panel

9.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
9.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.
9.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
9.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

9.4 Electric Shock

9.4.1. Disconnect power supply before handling LCD module.
9.4.2. Do not pull or fold the LED cable.
9.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

9.5 Absolute Maximum Ratings and Power Protection Circuit

9.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged. 9.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time. 11.5.3. It's recommended to employ protection circuit for power supply.

9.6 Operation

9.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.
9.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
9.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
9.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
9.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

9.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

9.8 Static Electricity

9.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

9.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

9.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

9.10 Disposal

When disposing LCD module, obey the local environmental regulations.