CMT453x Bluetooth® Low Energy wireless SoC Family

Datasheet

CMT453x series use 32-bit ARM Cortex-M0 core, support BLE 5.1 and SIG Mesh, and feature a frequency up to 64 MHz, 4.2 mA radio transmit current, 3.8 mA radio receive current, +6 dBm maximum transmitting power, and -96 dBm @BLE 1 Mbps RX sensitivity.

Key Features

- **CPU Core**
  - 32-bit ARM Cortex-M0 core
  - Frequency up to 64 MHz
- **Storage**
  - 256 KB Flash
  - 48 KB SRAM
- **Power Dissipation**
  - Radio receive current: 3.8 mA@3.3 V
  - Radio transmit current: 4.2 mA @0 dBm/3.3 V
  - Sleep mode (48 KB RAM retention): 1.4 μA@3 V
  - PD mode: 130 nA
- **RF Specification**
  - RX sensitivity: -96 dBm @BLE 1 Mbps
  - RX sensitivity: -93 dBm @BLE 2 Mbps
  - Power of programmable transmitter: up to +6 dBm
  - Single end antenna
- **Clock**
  - HSE: 32 MHz high speed external crystal
  - LSE: 32.768 KHz low speed external crystal
  - HSI: high speed internal RC 64 MHz
  - LSI: low speed internal RC 32 KHz
  - Support one clock output; different clock output can be configured; clock can be output after divided by four.
- **Reset**
  - Power-on/off/external pin reset
  - Watchdog reset
- **Communications Interface**
  - 2 × USART interfaces, with rate up to 4 Mbps (configurable as ISO7816, IrDA, LIN)
  - 1 × LPUART interface, featuring low-power dissipation, supporting communication rate up to 9,600 bps and low-power wakeup in Sleep mode
  - 2 × SPI interfaces, with rate up to 16 MHz, master/slave configurable, supporting I2S
  - 1 × I2C interface, with rate up to 1 MHz, master/slave configurable

- **Counter**
  - 1 × 16-bit advanced counter, supporting functions like input capture, output compare, PWM output, and quadrature encoder input; 4 independent channels, 3 of which support 6 complementary PWM outputs
  - 1 × 16-bit general-purpose counter, supporting functions like input capture, output compare, PWM output, and monopulse output, with 4 independent channels
  - 1 × 16-bit basic counter
  - 1 × 24-bit system timer
  - 1 × 7-bit window watchdog (WWDG)
  - 1 × 12-bit independent watchdog (IWDG)
- **Analog Interface**
  - 1 × 10-bit 1.33 Msps ADC (configurable as 16-bit 16 Ksps), supporting 5 external single-ended channels, 1 differential MIC channel, 2 internal channels
  - Built-in PGA up to 128x
  - MIC BIAS voltage, adjustable between 1.6 V and 2.3 V
- **21 × GPIO, supporting multiplexing**
- **1 × high speed 5-channel DMA controller**
- **1 × IR transmission controller, supporting all infrared remote control protocols**
- **1 × KEYSCAN module, where 8/10/13 GPIOs support 44/65/104 key functions respectively**
- **RTC real-time clock, supporting perpetual calendar (that can identify leap years), alarm events, and periodic wakeup**
- **Support hardware CRC16 and CRC32 operations**
- **Operating Conditions**
  - Operating voltage: 1.8 V~3.6 V
  - Operating temperature: -40°C~85°C
  - ESD: ±2 KV (HBM)
- **Package**
  - QFN32 (4 mm × 4 mm)
- **Ordering information**

Series	Part Number
CMT453x	CMT4531-EQR

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1 Overview

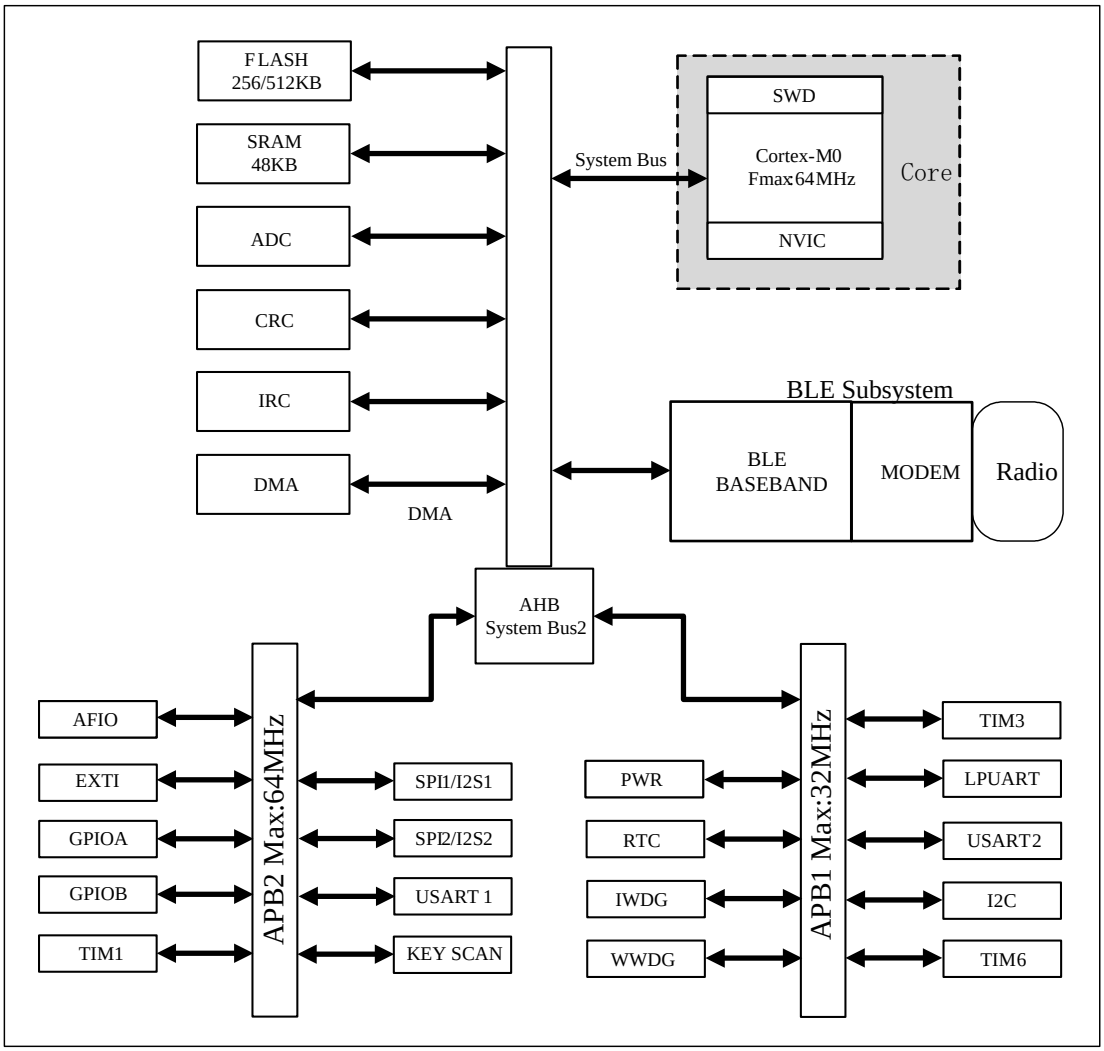
CMT453x Bluetooth® Low Energy wireless SoC Family is high performance, ultra-low power dissipation chips that support BLE 5.1. Equipped with 32-bit ARM Cortex®-M0 core, it features a frequency up to 64 MHz, 48 KB SRAM integrated on the chip, and 256 KB Flash.

Integrated with an advanced BLE 5.1 RF transceiver, it is compliant with the BLE 5.1 standard and provided with multiple modes including standard 1 Mbps BLE mode, enhanced 2 Mbps BLE mode, 125 kbps BLE remote mode (S8), and 500 kbps BLE remote mode (S2). In the 1 Mbps or 2 Mbps BLE mode, it supports AOA and AOD, RSSI, master/slave role, multi-connection, packet length expansion, KEYSCAN, IRC, 10-bit 1.33 Msps ADC (configurable as 16-bit 16 Ksps), analog MIC input, PGA, basic, universal and advanced timers, RTC, WWDG, IWDG, LPUART, USART, SPI, I2C, and other peripherals.

It is applicable to many application scenarios including Bluetooth KEY, OBU, data transmission module, Bluetooth voice remote controller, and smart home.

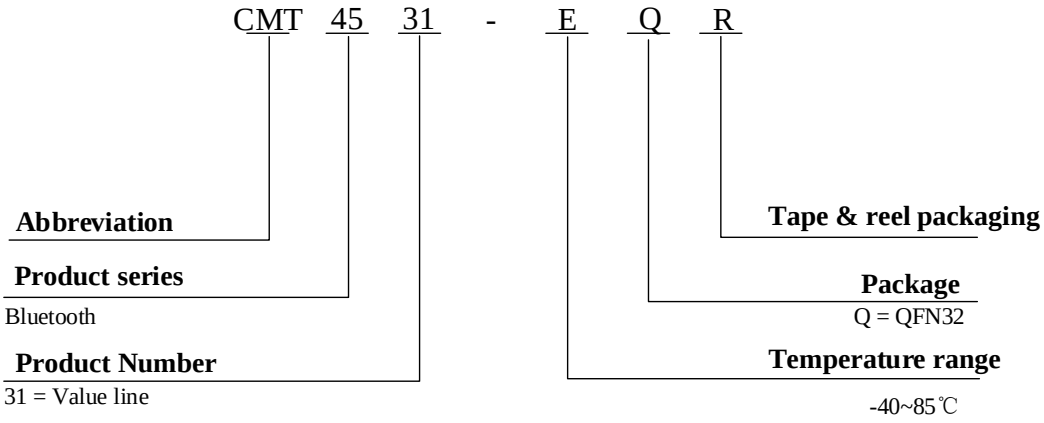
Figure 1-1 shows the block diagram of CMT453x series.

Figure 1-1 Block Diagram of CMT453x Series



1.1 Naming Rule

Figure 1-2 Structure of CMT453x Series Ordering Code



1.2 Device Schedule

Table 1-1 Resource Configuration of CMT453x Series

Model		CMT4531-EQR
Bluetooth Protocol		BLE5.1
Flash Capacity (KB)		256
SRAM Capacity (KB)		48
CPU Frequency		ARM Cortex-M0 @64MHz
Operating Environment		1.8 V~3.6 V/-40~85°C
Timer	Universal	1 pc (TIM3)
	Advanced	1 pc (TIM1)
	Basic	1 pc (TIM6)
	RTC	1 pcs (RTC)
Communication Interface	SPI	2 pcs (SPI1, SPI2)
	I2S	2 pcs (I2S1, I2S2)
	I2C	1 pc (I2C)
	USART	2 pcs (USART1, USART2)
	LPUART	1 pc (LPUART)
GPIO		21
DMA (channels)		1(5)
10-bit ADC (channels)		1(8)
KEYSCAN		8/10/13 GPIOs support 44/65/104 keys respectively
IRC		1 pc
CRC		CRC16/CRC32
Package		QFN32 (4 mm × 4 mm)

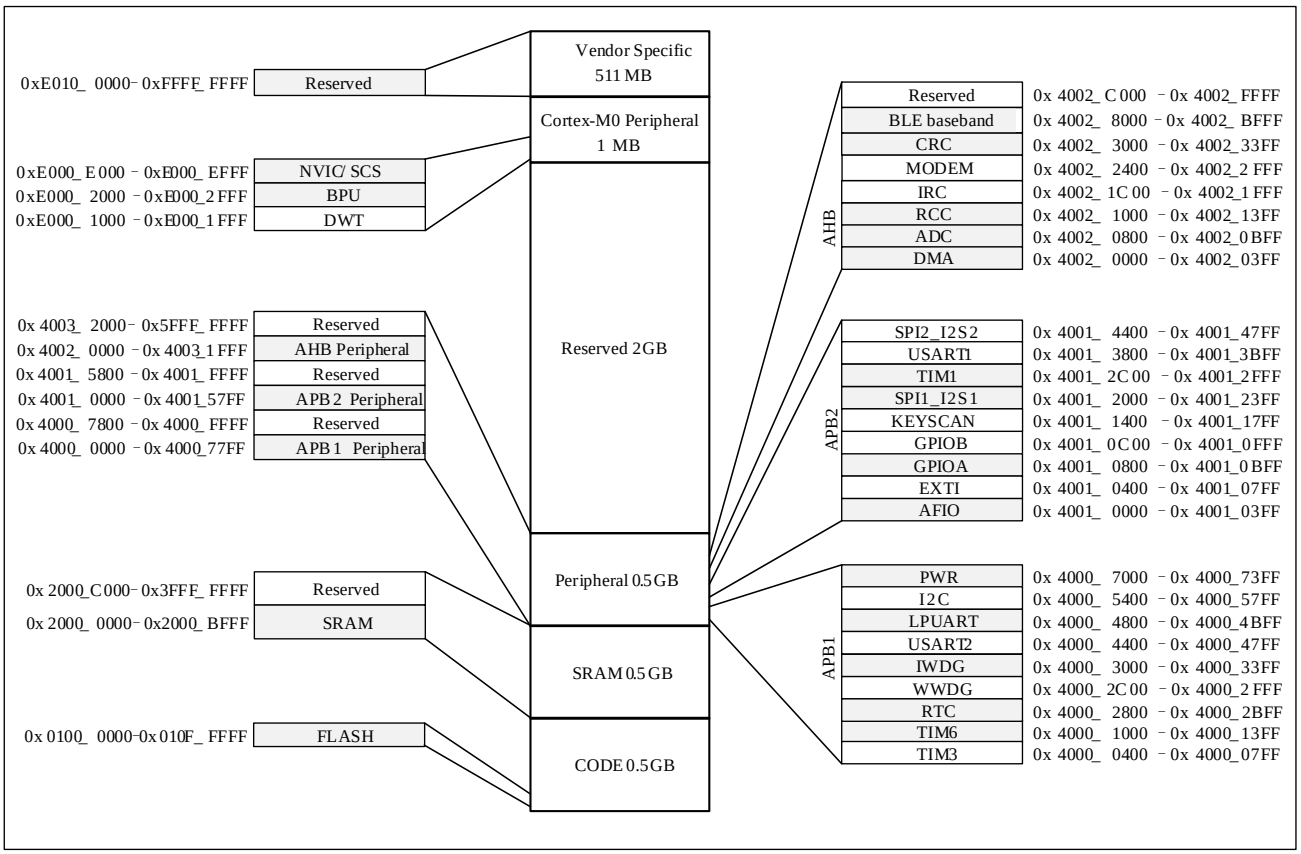
2 Production Features

2.1 Processor Core

CMT453x series are integrated with ARM Cortex®-M0 processors.

2.2 Memory

Figure 2-1 Memory Mapping



2.2.1 Flash

256 KB Flash, with up to 256 KB for program storage and the remaining space for data storage.

2.2.2 SRAM

48 KB SRAM, full retention in the Sleep mode

2.3 Low Power Modes

CMT453x series support four low power modes.

- Idle Mode

  Only the CPU stops running. All peripherals are working and can wake up the CPU in the event of any interrupt/event.

- Standby Mode

  The power supply works as usual. The CORE power domain is turned off. The BLE is available.

- Sleep Mode

  The high speed clock is switched off. The power supply runs in the low power mode. The CORE power domain and BLE are turned off.

- PD Mode

  All systems are shut down. Only WAKEUP IO and NRST can be woken up.

2.4 Clock System

Two high speed clocks:

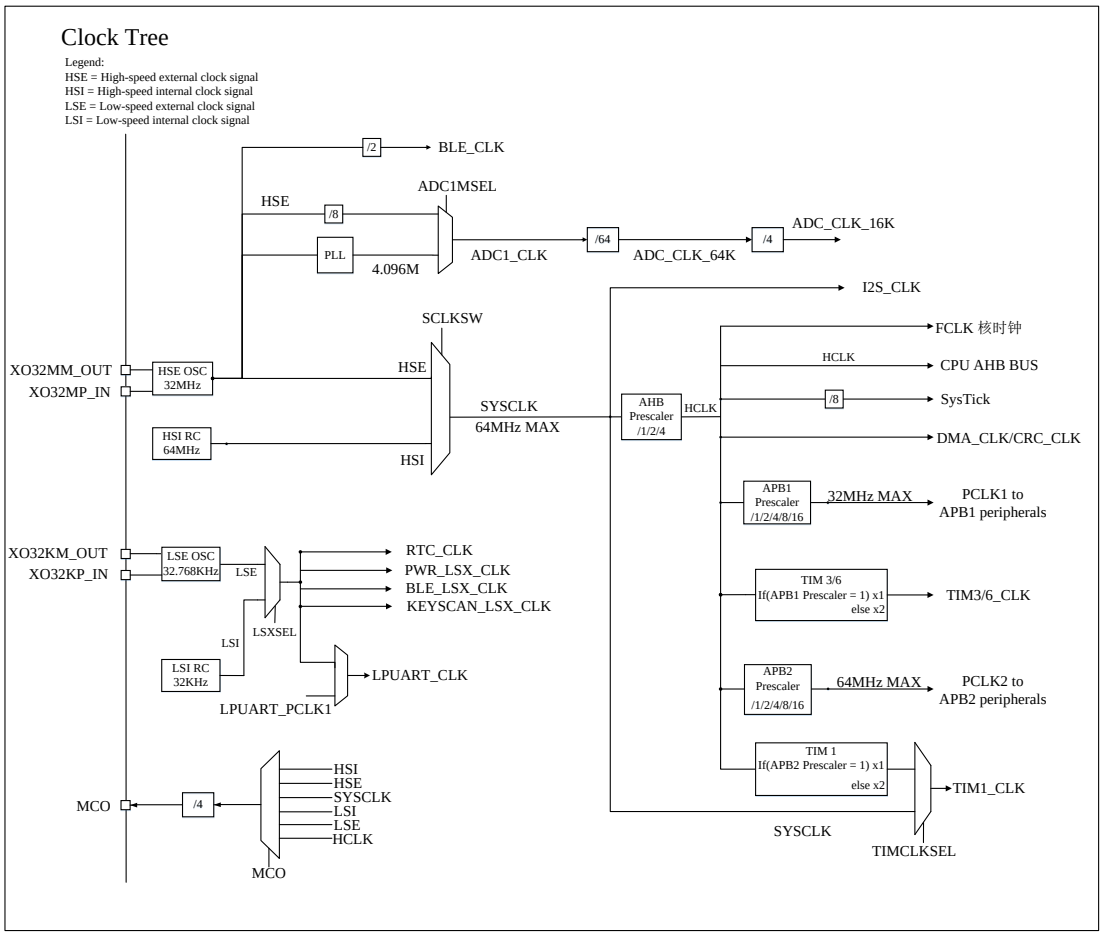
- HSI oscillator clock (64 MHz)
- HSE oscillator clock (32 MHz)

Two secondary clock sources:

- LSI oscillator clock (32 KHz)
- LSE oscillator clock (32.768 KHz)

After the system is powered on and reset, HSI and HSE are enabled and the system clock is set to HSI by default. LSI can be used to drive the IWDG. Both LSI and LSE can selectively drive RTC, KEYSCAN and LPUART through a program. Moreover, LSI/LSE can automatically wake up the system in the Idle /Standby/Sleep/PD mode. If not in use, either clock source can be turned on or off independently to optimize system power dissipation.

Figure 2-2 Clock Tree



2.5 General Purpose Input/Output (GPIO)

GPIO stands for general purpose input/output. AFIO stands for alternate-function input/output. A chip supports up to 21 GPIOs, which are divided into 2 groups (GPIOA/GPIOB). GPIOA has 7 ports and GPIOB has 14 ports. GPIO ports share pins with other multiplexed peripherals and can be flexibly configured as required. Each GPIO pin can be independently configured as an output, input, or multiplexed peripheral functional port, and configured with heavy current through capability.

Main features:

- GPIO ports can be configured through software to the following modes:
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Output open-drain
  - Output push-pull

  - Alternate function push-pull
  - Alternate function open-drain
- Separate bit setting or bit clearing function
- All I/O supports external interrupt
- All I/Os can be woken up from low power modes, with configurable rising or falling edge
- Eight EXTIs can wake up the Sleep mode and all I/O can be multiplexed as EXTI
- PB3 can wake up I/O from the PD mode
- Support remapping of AFIO through software
- Support GPIO locking mechanism and removal of locking status through resetting
- Each I/O port register bit is freely programmable, but it must be accessed as 32-bit words (16-bit half-word or 8-bit byte access is not allowed).

2.6 EXTI

The EXTI consists of 14 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured as an event or interrupt and the corresponding trigger event (rising edge or falling edge or both). Each line can also be masked independently. A pending register maintains the status line of the interrupt request. This request can be cleared by writing a '1' in the corresponding bit of the pending register.

2.7 DMA

DMA is integrated with one universal 5-channel DMA controller to manage data transfer from memory to memory, from peripheral to memory and from memory to peripheral;

Each channel has a dedicated hardware DMA request logic, and can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.

DMA is applicable to main peripherals including SPI, I2S, I2C, USART, ADC, and basic, universal and advanced control TIMx.

2.8 CRC

CRC is integrated with CRC32 and CRC16 to get any CRC calculation based on a fixed polynomial. Among numerous applications, CRC-based technologies are used to verify the consistency of data transmission or storage. Within the scope specified in EN/IEC 60335-1, CRC provides a means of detecting flash memory errors, and can be used to compute software signatures in real time and compare them with the signatures generated when linking and generating the software.

Main features:

- CRC16: supports the polynomial X16+X15+X2+X0
- CRC16 computing time: one AHB clock period (HCLK)
- CRC32: supports the polynomial $X_{32} + X_{26} + X_{23} + X_{22} + X_{16} + X_{12} + X_{11} + X_{10} + X_8 + X_7 + X_5 + X_4 + X_2 + X + 1$

- CRC32 computing time: four AHB clock periods (HCLK)
- Configurable initial value of cyclic redundancy computation
- DMA available

2.9 Timer and Watchdog

1 × advanced timer, 1 × general-purpose timer, 1 × basic timer, 2 × watchdog timer, and 1 × system tick timer.

2.9.1 Basic Timer (TIM6)

TIM6 contains a 16-bit auto-loading counter driven by a programmable prescaler. It provides a time baseline for general-purpose timers.

Main features:

- 16-bit automatic reloading accumulating counter
- 16-bit programmable (can be modified in real time) prescaler, used for frequency demultiplication of the input clock by a coefficient ranging from 1 to 65536
- Generate an interrupt/DMA request when an event is updated (counter overflow)

2.9.2 General-purpose Timer (TIM3)

A general-purpose timer consists of one 16-bit countup/countdown auto-loading counter, one 16-bit prescaler, and 4 independent channels, each for input capture (pulse width measurement), output compare, PWM, and monopulse output;

Main features:

- 16-bit countup, countdown, or countup/countdown auto-loading counter
- 16-bit programmable (can be modified in real time) prescaler; the frequency demultiplication coefficient of counter's clock frequency can be any numerical value ranging from 1 to 65536
- Four independent channels:
  - Input capture
  - Output compare
  - PWM generation (edge or middle alignment)
  - Monopulse output
- A synchronous circuit that uses an external signal control timer and allows interconnection of multiple timers
- Generate interrupt/DMA in the case of the following events:
  - Update: up/down counter overflow, counter initialization (software-based trigger or internal trigger)
  - Trigger events (startup, shutdown, and initialization of counter, or internally triggered counting)
  - Input capture
  - Output compare

- Support the incremental (quadrature) encoders for positioning and Hall sensor circuits
- Use trigger input signal as the input of external clock, or perform periodic current management

2.9.3 Advanced Timer (TIM1)

TIM1 consists of a 16-bit auto-loading counter driven by a programmable prescaler. It provides multiple functions, including measuring the pulse width of the input signal (input capture) or generating output waveform (such as output compare, PWM, and complementary PWM outputs with dead time in between). Using the timer's prescaler and RCC clock control prescaler can adjust the pulse width and waveform period from several microseconds to several milliseconds.

Main features:

- 16-bit countup, countdown, or countup/countdown auto-loading counter
- 16-bit programmable (can be modified in real time) prescaler; the frequency demultiplication coefficient of counter's clock frequency can be any numerical value ranging from 1 to 65536
- Use up to 64 MHz as timer's input clock
- Up to four independent channels:
  - Input capture
  - Output compare
  - PWM generation (edge or middle alignment)
  - Monopulse output
- Trigger time points can be configured by software in the entire PWM cycle
- Complementary output with programmable dead time
- A synchronous circuit that uses an external signal control timer or allows interconnection of multiple timers
- A repetitive counter to update the timer registers only after a given number of cycles of the counter
- Break input signal can put the timer's output signals in a reset state or in a known state
- Generate interrupt/DMA in the case of the following events:
  - Update: up/down counter overflow, counter initialization (software-based trigger or internal/external trigger);
  - Trigger events (startup, shutdown, and initialization of counter, or internally/externally triggered counting);
  - Input capture;
  - Output compare;
  - Break signal input;
- Support the incremental (quadrature) encoders for positioning and Hall sensor circuits;
- Use trigger input signal as the input of external clock, or perform periodic current management

In the debug mode, a counter can be frozen and PWM outputs are disabled, cutting off the switches controlled by those outputs. The advanced timer has many functions similar to and the same internal structure as that of the standard

TIM timer. Therefore, it can work with the TIM timer through the timer's link function to provide synchronization or event link function.

2.9.4 System Tick Timer (Systick)

This timer is tailored to a real-time operating system and can also be used as a standard downcounter. It has the following features:

- 24-bit downcounter
- Automatic re-loading function
- Generate a maskable system interrupt when the counter reaches zero
- Programmable clock source

2.9.5 Watchdog Timer (WDG)

It supports both independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs ensure higher security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The IWDG is based on a 12-bit downcounter and an 8-bit prescaler, and is driven by a separate, low speed RC oscillator. It still can work even if the master clock fails and operate in the Sleep mode. Once activated, the IWDG will generate a reset signal when the counter reaches 0x000 if the watchdog's counter is not cleared within a given time period. Moreover, it can also be used to reset the entire system in the event of an application error, or as a free timer to provide timeout management for applications.

Window Watchdog (WWDG)

The WWDG is typically used to monitor software failures caused by deviation of an application from the normal running sequence due to external disturbances or unforeseen logical conditions. Unless the value of a downcounter is refreshed before the T6 bit reaches zero, the watchdog circuit will generate a chip reset when the preset time cycle is reached. A chip reset is also generated if the value of a 7-bit downcounter (in the control register) is refreshed before the downcounter reaches the value of the window register. This indicates that the downcounter needs to be refreshed in a finite time window.

Main features:

- WWDG is driven by the clock obtained after frequency demultiplication of APB1 clock
- Programmable free-running downcounter
- Conditional reset
- A reset occurs when the value of the downcounter is less than 0x40 if the watchdog is enabled;
- A reset occurs when the downcounter is reloaded outside the window if the watchdog is enabled;
- If the watchdog is enabled and interrupt is allowed, an EWI is generated when the value of the downcounter reaches 0x40, and it can be used to reload the counter to avoid resetting WWDG.

2.10 ADC

Support 10-bit 1.33 Msps ADC (configurable as 16-bit 16 Ksps), single-ended or differential AMIC, and built-in

PGA with a gain up to 42 dB.

Provide adjustable (1.6–2.3 V) MIC BIAS voltage for MIC.

Up to 8 channels, including 5 external single-ended channels, 1 differential MIC channel, and 2 internal channels. Two internal channels are VCC detection channel and temperature sensor channel. For 5 external channels, the detection range of channels 1 (PB10) and 2 (PB9) is 0V-1V, and that of channels 3 (PB8), 4 (PB7), and 5 (PB6) is 0V-3.6V. the input voltage of channels 3 (PB8), 4 (PB7), and 5 (PB6) <=VCC+300 mV.

In the audio mode, using the built-in PGA and microphone bias, MIC signals are amplified by the PGA, and then converted to digital signals by an ADC. After the audio input control (low-pass decimation filter and optional energy and zero-cross detection), the audio data is stored in the system RAM through DMA. Finally, 16-bit 16 kHz audio signal format data is output.

Main features:

- Support AMIC input, with adjustable microphone bias
- PGA supports single-ended or differential input and adjustable gain
- Support one ADC, which can measure 5 external single-ended channels, 1 differential MIC channel, and 2 internal channels (input channels are optional)
- Support two internal channels, including TempSensor and VCC
- 10-bit 1.33 Msps ADC (configurable as 16-bit 16 Ksps)
- Support digital decimation filter to 16-bit and noise filter
- Support single and continuous conversion modes
- A DMA request can be generated during channel switching
- The analog watchdog feature allows an application to detect whether the input PB10 voltage exceeds a user-defined high/low threshold
- An interrupt occurs at the end of switching or in the case of an analog watchdog event
- In the audio mode, the filter's output data is stored in a 16-bit data register, and in the general mode, the data is right-aligned and stored in a 16-bit data register
- In the audio mode, data is output in 16-bit 16 Ksps signed mono PCM format, and in the general mode, data is output in 10-bit 1.33 Msps unsigned format

2.11 I2C Bus Interface (I2C)

The I2C bus interface provides multi-master function that controls all the I2C bus specific sequences, protocol, arbitration and timing. It supports multiple communication rate modes (up to 1 MHz), DMA operations, and SMBus 2.0. The I2C module suits multiple purposes, including CRC code generation and verification, SMBus (System Management Bus), and PMBus (Power Management Bus).

Main features:

- Multi-master function: The module can be either a master device or a slave device
- Functions of I2C master device

  - Generate a clock
  - Generate start and stop signals
- Functions of I2C slave device
  - Programmable address detection
  - The I2C interface supports 7-bit or 10-bit addressing, and dual-slave address responsiveness in 7-bit slave mode
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addresses; broadcast call
- Support different communication rates
  - Standard rate (up to 100 kHz)
  - Rapid (up to 400 kHz)
  - Rapid+(up to 1 MHz)
- Support multiple status flags
  - Transmitter/receiver mode flag
  - End of byte transmission flag
  - I2C bus busy flag
- Support multiple error flags
  - Arbitration is lost in the master mode
  - Acknowledgement (ACK) error after address/data transmission
  - Detection of a start or stop condition of misplacement
  - Overflow or underflow when the clock stretching function is disabled
- One interrupt vector:
  - Event interrupt and error interrupt share an interrupt vector
- Optional clock stretching function
- DMA with single-byte cache
- Generation or verification of configurable PEC
  - The PEC value can be transmitted as the last byte in the transmitter mode
  - PEC for the last received byte
- Compatible with SMBus 2.0
  - 25 ms clock low timeout delay
  - 10 ms cumulative time for low clock extension for master device

  - 25 ms cumulative time for low clock extension for slave device
  - Generation or verification of hardware PEC with ACK control
  - Support address resolution protocol (ARP)
- Compatible with SMBus

2.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The USART is integrated with 3 serial receiver/transmitter interfaces, including USART1, USART2, and LPUART. USART1 and USART2 interfaces support synchronous/asynchronous communication, IrDA SIR ENDEC transmission coding and decoding, multiprocessor communication mode, single-wire half-duplex communication mode, and LIN master/slave function.

USART1 and USART2 interfaces also support the CTS and RTS hardware flow control, and the single-wire mode such as the ISO7816 smart card standard. DMA is available to both interfaces.

Main features:

- Full-duplex asynchronous communication
- Single-wire half-duplex communication
- NRZ standard format
- Fractional baud rate generator system – a common programmable transmitting and receiving baud rate up to 4 Mbits/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bits – support for 1 or 2 stop bits
- LIN master is capable of sending synchronous break and LIN slave is capable of detecting the break: 13-bit break is generated and 10/11-bit break is detected when USART hardware is configured to LIN
- Transmitter clock output for synchronous transmission
- IRDA SIR encoder-decoder: Support for 3/16 bit duration in normal mode
- Smart card emulation capability
  - The smart card interface supports the asynchronous smart card protocol as defined in the ISO7816-3 standard
  - 0.5 and 1.5 stop bits for smart card
- Single-wire half-duplex communication
- Configurable multi-buffer communication using DMA – buffering of received/transmitted bytes in SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Detection flags

- Receive buffer full
- Transmit buffer empty
- End of transmission flags

- Checking control
  - Send check bits
  - Check the received data
- Four error detection flags
  - Overflow error
  - Noise error
  - Frame error
  - Checking error
- Ten USART interrupt sources with flags
  - CTS change
  - LIN break detection
  - Transmit data register empty
  - Transmission completed
  - Receive data register full
  - Detected idle bus
  - Overflow error
  - Frame error
  - Noise error
  - Checking error
- Multiprocessor communication – If addresses do not match, enable the silent mode
- Wake up from silent mode (by detecting idle bus or address flag)
- Two ways to wake up the receiver: address bit (MSB, 9th bit), bus idle
- Mode configuration:

Communication mode	USART1	USART2	LPUART
Asynchronous mode	Supported	Supported	Supported
Hardware flow control	Supported	Supported	Supported

Multi-buffer communication (DMA)	Supported	Supported	Supported
Multiprocessor communication	Supported	Supported	Not supported
Synchronous	Supported	Supported	Not supported
Single-wire half-duplex	Supported	Supported	Not supported
Smart card	Supported	Supported	Not supported
IrDA	Supported	Supported	Not supported
LIN	Supported	Supported	Not supported

2.13 Serial Peripheral Interface (SPI)

Two SPIs are provided, allowing half-duplex/full-duplex, synchronous, and serial communication between chips and peripherals. SPI can be configured to operate in the master mode and provide a communication clock (SCK) for the external slave device. Moreover, SPI can also work in the multi-master mode and use the CRC based reliable communication.

Main features:

- Full-duplex synchronous transmission
- Double-wire simplex synchronous transmission with/without the third two-way data cable
- 8-bit or 16-bit transmission frame format
- Support master or slave mode
- Support multi-master mode
- Rapid communication between master and slave modes
- NSS management can be performed by software or hardware in the master or slave mode: dynamic switching of master/slave mode
- Programmable clock polarity and phase
- Programmable data sequence, with MSB or LSB in the first order
- Dedicated transmit and receive flags to trigger interrupt
- SPI bus busy flag
- Support reliable communication based on hardware CRC
  - The CRC value can be transmitted as the last byte in the transmitter mode
  - Automatic CRC for the last received byte in the full-duplex mode
- Master mode failure, overload, and CRC error flags that trigger interrupt
- Single-byte transmitting and receiving buffers with DMA feature: Generate transmission and receiving

requests

- Maximum interface rate: 16 Mbps

2.14 Serial Audio Port (I2S)

I2S, a 3-pin synchronous serial interface communication protocol, operates in master or slave mode, supports an audio sample frequencies ranging from 8 kHz to 96 kHz, and can be configured as 16/24/32-bit transmission or as input or output channel. It is compatible with four audio standards, namely, the Philips' I2S standard, the MSB and LSB alignment standards, and the PCM standard.

It works in both master and slave modes in half-duplex communication. When it works as the master device, it provides clock signals to external slave devices through the interface.

Main features:

- Half-duplex communication (either transmitting or receiving only at a time)
- Master or slave operation
- 8-bit linear programmable prescaler, helping obtain an accurate audio sample frequency (8 kHz~96 kHz)
- 16/24/32-bit data format
- 16-bit (16-bit data frame) or 32-bit (16/24/32-bit data frame) fixed packet frame for audio channel
- Programmable clock polarity (stable state)
- Underflow flag bit in the slave transmitter mode and overflow flag bit in the master/slave receiving mode
- 16-bit data register to transmit and receive, one in each end of the channel
- Supported I2S protocols
  - Philips' I2S standard
  - MSB alignment standard (left-justified)
  - LSB alignment standard (right-justified)
  - PCM standard (a 16-bit channel frame with long or short frame synchronization; or extension from a 16-bit data frame to a 32-bit channel frame)
- Data sequence: MSB is always in the first order
- DMA is available to both transmitter and receiver

2.15 Real Time Clock (RTC)

RTC has a set of BCD timers/counters that count independently continuously. In the corresponding software configuration, RTC can provide the calendar function. RTC also has a programmable alarm clock interrupt.

The two 32-bit registers contain the subsecond, second, minute, hour (in 12- or 24-hour format), day of the week, day (day of the month), month, and year data in decimal format (BCD).

The subsecond value is provided by a separate 32-bit register in binary format. The other 32-bit register contains programmable second, minute, hour, day of the week, day, month, and year data.

RTC has the feature of automatic wakeup in the low power mode.

2.16 Infrared Controller (IRC)

The infrared controller can generate different infrared protocol signals by configuring different types of coding through software, and supports the software-based infrared self-learning function.

Main features:

- Carrier frequency range: 30 kHz~60 kHz
- Support pulse width coding and pulse spacing coding
- Support Manchester coding
- Support carrier-free mode
- Support any combination of Mark code and Space code
- Provide 16 (depth) × 21-bit (width) Code FIFO for storing coded commands
- Support repeatedly sending commands
- Generate interrupt upon the end of transmission

2.17 Automatic Key Scanning (KEYSCAN)

Support 8/10/13 IO ports that support 44/65/104 keys respectively.

Support configurable key jitter elimination.

Support automatic scanning, software scanning, low-power dissipation scanning modes.

- Automatic mode: Scanning performs at the configured fixed time interval
- Low power mode: A round of scanning (three times) is performed after the detection key is pressed
- Software mode: Scanning is triggered by the software

2.18 Serial SWD Debugging Interface (SWD)

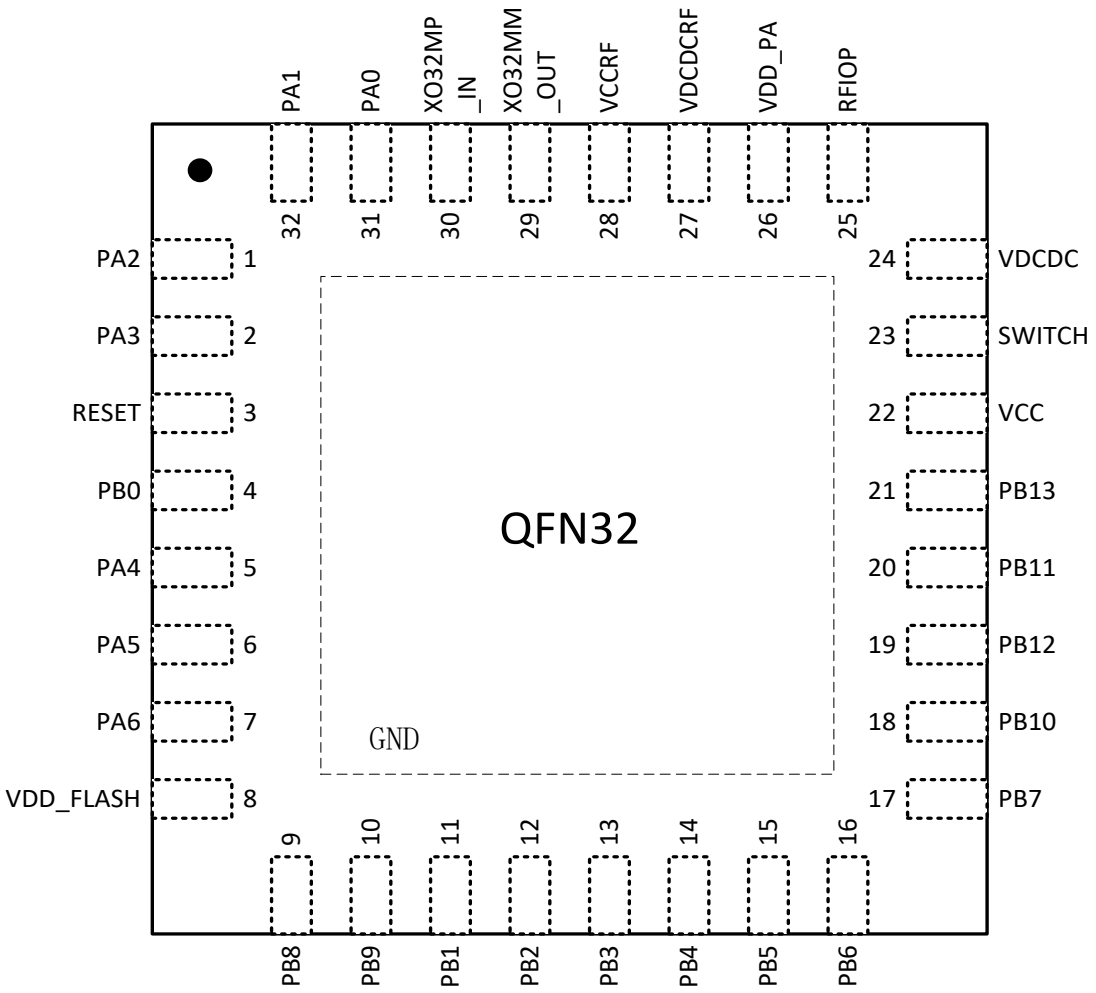
A SWJ-DP interface with built-in ARM, it integrates JTAG and serial single-wire debugging interfaces, and supports connecting to the serial single-wire debugging interface or JTAG interface. The TMS and TCK signals of JTAG share pins with SWDIO and SWCLK respectively.

3 Definition and Description

3.1 Device Pinout

3.1.1 QFN32

Figure 3-1 QFN32 Pin Distribution of CMT453x Series



3.2 Definition of Pin Multiplexing

Table 3-1 Definition of Pin

Pin No. (QFN32)	Pin Name (Default Function)	Type	Alternate Function	Function Description
1	PA2	I/O	SPI1_MOSI(I2S1_SD) KEY3	
2	PA3	I/O	SPI1_MISO(I2S1_MCK) KEY4	
3	RESET	AIO		
4	PB0	I/O	TIM1_CH1 SPI2_NSS(I2S2_WS) USART1_RTS LPUART_RTS KEY11	
5	PA4 (SWDCLK)	I/O	TIM1_CH3N USART1_TXD(7816_TX1) KEY9	
6	PA5 (SWDIO)	I/O	TIM1_ETR USART1_RXD(7816_RST1) KEY10	
7	PA6	I/O	TIM1_BKIN USART2_TXD USART1_CK(7816_CLK1) KEY5	
8	VDD_FLASH	S		External 2.2 uF capacitor
9	PB8 (XO32KP_IN)	I/O	TIM1_CH1 IIC_SDA USART1_RTS KEY7	ADC3
10	PB9 (XO32KM_OUT)	I/O	TIM1_CH2 IIC_SCL USART1_CTS KEY8	ADC2
11	PB1	I/O	TIM1_CH2 SPI2_CLK(I2S2_CLK) USART1_CTS LPUART_TXD KEY12 ANT_SW4	
12	PB2	I/O	TIM1_CH3 SPI2_MOSI	

			LPUART_RXD KEY13 ANT_SW5	
13	PB3	I/O	TIM1_CH4 SPI2_MISO(I2S_MCK) LPUART_CTS PA_LDO_EN ANT_SW1	WAKEUP
14	PB4	I/O	SPI2_CLK(I2S2_CLK) TIM3_CH1(IRC_TX) USART2_TXD(7816_TX2) ANT_SW6	
15	PB5	I/O	SPI2_MISO(I2S2_MCK) TIM3_CH2(IRC_RX) USART2_RXD(7816_RST2) RCC_MCO ANT_SW7	
16	PB6	I/O	SPI2_MOSI(I2S2_SD) TIM3_CH3 IIC_SDA USART1_TXD SWDCLK ANT_SW2	ADC5
17	PB7	I/O	SPI2_NSS(I2S2_WS) TIM3_CH4 IIC_SCL USART1_RXD SWDIO ANT_SW3	ADC4
18	PB10	I/O	TIM1_CH3 LPUART_RTS USART2_RXD IIC_SMBA KEY6	ADC1
19	PB12	I/O	TIM1_CH1N LPUART_TXD USART2_CTS	AMIC_BIAS
20	PB11	I/O	TIM1_CH4 LPUART_RXD USART2_RTS IIC_SMBA	AMIC_N
21	PB13	I/O	TIM1_CH2N LPUART_CTS USART2_CK	AMIC_P

22	VCC	S		Power supply for chip
23	SWITCH	S		DCDC external Interface
24	VDCDC	S		DCDC output
25	RFIOP	AIO		Antenna port
26	VDD_PA	S		PA power supply
27	VDCDCRF	S		DCDC output, connecting to VDCDC
28	VCCRF	S		Power supply for chip
29	XO32MM_OUT	AIO		External 32 MHz crystal
30	XO32MP_IN	AIO		External 32 MHz crystal
31	PA0	I/O	SPI1_NSS(I2S1_WS) KEY1	
32	PA1	I/O	SPI1_CLK(I2S1_CLK) KEY 2	
33	GND	S		Ground

I = input, O = output, S = power supply, AIO = analog IO

Upon resetting, the I/O port is configured to the analog input mode. But the following signals are not applicable:

- Input pull-up mode for NRST by default
- PA4: SWCLK under the input pull-down mode
- PA5: SWDIO under the input pull-up mode

4 Electrical Characteristics

4.1 Test Condition

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and Maximum

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by testing 100% of the product at ambient temperature T_A=25°C and T_A=T_{Amax} (T_{Amax} matches the specified temperature range) on the production line.

The annotations listed below each table are the data obtained through laboratory tests, design simulations and/or process characteristics, and will not be tested on the production line. On the basis of laboratory tests, the minimums and maximums are obtained by taking the average of the samples tested and adding to or subtracting from it three times the standard deviation (average ±3∑).

4.1.2 Typical Values

Unless otherwise specified, the typical data is based on T_A=25°C and VCC=3.3 V (1.8V≤VCC≤3.6 V). Such data is used for guiding the design only and is not tested.

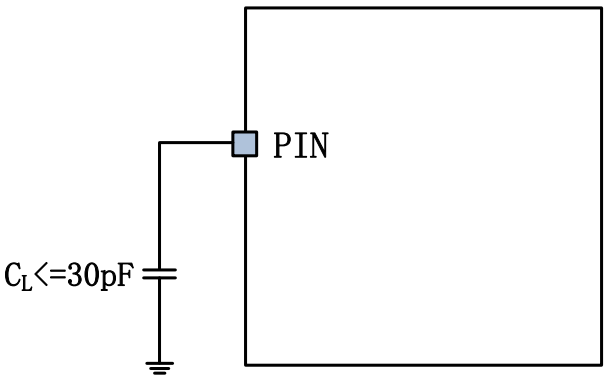
4.1.3 Typical Curve

Unless otherwise specified, the typical curve is used for guiding the design only and is not tested.

4.1.4 Load Capacitance

Figure 4-1 shows the load conditions for measuring pin parameters.

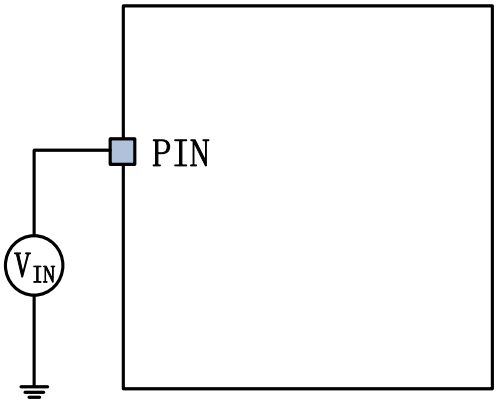
Figure 4-1 Load Conditions for Pins



4.1.5 Input Voltage of Pin

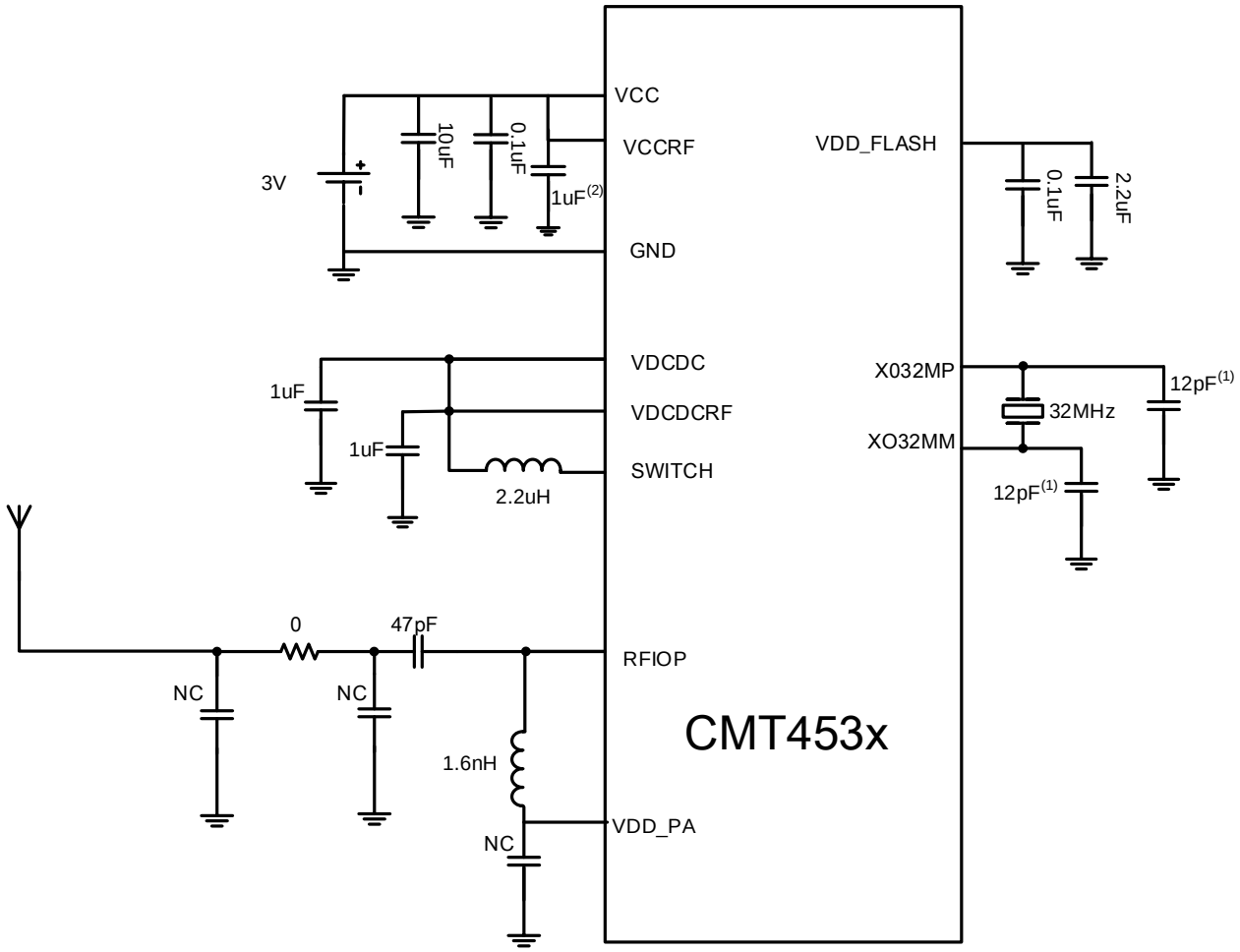
Figure 4-2 shows how to measure the input voltage of a pin.

Figure 4-2 Input Voltage of Pin

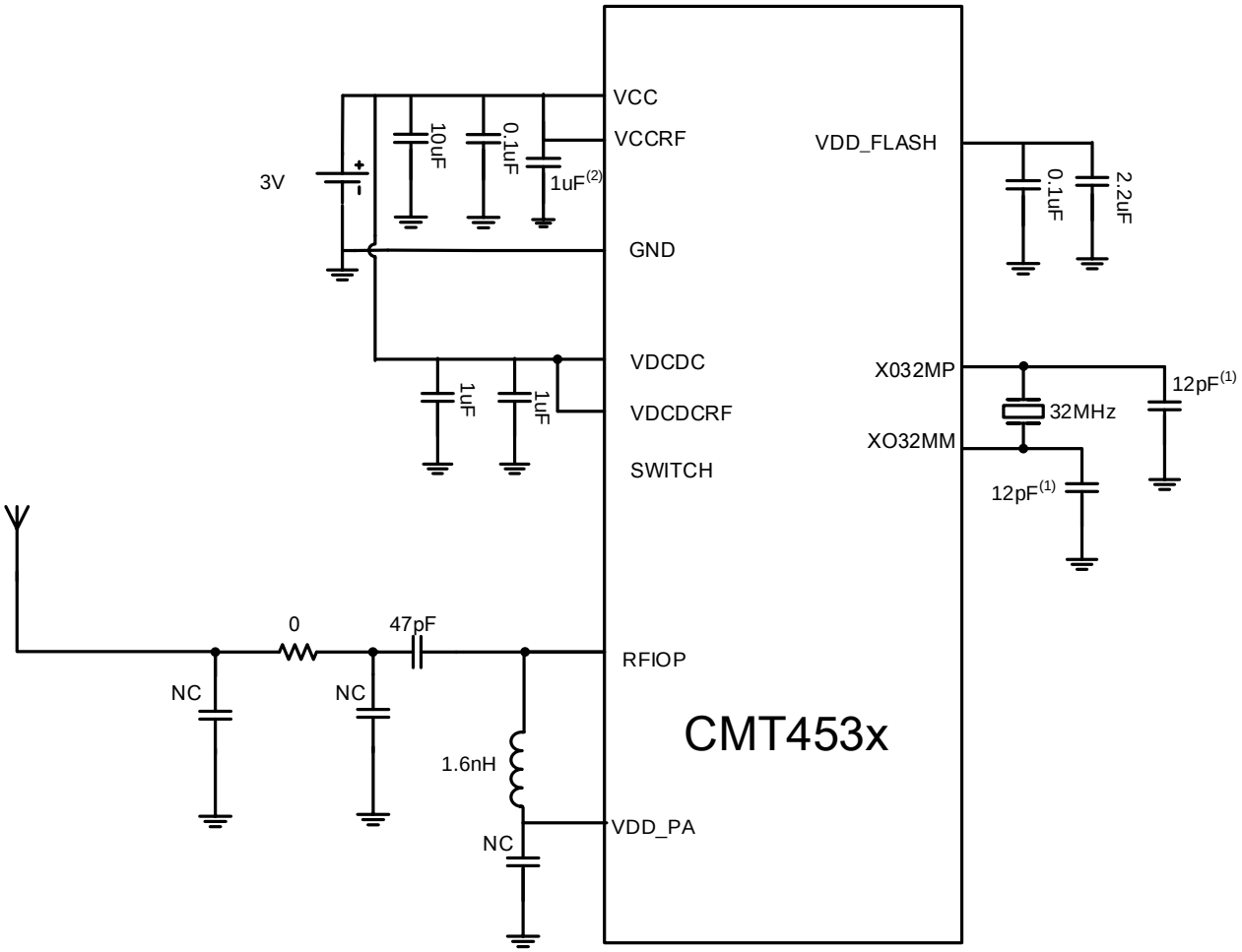


4.1.6 Power Supply Plan

Figure 4-3 Power Supply Plan



(a) VDCDC/VDCDCRF uses the internal DCDC power supply



(b) VDCDC/VDCDCRF uses the external power supply

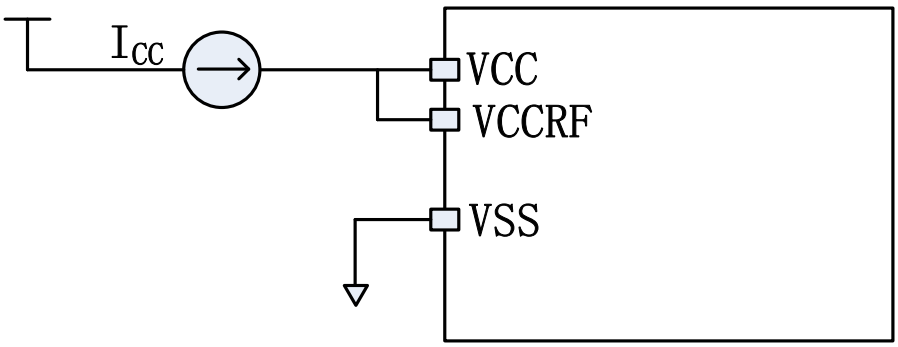
(1)The load capacitance C_L required by different crystals or resonators is usually different, refer to section 4.3.6 for details.

(2)In the case of low ripple requirements, the 1uF capacitor can be used without soldering.

(3) It is recommended to add TVS at the power supply pin as well as the antenna port for protection against ESD, and the junction capacitance of the TVS at the antenna port should not exceed 0.3pF.

4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Plan



4.2 Absolute Maximum Rating

The load applied to the device in excess of the value given in the "absolute maximum rating" tables (Tables 4-1, 4-2, and 4-3) may cause permanent damage to the device. The maximum allowable load is given here, but it does not mean that the functions of the device work well under these conditions. The device reliability will be affected if the device works at the maximum conditions for a long time.

Table 4-1 Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
VCC-VSS	External main supply voltage (including VCCRF and VCC)(1)	-0.3	3.6	V
V_{IN}	Input voltage on other pins(2)	VSS-0.3	VCC+0.3	
$V_{ESD(HBM)}$	Electrostatic discharge (ESD) voltage (human body model)	See Section 4.3.10		

(1) All power supply (VCC, VCCRF) and ground (VSS) pins must be connected to an external power supply system within the permissible range.

(2) $I_{INJ(PIN)}$ must not exceed its limit (see Table 4-2), ensuring that V_{IN} does not exceed its maximum. If impossible, you need to guarantee that the external limit $I_{INJ(PIN)}$ does not exceed its maximum. When V_{IN}<VSS, there is a reverse injection current.

Table 4-2 Current Characteristics

Symbol	Description	Maximum (1)	Unit
I_{VCC}	Total current (supply current) passing through VCC/VCCRF power cable(1)	150	mA
I_{VSS}	Total current (output current) passing through VSS ground wire(1)	150	
I_{IO}	Output sink current of any I/O and control pins	12	
	Output current of any I/O and control pins	-12	
$I_{INJ(PIN)}$(2)(3)	Injection current of NRST pin	+/-5	
	Injection current of HSE's OSC_IN pin and LSE's OSC_IN pin	+/-5	
	Injection current of other pins(4)	+/-12	
$\sum I_{INJ(PIN)}$(2)	Total injection current of all I/O and control pins(4)	+/-150	

(1) All power supply (VCC, VCCRF) and ground (VSS) pins must be connected to an external power supply system within the permissible range.

(2) $I_{INJ(PIN)}$ must not exceed its limit, ensuring that V_{IN} does not exceed its maximum. If impossible, you need to guarantee that the external limit $I_{INJ(PIN)}$ does not exceed its maximum.

(3) When several I/O ports have injection current simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of immediate absolute values of forward injection current and reverse injection current.

Table 4-3 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-40 to + 125	°C
T_J	Maximum junction temperature	105	°C
MSL(1)	Moisture Sensitivity Level	3	

(1) Generally follows Industry Standards IPC/JEDEC J-STD-020 and J-STD-033 to determine the moisture sensitivity level and corresponding floor life time.

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{HCLK}	Internal AHB clock frequency			64	MHz
f_{PCLK1}	Internal APB1 clock frequency			32	
f_{PCLK2}	Internal APB2 clock frequency			64	
VCC	Standard operating voltage		1.8	3.6	V
VCCRF	Analog operating voltage		1.8	3.6	V
T_A	Ambient temperature		-40	85	°C
T_J	Junction temperature range		-40	105	°C

4.3.2 Power-on and Power-off Operating Conditions

The parameters in the following table are obtained by testing at the ambient temperature listed in Table 4-4.

Table 4-5 Power-on and Power-off Operating Conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
T_{VCC}	VCC rising speed	VCC=3.3 V	20	∞	μs/V

	VCC lowering speed		100	∞	

4.3.3 Characteristics of Built-in Reset and Power Control Module

The parameters given in the following table are obtained by testing at the ambient temperature and VCC supply voltage listed in Table 4-4.

Table 4-6 Characteristics of Built-in Reset and Power Control Module(1)

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{BOR}	VCC threshold power-on voltage	T_A=25°C		1.65		V
	VCC threshold power-off voltage	T_A=25°C		1.60		
$V_{BORhyst}$	BOR delay	T_A=25°C		20		mV

(1) They are guaranteed by the design and are not tested in production.

4.3.4 Characteristics of DCDC

DCDC is an internal voltage generation module. The parameters given in the following table are obtained by testing at the ambient temperature and VCC supply voltage listed in Table 4-4.

Table 4-7 Built-in DCDC Power Management Module Characteristics (1)

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
VCC	Supply voltage			3.3		V
VDCDC	DCDC output voltage			1.15		V
I_{load}	DCDC current carrying capacity	Output current@ VDCDC=1.15 V			20	mA
η	DCDC conversion efficiency(2)			82.5		%
V_{RPL}	DCDC output voltage fluctuation			10		mV
L	DCDC load inductance		1	2.2	10	μH
C_{OUT}	DCDC load capacitance		0.5	2	10	μF
t_{STAR}	DCDC output voltage setup time			90		uS

(1) They are guaranteed by the design and are not tested in production.

(2) The FDK MIPSDZ1608G2R2PA inductor is used in test. Different inductor models may vary in DCDC efficiency.

4.3.5 Characteristics of Supply Current

Current consumption is a composite indicator evaluated based on multiple parameters and factors, including operating voltage, ambient temperature, I/O pin load, software configuration, operating frequency, I/O pin switching rate, position of a program in memory, and code executed.

For the detailed method to measure current consumption, see Figure 4-4.

4.3.5.1 Typical Current Consumption

Table 4-8 Typical Current Consumption in Sleep Mode(1)

Symbol	Parameter	Condition	Minimum	Typical Value(1)	Maximum(1)	Unit
I_{CC}	Current in Sleep mode	Low speed clock: ON; 48 KB SRAM retention; I/O state unchanged		1.6	3.8	uA
	Current in PD mode	VCC is maintained; WAKEUP IO and NRST can be woken up		0.13	1.0	uA

(1) The test condition is T_A=25°C, VCC=3.3 V.

4.3.5.2 Typical Current Consumption in Operating Mode

The chip is under the following conditions:

- All I/O pins are reset.
- All peripherals are turned off unless otherwise specified.
- Ambient temperature and VCC supply voltage conditions are listed in Table 4-4.

Table 4-9 Typical Current Consumption in Operating Mode

Symbol	Parameter	Condition	Typical Value(1)	Maximum	Unit
I_{CC}	Supply current in operating mode	High speed internal RC oscillator (HSI)(2)	2.0		mA

(1) The typical value is measured at T_A=25°C and VCC=3.3 V.

(2) High speed internal clock is 64 MHz.

Table 4-10 BLE Power Dissipation

Symbol	Parameter	Condition	Typical Value(1)	Maximum	Unit
I_{CC}	Supply current in operating mode	0 dbm transmitting power, VCC current	4.2		mA

		Minimum RX sensitivity, VCC current	3.8		mA
		1 s broadcast interval, VCC average current	13		uA
		100 ms broadcast interval, VCC average current	109		uA
		100 ms connection interval, VCC average current	70		uA

(1) The typical value is measured at T_A=25°C and VCC=3.3 V.

4.3.6 Characteristics of External Clock Source

4.3.6.1 High Speed External Clock Generated Using a Crystal/Ceramic Resonator

The high speed external clock (HSE) can be generated by an oscillator consisting of a 32 MHz crystal/ceramic resonator. The data presented in this section is obtained from the overall characteristic evaluation using the typical external components listed in the table below. In applications, the resonator and load capacitor must be as close to the pin of the oscillator as possible to reduce output distortion and stabilization time at startup. For more parameters (such as frequency, package, and precision) of a crystal resonator, please contact the manufacturer. (The crystal resonator mentioned here usually means the passive crystal oscillator.)

Table 4-11 Characteristics of HSE 32 MHz Oscillator(1)(2)

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{OSC_IN}	Oscillator frequency			32		MHz
C_{L1} C_{L2}(3)	Recommended load capacitance and corresponding crystal serial impedance (RS)(4)	RS = 100Ω(4)		12		pF
I_D	HSE drive current	VCC=3.3 V, 12 pF load		0.2		mA
$t_{SU(HSE)}$(5)	Startup time			0.2		ms

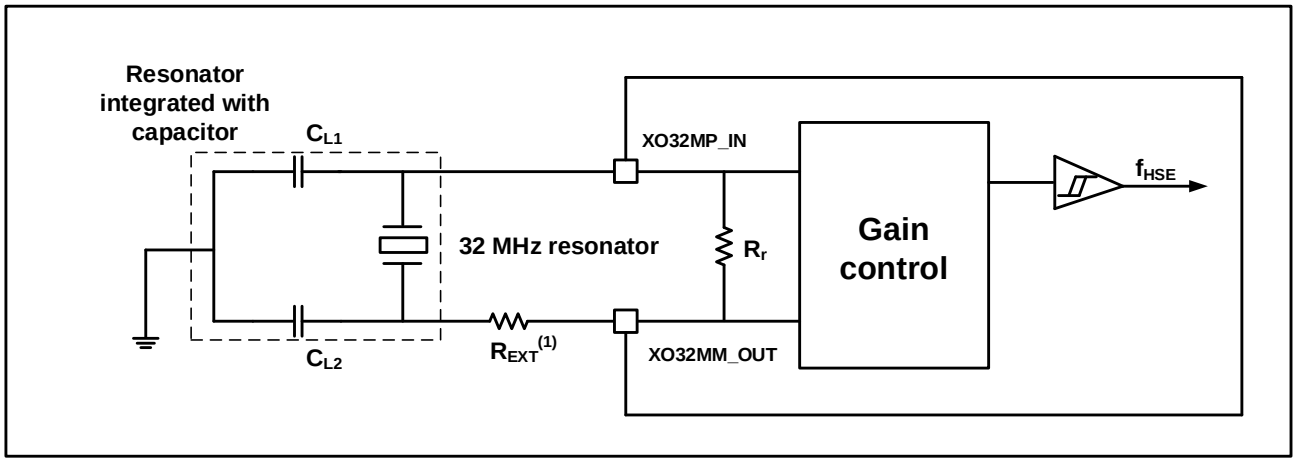
(1) Resonator's characteristic parameters are given by the manufacturers of crystal/ceramic resonators.

(2) They are obtained from laboratory tests and are not tested in production.

(3)(4) For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic dielectric capacitors designed for high frequency applications and select suitable crystals or resonators. C_{L1} and C_{L2} usually share same parameters. Crystal manufacturers usually give the parameter of load capacitance as a serial combination of CL1 and CL2. When selecting C_{L1} and C_{L2}, you should consider the capacitive reactance of PCB and chip pins.

(5) $t_{SU(HSE)}$ is the startup time, which is measured from the moment when the software enables HSE until a stable 32 MHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary greatly depending on the crystal manufacturer.

Figure 4-5 Typical Application with a 32 MHz Crystal



(1) The value of R_{EXT} depends on the characteristics of the crystal.

4.3.6.2 Low Speed External Clock Generated Using a Crystal/Ceramic Resonator

The low speed external clock (LSE) can be generated by an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. The data presented in this section is obtained from the overall characteristic evaluation using the typical external components listed in the table below. In applications, the resonator and load capacitor must be as close to the pin of the oscillator as possible to reduce output distortion and stabilization time at startup. For more parameters (such as frequency, package, and precision) of a crystal resonator, please contact the manufacturer. (The crystal resonator mentioned here usually means the passive crystal oscillator.)

Notes: For C_{L1} and C_{L2}, it is recommended to use ceramic dielectric capacitors between 8 pF and 20 pF and select suitable crystals or resonators. C_{L1} and C_{L2} usually share same parameters. Crystal manufacturers usually give the parameter of load capacitance as a serial combination of C_{L1} and C_{L2}. Different crystals or resonators usually require different load capacitance (CL). The selected C_{L1} and C_{L2} must match the crystal or resonator used.

The load capacitance CL is calculated by the formula: $CL = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where, C_{stray} is the capacitance of the pin and the capacitance associated with the PCB or PCB, typically between 2 pF and 7 pF.

Table 4-12 Characteristics of LSE Oscillator (f_{LSE}=32.768kHz)(1)

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
C_{L1} C_{L2}(2)	Recommended load capacitance and corresponding crystal serial impedance (RS)(3)	RS: 30KΩ~90KΩ		10		pF
I2	LSE drive current	VCC=3.3 V, C_{L1}=C_{L2}=10 Pf, RS=30 KΩ		0.2		μA

$t_{SU(LSE)}$(4)	Startup time			0.84		s

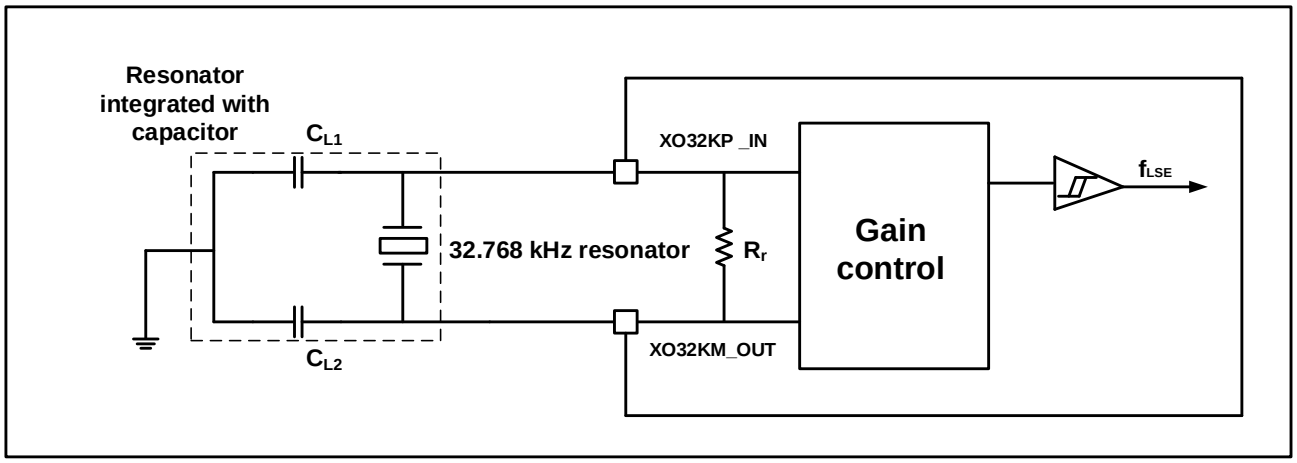
(1) They are obtained from laboratory tests and are not tested in production.

(2) See the "Notes" at the top of this table.

(3) Using a high quality oscillator with a small RS value can optimize the current consumption. For more details, please contact the crystal manufacturer.

(4) $t_{SU(LSE)}$ is the startup time, which is measured from the moment when the software enables LSE until a stable 32.768 KHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary greatly depending on the crystal manufacturer.

Figure 4-6 Typical Application with a 32.768 kH Crystal



4.3.7 Characteristics of Internal Clock Source

The characteristic parameters given in the following table are obtained by testing at the ambient temperature and supply voltage listed in Table 4-4.

High Speed Internal (HSI) RC Oscillator

Table 4-13 Characteristics of HSI Oscillator(1)(2)

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{HSI}	Frequency	T_A = 25°C	63.36	64	64.64	MHz
ACC_{HSI}	Temperature drift of HSI oscillator	T_A = -40~105°C, temperature drift	-3		3	%
		T_A = -10~85°C, temperature drift	-2		2	%
		T_A = 0~70°C, temperature drift	-1		1	%
$t_{SU(HSI)}$	Startup time of HSI oscillator				0.3	μs
$I_{CC(HSI)}$	Power dissipation of HSI			180	260	μA

	oscillator					

(1) VCC = 3.3 V, T_A = -40~105°C.

(2) They are guaranteed by the design and are not tested in production.

Low Speed Internal (LSI) RC Oscillator

Table 4-14 Characteristics of LSI Oscillator(1)

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{LSI}(2)	Output frequency	Calibrated at 25°C	31.9	32	32.2	KHz
		T_A = -40~85°C, temperature drift	-1		1	%
$t_{SU(LSI)}$ (3)	Startup time of LSI oscillator				200	μs
$I_{CC(LSI)}$ (3)	Power dissipation of LSI oscillator			0.23		μA

(1) VCC = 3.3 V, T_A = -40~85°C.

(2) They are obtained from laboratory tests and are not tested in production.

(3) They are guaranteed by the design and are not tested in production.

4.3.8 Time Required to Wake Up from Low Power Modes

The wakeup time listed in Table 4-15 is measured during the wakeup phase of a 64 MHz HSI RC oscillator. The clock source used in wakeup depends on the current operating mode:

Sleep or PD mode: The clock source is a RC oscillator

All the time is measured under the ambient temperature and supply voltage listed in Table 4-4.

Table 4-15 Time Required to Wake Up from Low Power Modes

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
$t_{WUSLEEP}$(1)	Wake up from Sleep mode		0.2		ms
t_{WUPD}(1)	Wake up from PD mode		42		

(1) The wakeup time is measured from the start of the wakeup event to the reading of the first command by the user program.

4.3.9 Characteristics of FLASH Memory

Unless otherwise specified, all characteristic parameters below are obtained at T_A = -40~85°C.

Table 4-16 Characteristics of Memory

Symbol	Parameter	Condition	Minimum	Typical Value(1)	Maximum(1)	Unit
t_{PP}	Page (256 bytes) programming time	T_A = -40~85°C		2	3	ms
t_{PE}	Page (256 bytes) erasing time	T_A = -40~85°C		16	30	ms
t_{SE}	Sector (4K byte) erase	T_A = -40~85°C		16	30	ms
t_{CE}	Chip erasing time	T_A = -40~85°C		16	30	ms

(1) They are guaranteed by the design and are not tested in production.

Table 4-17 Flash Memory Life and Data Retention Period

Symbol	Parameter	Condition	Minimum(1)	Unit
N_{END}	Life (note: erasure times)	T_A = -40~85°C	10	Ten thousand times
		T_A = -40~105°C	1	Ten thousand times
t_{RET}	Data retention period	T_A = 105°C	20	Year

(1) They are obtained from laboratory tests and are not tested in production.

4.3.10 Absolute Maximum (Electrical Sensitivity)

The electrical sensitivity is determined by testing the chip strength using specified measurement methods based on three different tests (ESD, LU).

Electrostatic Discharge (ESD)

Electrostatic discharge (one positive pulse followed by one negative pulse after one second) is applied to all pins of all samples, and the sample size depends on the number of power supply pins on the chip (3 × (n+1) power supply pins). This test complies with the MIL-STD-883K and ESDA/JEDEC JS -002-2018 standards.

Table 4-18 Absolute Maximum of ESD

Symbol	Parameter	Condition	Type	Minimum(1)	Unit
$V_{ESD(HBM)}$	ESD voltage (human body model)	T_A = +25°C, MIL-STD-883K compliant	II	2000	V
$V_{ESD(CDM)}$	ESD voltage (charging device model)	T_A = +25°C, ESDA/JEDEC JS -002-2018 compliant	II	1000	

(1) They are obtained from laboratory tests and are not tested in production.

Static Latch-Up

Provide a supply voltage exceeding the limit for each power supply pin.

Inject current into each input, output and configurable I/O pin.

This test complies with JEDEC78E integrated circuit latch-up standard.

Table 4-19 Electrical Sensitivity

Symbol	Parameter	Condition	Type
LU	Static latch-up	T_A = +25/+85°C, JEDEC78E compliant	Class II A

4.3.11 I/O port characteristics

Characteristics of General Purpose Input/Output

Unless otherwise specified, the parameters given in the following table are obtained by measuring under the conditions listed in Table 4-4. All I/O ports are compatible with CMOS and TTL.

Table 4-20 Static Characteristics of I/O(1)(2)

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{IL}	Input low level voltage	VCC=3.3 V	VSS	0.8	V
		VCC=2.5 V	VSS	0.7	
V_{IH}	Input high level voltage	VCC=3.3 V	2	VCC	
		VCC=2.5 V	1.7	VCC	
Vhys	Hysteresis voltage of Schmitt trigger(1)	VCC=3.3 V/2.5 V	200		mV
Ilkg	Input leakage current(3)	V_{PAD}=0	-1	1	µA
		V_{PAD}=VCC			
R_{PU}	Weak pull-up equivalent resistance(4)	VCC=3.3 V V_{IN}= V_{IL}	120	140	kΩ
R_{PD}	Weak pull-down equivalent resistance(4)	VCC=3.3 V V_{IN}= V_{IH}	120	140	kΩ
C_{IO}	Capacitance of I/O pin			0.1	pF

(1)(2) Hysteresis voltage of Schmitt trigger's switching level. They are obtained from laboratory tests and are not tested in production.

(3) The leakage current may exceed the maximum if there is reverse sink current on adjacent pins.

Output Drive Current

GPIO (general purpose input/output port) can absorb or output up to +/-12 mA current.

Output Voltage

Table 4-21 I/O Output Voltage

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{OL}	Output low level	VCC=3.3, I_{OH}=2 mA, 4 mA, 8 mA, 12 mA	VSS	0.4	V
		VCC=2.5, I_{OH}=2 mA, 4 mA, 8 mA, 12 mA	VSS	0.4	
V_{OH}	Output high level	VCC =3.3 V, I_{OH} = -2 mA, -4 mA, -8 mA, -12 mA	2.4	VCC	
		VCC =2.5 V, I_{OH} = -2 mA, -4 mA, -8 mA, -12 mA	2	VCC	

Input and Output AC Characteristics

The definitions and values of input and output AC characteristics are given in Table 4-22.

Unless otherwise specified, the parameters given in the following table are obtained by measuring at the ambient temperature and supply voltage listed in Table 4-4.

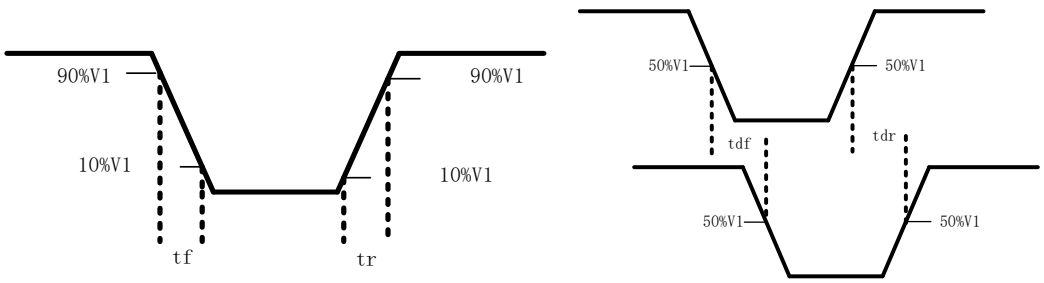
Table 4-22 Input and Output AC Characteristics(1)

Register Configuration	Symbol	Parameter	Condition	Minimum	Maximum	Unit
00 (2 mA)	$f_{max(IO)out}$	Maximum frequency	C_L=5 pF, VCC =3.3 V		64	MHz
			C_L=5 pF, VCC =2.5 V		50	
	$t_{(IO)out}$	Output delay	C_L=5 pF, VCC =3.3 V		3.66	ns
			C_L=5 pF, VCC =2.5 V		4.72	
	$t_{(IO)in}$	Input delay	C_L=50 fF, VCC =2.97 V		1.2	ns
			VCC=2.5 V			
01	$f_{max(IO)out}$	Maximum	C_L=10 pF, VCC =3.3 V		64	MHz

(4 mA)		frequency	C_L=10 pF, VCC =2.5 V		60	
	$t_{(IO)out}$	Output delay	C_L=10 pF, VCC =3.3 V		3.5	ns
			C_L=10 pF, VCC =2.5 V		4.5	
	$t_{(IO)in}$	Input delay	C_L=50 fF, VCC =2.97 V		1.2	ns
			C_L=50 fF, VCC=2.5 V			
10 (8 mA)	$f_{max(IO)out}$	Maximum frequency	C_L=20 pF, VCC =3.3 V		64	MHz
			C_L=20 pF, VCC =2.5 V		50	
	$t_{(IO)out}$	Output delay	C_L=20 pF, VCC =3.3 V		3.42	ns
			C_L=20 pF, VCC =2.5 V		4.73	
	$t_{(IO)in}$	Input delay	C_L=50 fF, VCC =2.97 V		1.2	ns
			C_L=50 fF, VCC = 2.5 V			
11 (12 mA)	$f_{max(IO)out}$	Maximum frequency	C_L=30 pF, VCC =3.3 V		64	MHz
			C_L=30 pF, VCC =2.5 V		50	
	$t_{(IO)out}$	Output delay	C_L=30 pF, VCC =3.3 V		3.34	ns
			C_L=30 pF, VCC =2.5 V		4.26	
	$t_{(IO)in}$	Input delay	C_L=50 fF, VCC =2.97 V		1.2	ns
			C_L=50 fF, VCC=2.5 V			

(1) They are guaranteed by the design and are not tested in production.

Figure 4-7 Definition of Input and Output AC Characteristics



4.3.12 Characteristics of NRST Pins

The NRST pin's input drive uses the CMOS process and is connected with a pull-up resistor R_{PU} that cannot be disconnected. Unless otherwise specified, the parameters given in Table 4-23 are obtained by measuring at the

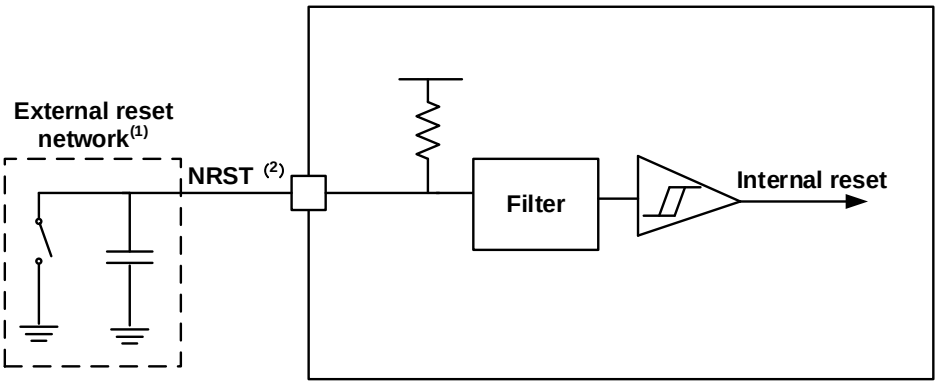
ambient temperature and supply voltage listed in Table 4-4.

Table 4-23 Characteristics of NRST Pins

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	VCC = 3.3 V	Vss	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	VCC = 3.3 V	2	-	VCC	
$V_{hys(NRST)}$(1)	Hysteresis voltage of NRST Schmitt trigger	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	VCC = 3.3 V	40	50	60	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	-	-	-	500	ns
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	-	5	-	-	us

(1) They are guaranteed by the design and are not tested in production.

Figure 4-8 Recommended NRST Pin Protection



(1) The external reset network is to avoid a parasitic reset.

(2) Users must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 4-23. Otherwise, the chip cannot be reset.

4.3.13 Characteristics of TIM Timer

The parameters given in Table 4-24 are obtained by measuring at the ambient temperature and supply voltage listed in Table 4-4.

Table 4-24 Characteristics of TIMx(1)(2)

Symbol	Parameter	Condition	Minimum	Maximum	Unit

$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$= 64 MHz	1		$t_{TIMxCLK}$
			15.625		ns
f_{EXT}	Timer's external clock frequency (CH1~CH4)		0	$f_{TIMxCLK}$/2	MHz
			0	32	MHz
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	Clock period of a 16-bit counter when an internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.015625	1024	μs
t_{MAX_COUNT}	Maximum possible count			65536x65536	$t_{TIMxCLK}$
				67.1	s

(1) TIMx is a generic name that represents TIM1/TIM3/TIM6.

(2) Parameters are guaranteed by the design.

4.3.14 Characteristics of I2C Interface

Unless otherwise specified, the parameters below are obtained by measuring at the ambient temperature, f_{PCLK1} frequency, and VCC supply voltage listed in Table 4-4.

The I2C interface conforms to the standard I2C communication protocol, but is subject to the following limitations: SDA and SCL are not "real" open-drain pins, and when they are configured as output open-drain, the PMOS transistor between the lead-out pin and VCC is turned off, but still exists.

The characteristics of I2C interface are shown in the table below. For more details on the characteristics of the input/output alternate function pins (SDA and SCL), see Section 4.3.11.

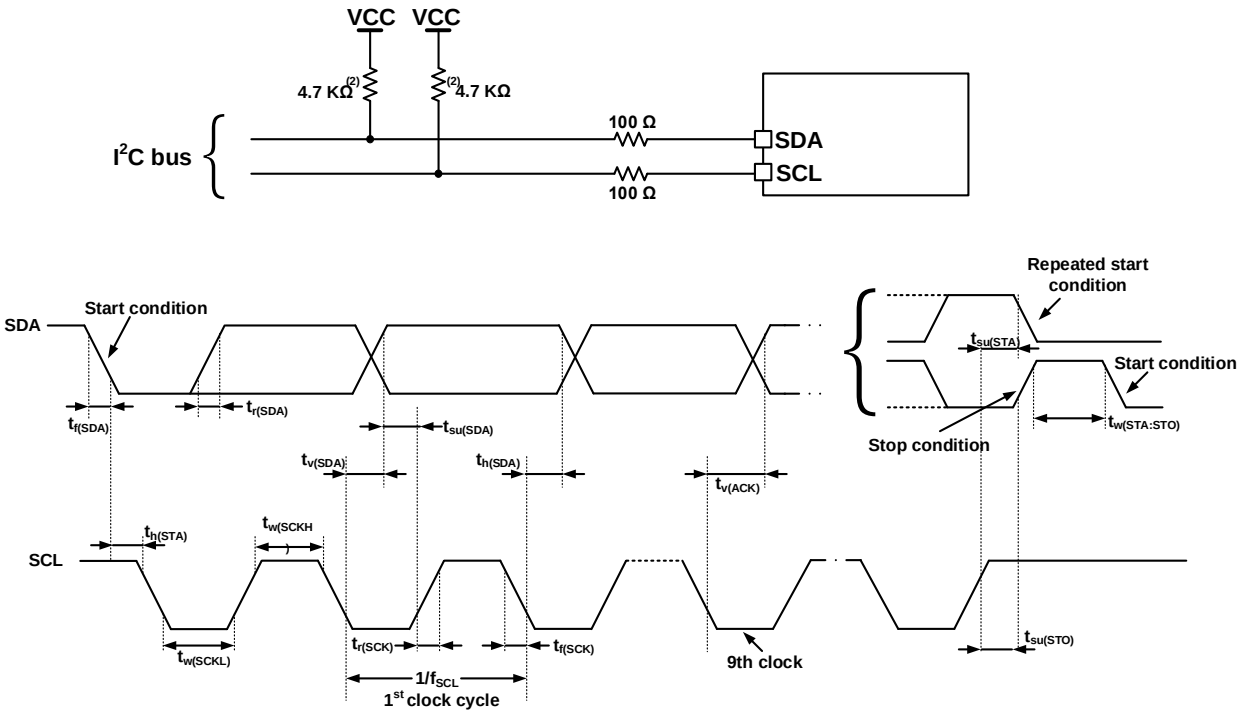
Table 4-25 Characteristics of I2C Interface(1)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
f_{SCL}	I2C Interface Frequency		100		1000	KHz
$t_{h(STA)}$	Start condition holding time	4.0		0.6		μs
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		μs
$t_{su(STA)}$	Setup time for a repeated start condition	4.7		0.6		μs
$t_{h(SDA)}$	SDA data hold time		3.4		0.9	μs
$t_{su(SDA)}$	SDA setup time	250.0		100		ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	ns
$t_{su(STO)}$	Setup time for a stop condition	4.0		0.6		μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7		1.3		μs
C_b	Capacitive load per bus		400		100	pf
$t_{v(SDA)}$	Data validity time	3.45		0.9		μs
$t_{v\ (ACK)}$	Valid time of acknowledgement	3.45		0.9		μs

(1) They are guaranteed by the design and are not tested in production.

(2) To reach the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2 MHz. To reach the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4 MHz.

Figure 4-9 AC Waveform and Measuring Circuit of I2C Bus(1)



(1) The measuring points are set at CMOS levels: 0.3 VCC and 0.7 VCC.

4.3.15 Characteristics of SPI

Unless otherwise specified, the SPI parameters are obtained by measuring at the ambient temperature, f_{PCLK2} frequency, and VCC supply voltage listed in Table 4-4.

For more details on the characteristics of the input/output alternate function pins (NSS, SCLK, MOSI, MISO), see Section 4.3.11.

Table 4-26 Characteristics of SPI(1)

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI's clock rise and fall time	Load capacitance: C = 30 pF	-	8	ns
$DuCy_{(SCK)}$	Duty cycle of SPI's slave input clock	SPI slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1)	SCLK high and low time	Master mode	t_{PCLK} - 2	t_{PCLK} + 2	ns

$t_{w(SCLKL)}$(1)						
$t_{su(MI)}$(1)	Data input setup time	Master mode	SPI1	5	-	ns
			SPI2	6		
$t_{su(SI)}$(1)		Slave mode	SPI1	5		
			SPI2	6		
$t_{h(MI)}$(1)	Data input hold time	Master mode		4		ns
$t_{h(SI)}$(1)		Slave mode		3		
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 32 MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Data output disabled time	Slave mode		2	10	ns
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enabled edge)	SPI1		16	ns
			SPI2		20	
$t_{v(MO)}$(1)		Master mode (after enabled edge)	SPI1		8	
			SPI2		10	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enabled edge)		2		ns
$t_{h(MO)}$(1)		Master mode (after enabled edge)		0		

(1) They are obtained from laboratory tests and are not tested in production.

(2) The minimum represents the minimum time to drive the output, and the maximum represents the maximum time to obtain the data correctly.

(3) The minimum represents the minimum time to turn off the output, and the maximum represents the maximum time to put the data line in a high impedance state.

Figure 4-10 SPI Sequence Diagram–Slave Mode and CPHA=0

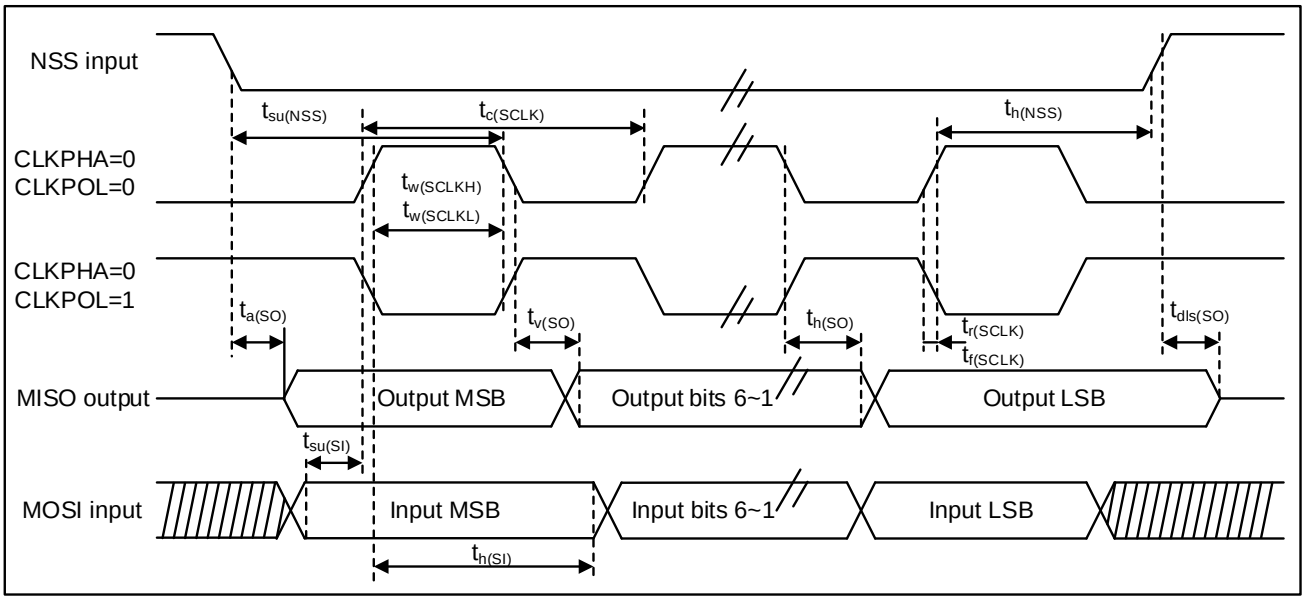
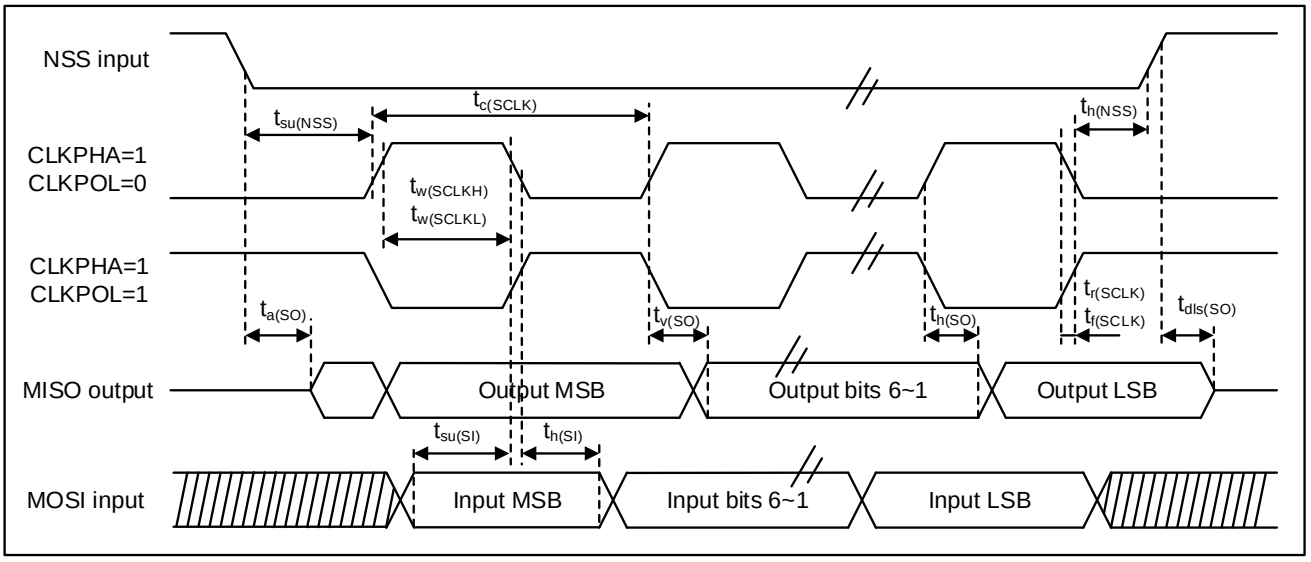
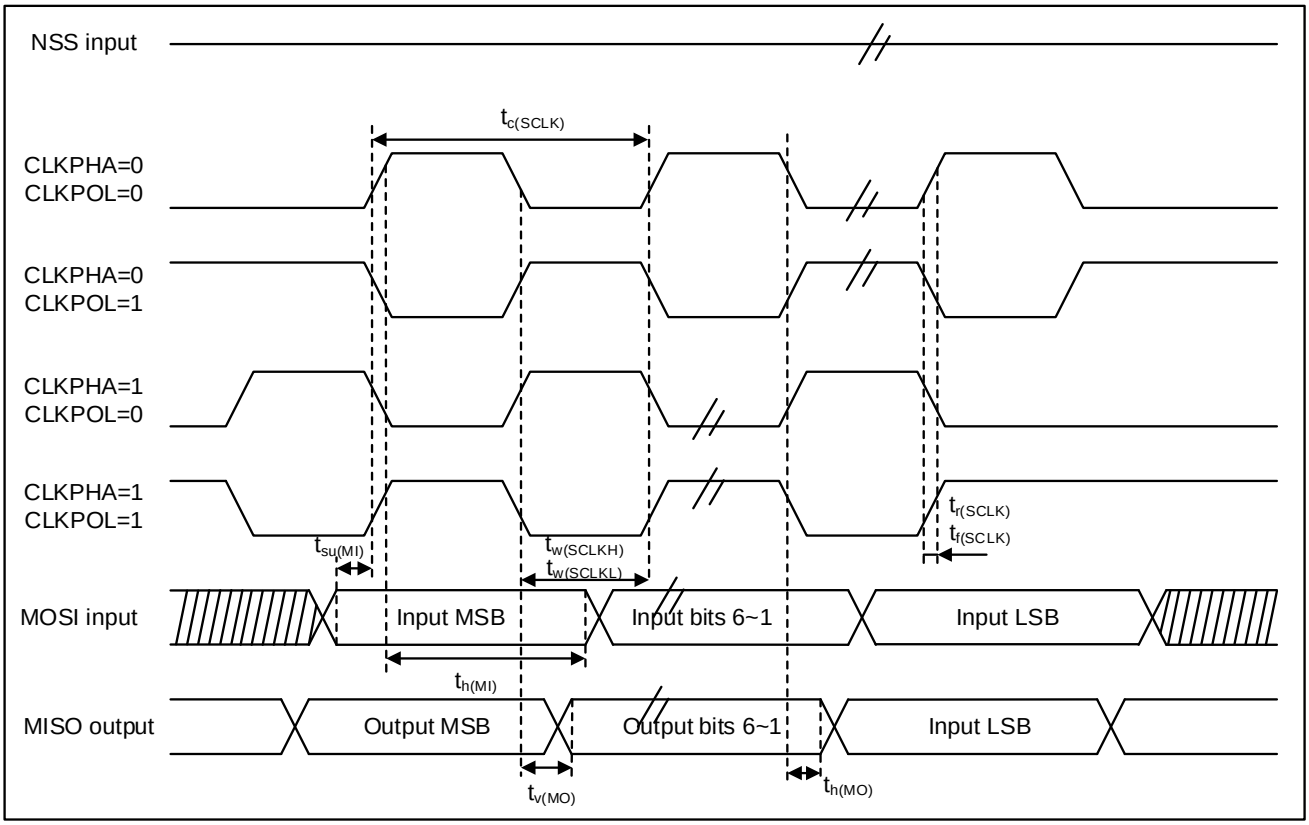


Figure 4-11 SPI Sequence Diagram–Slave Mode and CPHA=1(1)



(1) The measuring points are set at CMOS levels: 0.3 VCC and 0.7 VCC.

Figure 4-12 SPI Sequence Diagram–Master Mode(1)



(1) The measuring points are set at CMOS levels: 0.3 VCC and 0.7 VCC.

4.3.16 Characteristics of Temperature Sensor (TS)

Unless otherwise specified, the parameters below are obtained by measuring at the ambient temperature, f_{HCLK} frequency, and VCC supply voltage listed in Table 4-4.

Table 4-27 Characteristics of Temperature Sensor

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
T_L(1)	V_{SENSE} Linearity with respect to temperature		±4		°C
Avg_Slope(1)	Average slope		2.14(2)		mV/°C
t_{START}(1)	Setup time			10	μs

(1) They are guaranteed by the design and are not tested in production.

(2) They are obtained from laboratory tests and are not tested in production.

4.3.17 Characteristics of ADC

Unless otherwise specified, the parameters below are obtained by measuring at the ambient temperature, f_{HCLK} frequency, and VCC supply voltage listed in Table 4-4.

Table 4-28 Characteristics of ADC

Symbol	Parameter	Test Condition	Minimum	Typical Value	Maximum	Unit
V_{REF+}	Positive reference voltage			1.0		V
f_{ADC}	ADC sampling rate				1.33	MHz
V_{AIN}	Voltage conversion range, external low voltage path		0		1000	mV
	Voltage conversion range, external high voltage path		0	-	3600(2)	mV
R_{ADC}	Sampling switch resistance					kΩ
C_{ADC}	Internal sampling and holding capacitance					pF
SNDR	Ingal noise distortion ration	Input Frequency=1.03 KHz, VCC=3.3 V, T_A=25°C f_{ADC}=1Msps		46		dBFS
SNDR	Ingal noise distortion ration	Input Frequency=0.98 KHz, VCC=3.3 V, T_A=25°C f_{ADC}=16 Ksps		58		dBFS
t_{STAB}(1)	Power-on time			16		us
t_{CONV}(1)	Conversion time		752			ns
DNL	Differential linear error	VCC=3.3 V, T_A=25°C,	-1		6	LSB
INL	Integral linear error	VCC=3.3 V, T_A=25°C	-8		2	LSB

(1) They are obtained from laboratory tests and are not tested in production.

(2) The maximum value 3600 mV and <= VCC+ 300 mV.

4.3.18 Characteristics of PGA

Unless otherwise specified, the parameters below are obtained by measuring at the ambient temperature and VCC supply voltage listed in Table 4-4.

Table 4-29 Characteristics of PGA

Symbol	Parameter	Test Condition	Minimum	Typical Value	Maximum	Unit
GAIN	PGA gain		0		42	dB
GAIN STEP	PGA gain step			6		dB
THD+N(1)	Gain=0dB		73	82	85	dB
	Gain=42 dB		73	83	87	dB
In-band ripple(1)	Gain fluctuation in 300–3400 Hz band			0.78		dB
T_{PGA}(1)	PGA setup time			15		ms
MIC_BIAS voltage	MIC bias voltage, step=0.1 V		1.6		2.3	V
MIC_BIAS Noise(1)	20Hz to 8kHz A-weighted with 4.7uF			-92		dBV

(1) They are obtained from laboratory tests and are not tested in production.

4.3.19 Characteristics of KEYSCAN

Unless otherwise specified, the parameters below are obtained by measuring at the ambient temperature and VCC supply voltage listed in Table 4-4.

Table 4-30 Characteristics of KEYSCAN

Symbol	Parameter	Test Condition	Minimum	Typical Value	Maximum	Unit
T_{WTS}	Time interval for each round of keyboard scanning			32	224	ms
T_{DTS}	Key jitter elimination time		10		640	ms
Icc(1)	Power dissipation in automatic scanning mode (104 keys)	T_{DTS}=40 ms, T_{WTS}=32 ms VCC=3.3 V, T_A=25 °C		2.9		uA
	Power dissipation in low power mode (104 keys)	VCC=3.3 V, T_A=25 °C		2.3		uA

(1) They are obtained from laboratory tests and are not tested in production.

4.3.20 Characteristics of BLE

Unless otherwise specified, the parameters below are obtained by measuring at the ambient temperature and VCC

supply voltage listed in Table 4-4.

Table 4-31 BLE Receiving Characteristics(1)

No.	Parameter	Test Condition	Minimum	Typical Value	Maximum	Unit
1	Sensitivity, 1 Mbps	VCC=3.3 V, T_A=25 °C		-96		dBm
2	Sensitivity, 2 Mbps			-93		dBm
3	Co-channel interference			8		dB
4	Adjacent channel interference, +-1 MHz			1		dB
5	Adjacent channel interference, +-2 MHz			-31		dB
6	Adjacent channel interference, >=+-3 MHz			-40		dB
7	Mirror channel interference			-24		dB
8	Adjacent mirror channel interference, +-1 MHz			-28		dB
9	Maximum input power			6		dBm

(1) They are obtained from laboratory tests and are not tested in production.

Table 4-32 BLE Transmitting Characteristics(1)

No.	Parameter	Test Condition	Minimum	Typical Value	Maximum	Unit
1	Output power	VCC=3.3 V, T_A=25 °C		6		dBm
2	Frequency accuracy			7.5		kHz
3	Frequency drift rate			-9.4		kHz/50us
4	Frequency drift			-15.1		kHz
5	Initial frequency drift			-13.2		kHz
6	Δf1 average			258		kHz
7	Δf2 99.9%			218		kHz

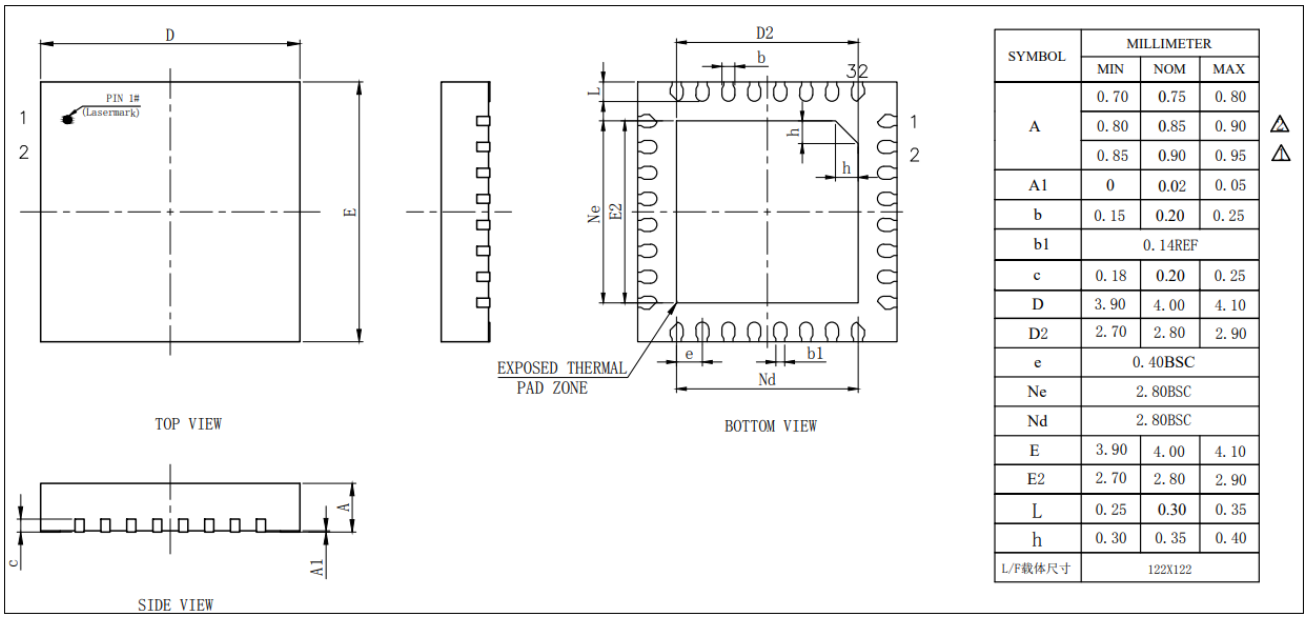
8	Δf2/Δf1			1.06		-
9	Harmonic power, second harmonic			-26		dBm
10	Harmonic power, third harmonic			-28		dBm
11	Harmonic power, fourth harmonic			-54		dBm
12	Harmonic power, quintuple harmonic			-55		dBm

(1) They are obtained from laboratory tests and are not tested in production.

5 Package Size

5.1 QFN32

Figure 5-1 QFN32 Package Size



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	⚠2
	0.85	0.90	0.95	⚠1
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.14REF			
c	0.18	0.20	0.25	
D	3.90	4.00	4.10	
D2	2.70	2.80	2.90	
e	0.40BSC			
Ne	2.80BSC			
Nd	2.80BSC			
E	3.90	4.00	4.10	
E2	2.70	2.80	2.90	
L	0.25	0.30	0.35	
h	0.30	0.35	0.40	
L/F载体尺寸	122X122			

6 Version History

Date	Version	Modification
2023/5/23	V1.3	Initial version
2023/7/28	V1.4	Added the MSL information in 4.2. Added note regarding the power supply in 4.1.6.