Application Note AN-62
LYTSwitch-2 Family

Design Guide and Considerations

Introduction

The LYTSwitch™-2 family comprises a group of highly integrated monolithic switching ICs designed for off-line power supplies with outputs up to 12 W. Ideally suited for LED drivers both ballast (external) and bulb (internal) applications, LYTSwitch-2 ICs provide constant voltage and constant current (CV/CC) output regulation without the need for an optocoupler or secondary feedback circuitry. ON/OFF control optimizes efficiency across load and line, enabling designs to easily meet low no-load and high efficiency requirements.

Each member of the LYTSwitch-2 family has a high-voltage power MOSFET and controller integrated onto the same die. The internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up components. The internal oscillator is frequency-modulated (jitter) to reduce EMI. In addition, the ICs have integrated system-level protection. The auto-restart function limits dissipation in the power MOSFET, the transformer, and the output diode during overload, output short-circuit, and open-loop conditions. The auto-recovering hysteretic thermal shutdown function disables MOSFET switching during a thermal fault.

Power Integrations' EcoSmart™ Technology enables power supplies designed around the LYTSwitch-2 family to consume less than 200 mW of no-load power at 230 VAC without an external bias circuit, and to consume below 30 mW with a low-cost external bias circuit.

Basic Circuit Configuration

The circuit in Figure 1 shows a flyback power supply using a LYTSwitch-2 IC. Because of the high-level integration of LYTSwitch-2 ICs, there are few design issues that need to be addressed externally, resulting in a common circuit configuration for all applications.

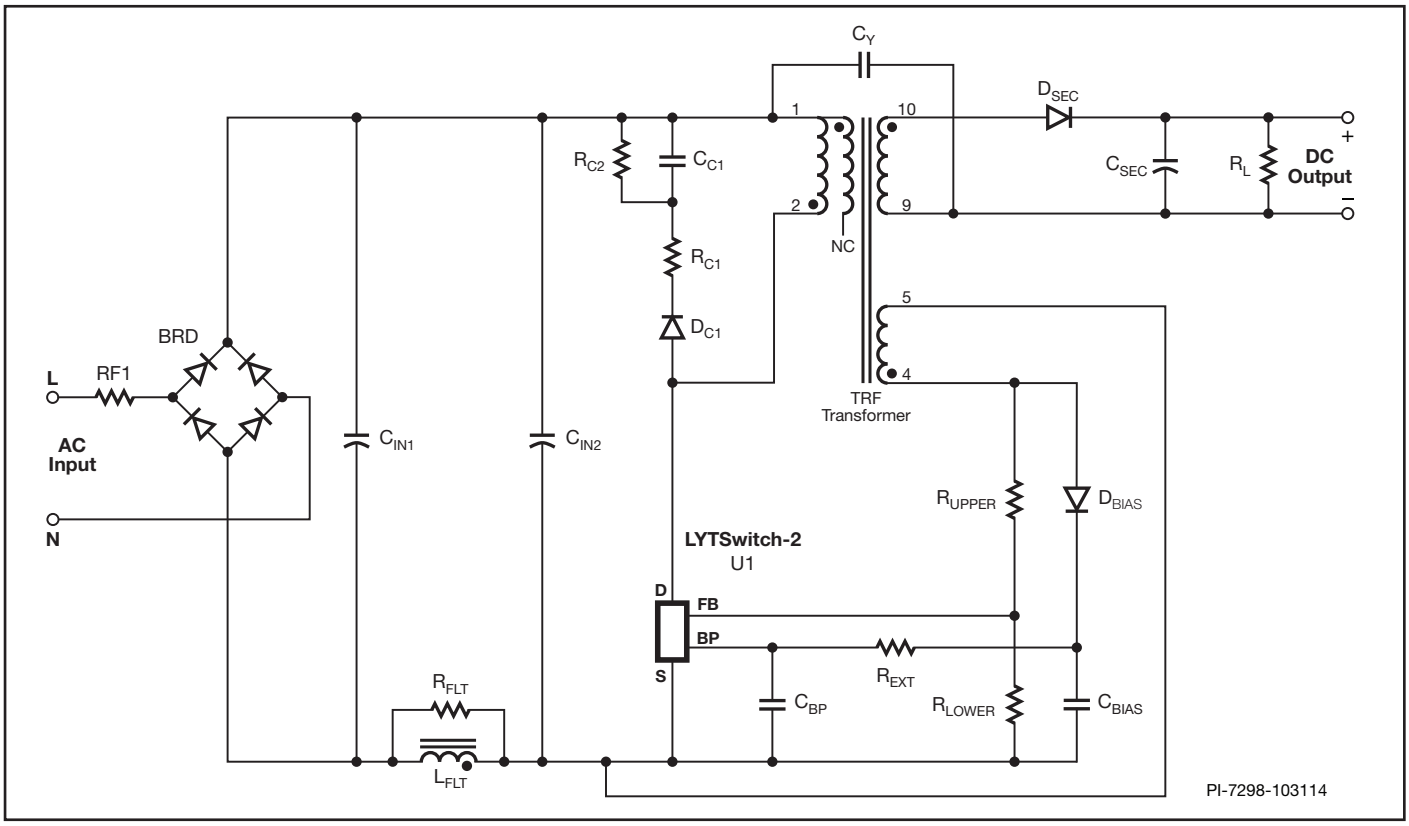


Figure 1. Typical LYTSwitch-2 Flyback Power Supply with Primary Sensed Feedback and Bias Supply.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the LYTSwitch-2 family of ICs. It provides guidelines to enable an engineer to quickly select key components and complete a suitable transformer design. The application note makes use of the PIXIs design spreadsheet, part of the PI Expert™ design software suite which can be downloaded from http://www.power.com/en/design-support/pi-expert-design-software.

In addition to this application note you may also find LYTSwitch-2 Reference Design Kits (RDK), containing engineering prototype boards, and device samples, useful as the starting point for a new design.

Further details on downloading PI Expert, obtaining an RDK, and updates to this document can be found at www.power.com.

Quick Start

To start immediately, use the following methodology to design the transformer and select the components for a first prototype. Only the information described below needs to be entered into the PIXIs spreadsheet; other parameters will be automatically selected. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX}, and minimum line frequency f_L [B3, B4, B5].
- Enter application type (Ballast CV or CC, or Bulb) [B6].
- Enter nominal output voltage V_O [B7].
- Enter the nominal output current [B8].
- Enter efficiency estimate [B10] – entered as a decimal.
  - 0.8 for universal input voltage (90-265 VAC) or single 100/115 VAC (90-132 VAC), 0.85 for a single 230 VAC (180-265 VAC) design. You will be able to adjust the number as needed after measuring the efficiency of the first prototype board at maximum load and VAC_{MIN}.
- Enter loss allocation factor Z [B11].
  - 0.5 for typical application (adjust the number accordingly after first prototype board evaluation)
- Enter C_{IN} input capacitance [B13].
  - ≥2 µF/W for universal (90-265 VAC) or single (100/115 VAC) line voltage.
  - ≥1 µF/W for single (230 VAC) or single (180-265 VAC) line voltage.
  - Note: After selecting the LYTSwitch-2 device, if the computed maximum duty cycle [D64] is greater than 55%, you will need to increase input capacitance.
- Select the LYTSwitch-2 device from the drop-down list or Auto [B18].
  - Select the device using the information in Table 1.
- Enter the maximum operating frequency FS [B22]. (FS is the maximum operating frequency with nominal component values.)
  - Note: Recommended frequency is between 60 kHz and 90 kHz.
- Enter V_{DS} [B24], the on-state drain source voltage drop. Use 10 V if no better data is available.

Output Power Table[2]

Product[5]	90-308 VAC	
	Enclosed Bulb[3]	Ballast Driver[4]
LYT2001D	4 W	5 W
LYT2002D	5 W	6 W
LYT2003D	6 W	7 W
LYT2004D	7 W	8 W
LYT2004E/K	9 W	10 W
LYT2005E/K	10 W	12 W

Table 1. Output Power Table.

Notes:
1. Nominal input and bias supply applied to BYPASS pin.
2. Performance for typical design.
3. Maximum continuous power in a typical non-ventilated bulb measured at +50 °C ambient, device T_J ≤ 100 °C.
4. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at +50 °C.
5. Packages: D: SO-8C, E: eSIP-7C, K: eSOP-12B.

- Enter the output rectifier's forward voltage drop V_D [B25]. Use 0.5 for Schottky and 0.7 for ultrafast or standard PN-junction diodes.
- Verify that K_P [D26] is greater than 1.3 to ensure discontinuous operation. For best regulation performance, select value for K_P greater than 1.5.
- Select if External bias or Self bias [B35].
  - Select External bias for improved efficiency and minimized no-load input power.
  - If an external bias is selected in [B35], enter the desired bias voltage [B36]. 10 V is recommended to minimize no-load input power when V_O is less than 10 V.
- Enter > 4.6 µs for D_{CON} [B40], the output rectifier conduction time.
- Enter the core type from the drop down menu [B48]. If the desired core is not listed, then enter the core characteristics A_E, L_E, A_L and B_W ([B51] [B52] [B53] [B54]).
- Enter the margin width in [B55], if margin is needed.
  - Note: This reduces the winding width by twice the entered value.
- Enter the number of primary layers L [B56]. Use a maximum of 4 layers to limit the primary leakage inductance value.
- Enter the primary inductance tolerance $L_{P(TOLERANCE)}$ [B73].
- Enter in the transformers core maximum flux density BM_TARGET [B76].
  - Note: Limit flux density to 2500 Gauss, to keep the transformers audible noise to acceptable levels. Follow the guidance in column F.
- Verify that the core gap L_G [D81], the wire gauge AWG [D85], and the primary's winding current density CMA [D88] are acceptable.
- Verify that the LYTSwitch-2 drain voltage [D99] is less than 680 V.
- R_{UPPER} [D43] and R_{LOWER} [D44] feedback resistor values are provided automatically (Figure 1).
- Using PIVS [D100] and I_{SRMS} [D93] determine the proper output rectifier.

- Select an input capacitor voltage rating (above V_{MAX} [D61]), and select the ripple current rating (above I_{RIPPLE} [D67]).
- Use V_O [B7], I_{SP} [D92], and I_{RIPPLE} [D94], to select appropriate output filter capacitor.
- Using I_{AVG} [D65] and an estimated peak reverse voltage of 600 V to 1000 V, select the input rectifier diodes (typically 1N4006 or 1N4007 types).
- Using I_{AVG} [D65] determine the appropriate input filter inductor current rating. Usually an inductor value of 1 mH to 3 mH is sufficient to meet conducted EMI limit.
- After building the prototype power supply, measure the output voltage and current at peak power. Enter the values used for R_{UPPER_ACTUAL} and R_{LOWER_ACTUAL} in cells [B103] and [B104], respectively.
- Enter the measured voltage in cell [B105]. Enter the measured current at the transition from CV to CC operation in cell [B106]. PIXIs fine-tunes the feedback resistor values for the power supply. Install the closest 1% value resistors for R_{UPPER_FINE} [D107] and R_{LOWER_FINE} [D108].

Step-by-Step Design Procedure

Step 1. Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, Application Type, V_O, I_O, η, Z, t_C, C_{IN}

ENTER APPLICATION VARIABLES				
VACMIN		90	V	Minimum AC Input Voltage
VACMAX		265	V	Maximum AC Input Voltage
fL		50	Hz	AC Mains Frequency
Application Type	Ballast-CC	Ballast-CC		Choose application type
VO		30.00	V	Output Voltage. This value is recommended to be 10% higher than the maximum LED Voltage
IO		0.30	A	Power Supply Output Current (corresponding to peak power)
Power		9.00	W	Continuous Output Power
n		0.85		Efficiency Estimate at output terminals
Z		0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC		3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN		24.00	uF	Input Capacitance

Figure 2. Application Variables Section of the Design Spreadsheet.

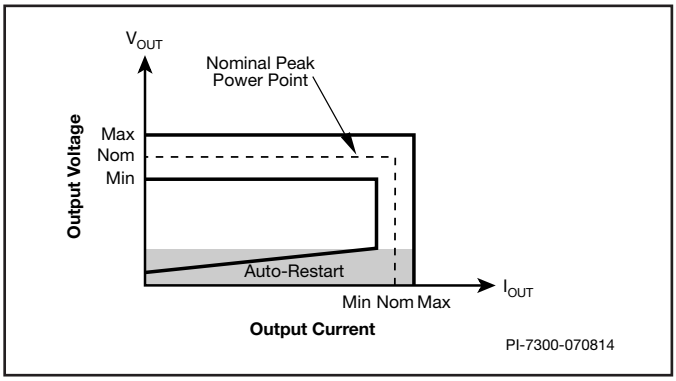


Figure 3. Output Characteristic Envelope Definitions.

Determine the input voltage range from Table 2.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	90	132
230	180	265
Universal	90	265

Table 2. Standard Worldwide Input Line Voltage Ranges.

Note: For designs that have a DC rather than an AC input, enter the values for minimum and maximum DC input voltages, V_{MIN} and V_{MAX}, directly into the grey override cell on the design spreadsheet (see Figure 4).

Line Frequency, F_L

Typical line frequencies are 50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC, and 50 Hz for single 230 VAC inputs. These values represent typical, rather than minimum, frequencies, but for most applications this gives adequate overall design margin. To design for the absolute worst case, reduce frequency by 6% (to 47 Hz or 56 Hz). For half-wave rectification use F_L/2. For DC input enter the voltage directly into Cells [B60] and [B61].

Nominal Output Voltage, V_O (V)

For either CC ballast or bulb designs, set V_O value to be 10% higher than the maximum LED load voltage. For CV ballast designs V_O is set to the nominal output voltage. Output voltage is measured at the end of an attached cable passing nominal output current.

Nominal Output Current, I_O (A)

For either CC ballast or bulb designs, I_O is the nominal output current at nominal output voltage. For CV ballast designs enter the specified output current plus 10%. The 10% factor ensures the supply remains in CV mode, while delivering the required output current across all conditions. The nominal output voltage and current may not be the same as the name-plate specification in the case of an external adapter. The nameplate specification typically describes minimum output voltage and current. Refer to Figure 3 for a representation of output voltage and current. The tolerance for the output current is ±5% (including initial tolerance and across temperature range).

Power Supply Efficiency, η

Enter the estimated efficiency of the power supply. Measure voltage and current at the end of the output cable (if applicable) under full load conditions and worst-case line (typically lowest input voltage). Start with 0.8 for universal input (90-265 VAC) or single 100/115 VAC (90-132 VAC) input voltage and 0.85 for a single 230 VAC (180-265 VAC) input voltage design. Adjust the number after measuring the efficiency of the first prototype board at peak output power, and at both VAC_{MIN} and VAC_{MAX}.

Power Supply Loss Allocation Factor, Z

This represents the ratio of power loss from the secondary relative to the total power loss from both the primary and secondary of the power supply. Z is used with the calculated efficiency to

DC INPUT VOLTAGE PARAMETERS				
VMIN		100.12	V	Minimum DC bus voltage
VMAX		374.77	V	Maximum DC bus voltage

Figure 4. DC Input Voltage Parameters Section of the Design Spreadsheet.

determine the power the input power stage must deliver. For example, losses in the input stage (EMI filter, rectification, etc.) are not processed by the power stage (transferred through the transformer), although they reduce efficiency, the transformer design is not impacted.

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

Use a value of 0.5 if no other data is available.

Bridge Diode Conduction Time, t_C (ms)
This is the duration of the incoming AC sine wave during which the input diodes conduct charging the input capacitance. This value is used to calculate the minimum voltage across the input capacitance at $VAC_{(MIN)}$. The actual value for t_C can be found by measuring the input current waveform. Use a value of 3 ms if no other data is available.

Total Input Capacitance, C_{IN} (µF)
Enter total input capacitance (use Table 3 for guidance). The capacitance is used to calculate the minimum voltage, V_{MIN}, across the bulk capacitor. Select a value for C_{IN} that keeps V_{MIN} >70 V.

Total Input Capacitance per Watt Output Power (µF/W)	
AC Input Voltage (VAC)	**Full Wave Rectification**
100/115	2
230	1
90-265	3

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

Step 2 – Enter LYTSwitch-2 Variables: LYTSwitch-2 Device and Package, F_S, V_{DS} and V_D

Select the correct LYTSwitch-2 device from Table 4. If "Auto" is chosen, PIXI's will choose the appropriate device size accordingly.

Output Power Table

Product	90-308 VAC	
	Enclosed Bulb	Ballast Driver
LYT2001D	4 W	5 W
LYT2002D	5 W	6 W
LYT2003D	6 W	7 W
LYT2004D	7 W	8 W
LYT2004E/K	9 W	10 W
LYT2005E/K	10 W	12 W

Table 4. Output Power Table.

Select the Operating Frequency, F_S
Enter the nominal operating switching frequency F_S. F_S is the switching frequency when the power supply is operating at nominal peak output power point. Changing the value for F_S can be used to adjust K_P, L_P and N_P. Select a frequency range between 60 kHz and 90 kHz. The minimum and maximum operating frequency varies depending on the tolerance of L_P and the internal current limit. A warning will be displayed if the calculated minimum or maximum frequency is outside the range of 60 kHz to 90 kHz.

LYTSwitch-2 On-State Drain-to-Source Voltage, V_{DS} (V)
This parameter is the average on-state voltage developed across the LYTSwitch-2 DRAIN and SOURCE pins. If no value is entered, PIXIs uses a default value of 10 V.

Output Diode Forward-Voltage Drop, V_D (V)
Enter the average forward-voltage drop of the output diode. If specific diode data is not available use 0.5 V for a Schottky diode or 0.7 V for a PN-junction diode. V_D has a default value of 0.5 V.

Ratio of MOSFET Off-Time to Secondary Diode Conduction Time, K_P
For proper regulation, LYTSwitch-2 requires the power supply to operate in discontinuous conduction mode (DCM). Verify that K_P is greater than 1.3 to ensure discontinuous operation. A value of greater than 1.5 is recommended. K_P should always be greater than 1, indicating discontinuous conduction mode, and is the ratio of primary MOSFET off-time to the secondary diode conduction time.

$$K_P \equiv K_{DP} = \frac{(1-D)\times T}{t} = \frac{V_{OR}\times(1-D_{MAX})}{(V_{MIN}-V_{DS})\times D_{MAX}}$$

Feedback Winding Parameter
The feedback winding parameters are calculated by PIXIs. N_{FB} is the number of feedback winding turns in the transformer. V_{FLY} and V_{FOR} represent the voltage across the feedback winding while the MOSFET is on (V_{FOR}) or off (V_{FLY}).

Bias Winding Parameters
If an external bias has been chosen in cell [B35], enter the bias voltage for V_B (Figure 7). N_B is the number of additional turns stacked on top of the feedback turns (AC stacked).

Step 3 – Select Output Diode Conduction Time, D_{CON} (µs)

D_{CON} is the output diode conduction time at peak output power. Changing the value for D_{CON} adjusts the number of secondary and feedback winding turns for better bobbin winding window utilization. Increasing D_{CON} increases the number of turns.

ENTER LYTSwitch-2 VARIABLES				
Chosen Device	**Auto**	LYT2004K/E		Chosen LYTSwitch-2 device
ILIMITMIN		0.46	A	Minimum Current Limit
ILIMITTYP		0.50	A	Typical Current Limit
ILIMITMAX		0.53	A	Maximum Current Limit
FS		80.00	kHz	Typical Device Switching Frequency at maximum power
VOR		94.71	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS		10.00	V	LYTSwitch-2 on-state Drain to Source Voltage
VD		0.50	V	Output Winding Diode Forward Voltage Drop
KP		1.28		Design will work, but for optimum CC regulation and audible noise, please use a KP larger than 1.30. You can either increase VMIN, or decrease FS, or increase part size to achieve this

Figure 5. Enter LYTSwitch-2 Variables Section of the Design Spreadsheet.

FEEDBACK WINDING PARAMETERS				
NFB		13.00		Feedback winding turns
VFLY		20.87	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR		22.06	V	Forward voltage - Voltage on Feedback Winding during switch on time

Figure 6. Feedback Winding Parameters Section of the Design Spreadsheet.

BIAS WINDING PARAMETERS				
BIAS	**Self bias**	Self bias		Select between self bias or external bias to supply the IC.
VB		N/A	V	Feedback Winding Voltage (VFLY) is greater than 20 V. The feedback winding itself can be used to provide external bias to the LYTSwitch. Additional Bias winding is not required.
NB		N/A		Bias Winding number of turns
REXT		N/A	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)

Figure 7. Bias Winding Parameters Section of the Design Spreadsheet.

DESIGN PARAMETERS				
DCON		4.60	us	Desired output diode conduction time
DCON_FINAL		4.65	us	Final output conduction diode, assuming integer values for NP and NS
TON		4.40	us	LYTSwitch-2 On-time (calculated at minimum inductance)
RUPPER		83.54	k-ohm	Upper resistor in Feedback resistor divider. Once the initial prototype is running, it may be necessary to use the fine tuning section of this spreadsheet to adjust to the correct output current
RLOWER		8.56	k-ohm	Lower resistor in resistor divider

Figure 8. Design Parameters Section of the Design Spreadsheet.

The minimum value for D_{CON} is limited to 4.6 µs to ensure that the output diode is still controlled under light loads when the feedback winding is sampled, (2.5 µs after the internal MOSFET is turned off). The maximum value of D_{CON} is normally limited by the value of K_P. As D_{CON} increases, K_P decreases until it reaches its minimum value of 1.3.

Resistors R_{UPPER} and R_{LOWER} (Figure 1) are the initial calculated values for the feedback winding resistors (Figure 1).

Step 4 – Choose Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, B_W, L

These symbols represent core effective cross-sectional area A_E (mm^2), core effective path length L_E (mm), core ungapped effective inductance A_L ($nH/Turn^2$), bobbin width B_W (mm) and number of primary layers L.

By default, if the core selection cell is left empty, the spreadsheet selects the smallest core size that meets the peak flux density limit. The user can change this selection and choose an alternate core from a list of commonly available cores (shown in Table 6).

Table 5 provides guidance on the power capability of specific core sizes.

The gray override cells [B48 through B55] can be used to enter the core and bobbin parameters directly.

Core Size	Output Power Capability
EF12.6	3.3 W
EE13	3.3 W
EE16	6.1 W
EF20	11 W

Table 5. Output Power Capability of Commonly Used Sizes in LYTSwitch-2 Designs.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type				
Core	**Auto**	EF20		Enter Transformer Core.
Custom_Core				Enter Core name if selection on drop down menu is "Custom"
Bobbin		EF20_BOBBIN		Generic EF20_BOBBIN
AE		33.50	mm^2	Core Effective Cross Sectional Area
LE		44.90	mm	Core Effective Path Length
AL		1570.00	nH/turn^2	Ungapped Core Effective Inductance
BW		12.20	mm	Bobbin Physical Winding Width
M		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L		3.00		Number of Primary Layers
NS		19.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON

Figure 9. Enter Transformer Core/Construction Variables Section of the Design Spreadsheet.

For designs that require safety isolation between primary and secondary (but are not using triple insulated wire), enter the width of the safety margin to be used on each side of the bobbin (parameter M) in box [B55]. Universal input designs typically require a total margin of 6.2 mm (3.1 mm entered into the spreadsheet). For vertical bobbins the margin may not be symmetrical. For a total required margin of 6.2 mm, enter 3.1 mm even if the physical margin is only on one side of the bobbin.

Enter the number of primary layers (L) [B56]. The maximum number of recommended primary layers is three. More layers increases leakage inductance, which increases losses.

Transformer Core Size		
EE8	EF12.6	EI16
EE10	EF16	EI19
EE12.9	EF20	EI22
EE13	EFD10	EI25
EE26	EFD12	EEL16
EE16W	EFD15	EEL19
EE1616	EFD20	EEL22
EE19	EFD25	RM5
EE22	EPC13	RM6
EE25	EPC17	RM7
EEM12.4	EPC19	EE10/10

Table 6. List of Cores Provided in LYTSwitch-2 PIXIs Spreadsheet.

NS is the number of secondary turns. To increase the number of turns, increase the value of D_{CON} [B40].

Step 5 – Iterate Transformer Design and Generate Key Transformer Design Parameters

Iterate the design, making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column. Messages marked “Info” provides information on parameters that can be further optimized. Once all warnings have been addressed, use the information to build the transformer.

Primary Inductance, $L_{P(TYP)}$, $L_{P(MIN)}$ (µH), $L_{P(TOLERANCE)}$, (%)
The key transformer electrical parameters are $L_{P(TYP)}$, $L_{P(MIN)}$ (µH), $L_{P(TOLERANCE)}$ and represent the minimum primary inductance needed to deliver the nominal peak output power ($V_O \times I_O$).

As it is more common to specify the primary inductance to a vendor as a nominal value with tolerance, the value for $L_{P(TYP)}$ can be calculated

$$L_{P(TYP)} = L_{P(MIN)} \times \left(1 + \frac{L_{P(TOLERANCE)}}{100}\right)$$

where $L_{P(TOLERANCE)}$ is the percentage tolerance. If no value is entered, PIXIs uses 7 by default, signifying $L_{P(TOLERANCE)}$ of ±7%.

Primary Winding Number of Turns, N_P
This is the total number of primary turns.

Gapped Core Effective Inductance, A_{LG} (nH/T²)
This is the target core effective inductance at $L_{P(MIN)}$ for the typical A_{LG} value multiplied by 1 + ($L_{P(TOLERANCE)}$/100).

Target Flux Density, B_{M_TARGET} (Gauss)
B_{M_TARGET} is the operating core flux density and the AC flux swing. Use a maximum value of 2600 (0.26 T) to minimize audible noise.

DC INPUT VOLTAGE PARAMETERS				
VMIN		100.12	V	Minimum DC bus voltage
VMAX		374.77	V	Maximum DC bus voltage

Figure 10. DC Input Voltage Parameters Section of the Design Spreadsheet.

CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.43		Maximum duty cycle measured at VMIN
IAVG		0.12	A	Input Average current
IP		0.46	A	Peak primary current
IR		0.46	A	Primary ripple current
IRMS		0.20	A	Primary RMS current

Figure 11. Current Waveform Shape Parameters Section of the Design Spreadsheet.

TRANSFORMER PRIMARY DESIGN PARAMETERS				
LPMIN		958.16	uH	Minimum Primary Inductance
LPTYP		1030.28	uH	Typical Primary inductance
LP_TOLERANCE		7.00	%	Tolerance in primary inductance
NP		59.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG		295.97	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET		2600.00	Gauss	Target Flux Density
BM		2580.25	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2600 is recommended
BP		2956.08	Gauss	Peak Operating Flux Density (calculated at maximum inducatnce and max current limit), BP < 3100 is recommended
BAC		1290.13	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		167.45		Relative Permeability of Ungapped Core
LG		0.13	mm	Gap Length (LG > 0.1 mm)
BWE		36.60	mm	Effective Bobbin Width
OD		0.62	mm	Maximum Primary Wire Diameter including insulation
INS		0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.55	mm	Bare conductor diameter
AWG		24	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		406.37	Cmils	Bare conductor effective area in circular mils
CMA		2036.33	Cmils/A	!!! Info. CMA is on the higher side of recommenation but design will work. Consider reducing number of primary layers

Figure 12. Transformer Primary Design Parameters Section of the Design Spreadsheet

TRANSFORMER SECONDARY DESIGN PARAMETERS				
ISP		1.43	A	Peak Secondary Current
ISRMS		0.64	A	Secondary RMS Current
IRIPPLE		0.56	A	Output Capacitor RMS Ripple Current
CMS		127.43	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		29.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)

Figure 13. Transformer Secondary Design Parameters Section of the Design Spreadsheet.

Core Gap Length, L_G (mm)

L_G is the estimated core gap length. Values below 0.1 mm are generally not recommended for center-leg gapped cores due to the resultant increase in tolerance of the primary inductance.

Maximum Primary Winding Wire Outside Diameter, OD (mm)

This is the maximum wire diameter that will allow the primary winding to fit into the number of specified layers. When selecting the wire type we recommend the use of double-coated magnetic wire (rather than single-coated types) to improve reliability and reduced primary capacitance (lowering no-load input power).

Primary Winding Wire Bare Conductor Diameter, DIA (mm)

This is the diameter of the wire without insulation.

Primary Winding Wire Gauge, AWG

This is the wire diameter rounded down to the next standard American Wire Gauge size.

Primary Winding Bare Conductor Effective Area, CM (C_{MILS})

CM is the effective conductor area in circular mils.

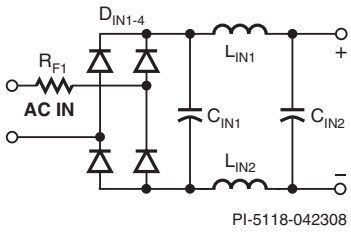
Primary Winding Wire Current Capacity, CMA (C_{MILS}/A)

CMA is the primary conductor area in circular mils (where 1 mil = 1/1000th of inch) per Amp. Values below the recommended minimum of 200 may be acceptable if worst-case winding temperature is measured (maximum ambient, lowest AC input voltage, maximum output power) and is <100 ºC, meeting Class A Safety limits

Step 6 – Selection of Input Stage

The recommended input stage is shown in Table 7. It consists of a fusible element, input rectification, and a line filter network.

The fusible element can be either a fusible resistor or a fuse. If a fusible resistor is selected, the use of a flameproof type is recommended. Depending on the differential line input surge requirements, a wire-wound type may be required. Avoid using metal or carbon film types as these can fail due to the inrush current when VAC_{MAX} is applied repeatedly to the power supply.



R_{F1}: 8.2 Ω, 2 W, Flameproof fusible resistor
L_{IN1}: 470 µH – 4.7 mH, 0.05 A – 0.3 A
L_{IN2}: Ferrite bead or 470 µH – 4.7 mH, 0.05 A – 0.3 A
C_{IN1} + C_{IN2}: ≥ 2 µF/W_{OUT}, 400 V, 90 VAC - 265 VAC
: ≥ 2 µF/W_{OUT}, 200 V, 100 VAC - 115 VAC
: ≥ 1 µF/W_{OUT}, 400 V, 180 VAC - 265 VAC
D_{IN1-4}: 1N4007, 1 A, 1000 V

Table 7. Input Stage Recommendation.

Step 7 – Selection of BYPASS Pin Capacitor, Bias Winding and Feedback Components

BYPASS Pin Capacitor

Use a 1 µF BYPASS pin capacitor (C5 in Figure 16) with a voltage rating greater than 7 V. The capacitor type is not critical. However, the absolute minimum value (including tolerance and temperature) must be ≥0.5 µF. The capacitor must be physically located close to the LYTSwitch-2 BYPASS and SOURCE pins.

External Bias Circuit

The addition of a bias circuit decreases the no-load input power from ~200 mW down to less than 30 mW.

The power supply schematic shown in Figure 16 uses the bias circuit formed by diode D2, capacitor C6, and resistor R6. If the output voltage is less than 8 V, an additional transformer winding is needed as shown in Figure 19. This provides sufficient voltage to supply the BYPASS pin under all conditions.

The additional bias winding (from pin 2 to pin 1) is stacked on top of the feedback winding (pin 4 to pin 2). Diode D6 rectifies the output and C5 is the filter capacitor. A capacitor of at least 1 µF is recommended to hold up the bias voltage during low frequency operation at no-load. The voltage rating should be above the maximum value of V_{BIAS}. The recommended current into the BYPASS pin is equal to the IC supply current (~0.5 mA). The value of R4 is calculated according to

$$R_4 = (V_{BIAS} - V_{BP})/I_{S2}$$

VOLTAGE STRESS PARAMETERS				
VDRAIN		593.66	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
PIVS		150.69	V	Output Rectifier Maximum Peak Inverse Voltage

Figure 14. Voltage Stress Section of the Design Spreadsheet.

FINE TUNING				
RUPPER_ACTUAL		83.54	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL		8.56	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)		30.00	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)		0.30	Amps	Measured Output current from first prototype
RUPPER_FINE		83.54	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 84.5 k-ohms
RLOWER_FINE		8.56	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 8.66 k-ohms

Figure 15. Fine Tuning Section of the Design Spreadsheet.

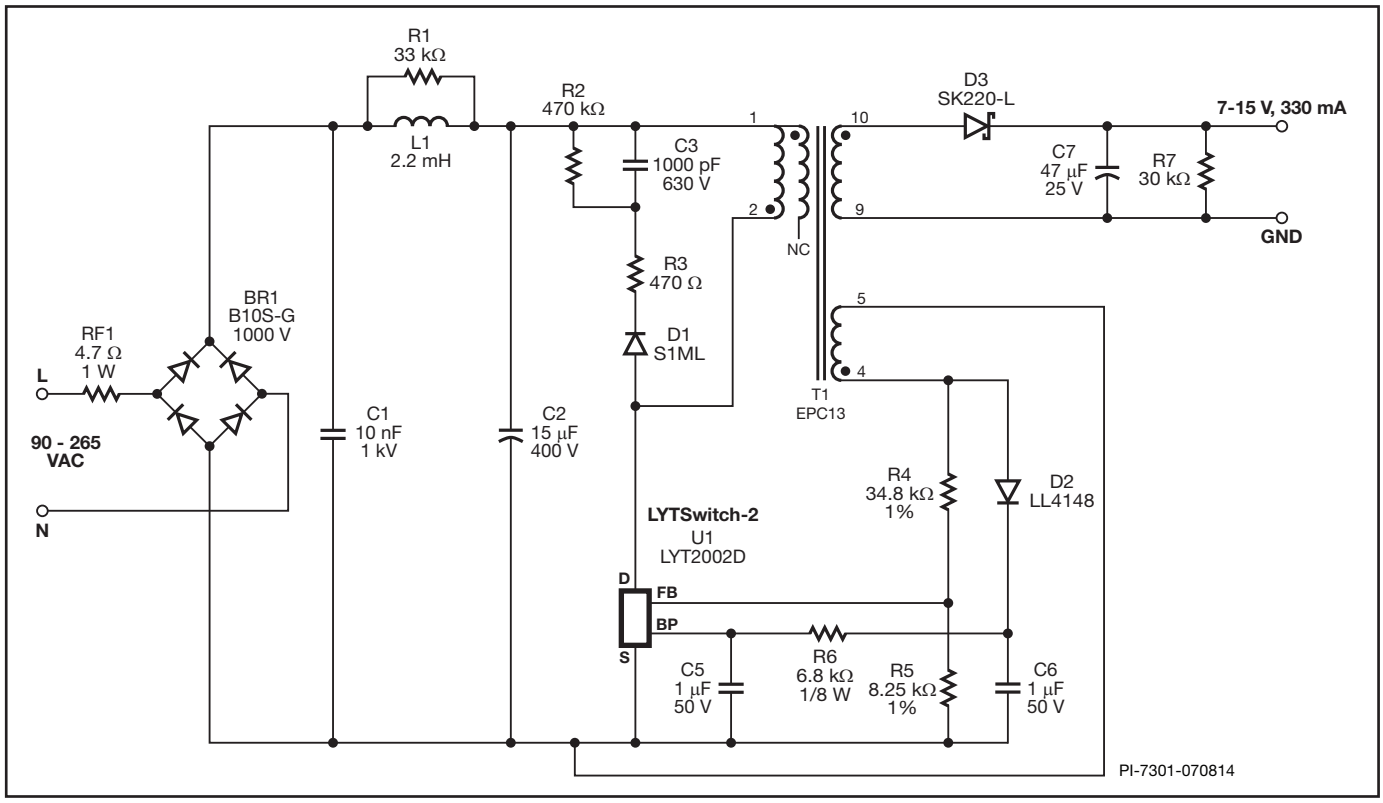


Figure 16. Typical 5 W LYTSwitch-2 Flyback Power Supply.

where V_{BIAS} (10 V typical) is the voltage across C5, I_{S2} (0.55 mA typical) is the IC supply current, and V_{BP} (6.4 V typical) is the BYPASS pin voltage. The parameters I_{S2} and V_{BP} are provided in the parameter table of the LYTSwitch-2 data sheet. Diode D6 can be a low-cost diode such as FR102, 1N4148, or BAV19/20/21. The diode voltage stress can be derived from the Feedback Winding Parameter section of the design spreadsheet which is the sum of V_{FLY} and V_{FOR} values.

If the feedback winding voltage (V_{FLY} in the design spreadsheet) is >10 V an additional winding is not required. In this case, connect D6 directly to the feedback winding at pin 2 of the transformer and eliminate the bias winding between pins 1 and 2.

FEEDBACK Pin Resistor Values

Initial Values

Resistors R_{UPPER} and R_{LOWER} form a resistor divider network that sets the voltage on the FEEDBACK (FB) pin during both the on-time and off-time of the internal MOSFET.

During CV operation the controller regulates the FEEDBACK pin voltage using an ON/OFF state-machine. The FEEDBACK pin voltage is sampled 2.5 µs after the turn-off of the internal MOSFET. At light loads the current limit reduces to decrease the transformer flux density which eliminates audible transformer noise and maintain high efficiency.

During CC operation the switching frequency is adjusted as the FEEDBACK pin voltage changes, providing constant output current regulation. During the MOSFET on-time the FEEDBACK pin voltage is used to monitor the DC input voltage and thereby minimizes CC variation with input line range.

The initial values of R_{UPPER} and R_{LOWER} are provided in cells [D43] and [D44]. Once a prototype has been built and tested follow the Fine-Tuning procedure (described below) to determine the final resistor values. Use the closest 1% values for best results. Place R_{UPPER} and R_{LOWER} as close as possible to the FEEDBACK pin.

Fine-Tuning FEEDBACK Pin Values

After building a prototype power supply the Fine Tuning section of the design spreadsheet (Figure 15) can be used to optimize the design. Enter the actual values used for feedback resistors R_{UPPER} and R_{LOWER} in cells [B103] and [B104], and the measured power supply output voltage and current at peak output power in cells [B105] and [B106]. The PIXIs spreadsheet will calculate the feedback resistor values for R_{UPPER_FINE} and R_{LOWER_FINE} to center both the output voltage and current.

Series Number	Type	Voltage Range (V)	Currnt Rating (A)	Package
1N5817 thru 1N5819	Schottky	20-40	1	Leaded
SB120 thru SB1100	Schottky	20-100	1	Leaded
1N5820 thru 1N5822	Schottky	50-60	1	Leaded
MBR320 thru MBR360	Schottky	20-40	3	Leaded
SK12-L thru SK110-L	Schottky	20-100	1	SMD
SK22-L thru SK220-L	Schottky	20-200	2	SMD
SK1150-L thru SK1200-L	Schottky	150-200	1	SMD
UF4002 thru UF4006	Ultrafast	100-600	3	Leaded
UF5401 thru UF5408	Ultrafast	100-800	3	Leaded
ES1A thru ES1D	Ultrafast	50-200	1	SMD
ES2A thru ES2D	Ultrafast	50-200	1	SMD
US1A thru US1M	Ultrafast	50-1000	1	SMD

Table 8. List of Recommended Diodes That May be Used with LYTSwitch-2 Designs.

Step 8 – Selection of Output Diode and Pre-Load

The output rectifier diode should be either a fast or an ultrafast recovery PN-junction or Schottky-barrier type.

Select a diode with sufficient voltage margin (VR). Typically VR ≥ 1.2 × PIVs, PIVs is showing the Voltage Stress Parameters section of the PIXIs spreadsheet. Once a prototype is completed use an oscilloscope to confirm the actual diode stress at VAC_{MAX}.

Select the diode with the closest continuous rating to 2 × I_O, where I_O is the output current. Use a larger diode, if necessary, to meet thermal or efficiency requirements.

Table 8 lists some suitable Schottky and ultrafast diodes that may be used with LYTSwitch-2 circuits.

As the output voltage is sampled at the switching frequency, a minimum switching frequency is maintained at no-load to give good transient load response. Therefore, if the supply can operate unloaded, a pre-load resistor is necessary to prevent the output voltage from rising below 10 mW load (see resistor R7 in Figure 16). Select a value that represents a load of approximately 10 mW at the nominal output voltage. For example, for a 24 V output use a pre-load resistor value of 57.6 kΩ.

For designs where the output voltage can rise under no-load, select the pre-load resistor value such that the output voltage remains within the maximum output voltage limit. Limit the maximum voltage rise at no-load to less than 50% of the normal output voltage to minimize no-load input power due to increases in the primary clamp and bias winding dissipation.

Step 9 – Selecting the Output Capacitor and Optional Post Filter

Select the capacitor voltage to be ≥1.2 × $V_{O(MAX)}$.

Select the capacitor using the maximum allowable equivalent series resistance (ESR) expression below:

$$ESR_{MAX} = \frac{V_{RIPPLE(MAX)}}{I_{SP}}$$

Where $V_{RIPPLE(MAX)}$ is the maximum specified output ripple and noise and I_{SP} is the secondary peak current from the Transformer Secondary Design Parameters section of the design spreadsheet.

The absolute minimum capacitance (excluding the effect of ESR) is given by:

$$C_{OUT(MIN)} = \frac{I_{O(MAX)}\left(\frac{1}{F_S} - D_{CON}\right)}{V_{RIPPLE(MAX)}}$$

Where $I_{O(MAX)}$ is the maximum output current, F_S is switching frequency, D_{CON} is the output diode conduction time and $V_{RIPPLE(MAX)}$ is the maximum allowable output ripple voltage.

Verify that the ripple current rating of the capacitor is greater than or equal to the I_{RIPPLE} value (from the Transformer Secondary Design Parameters section of the design spreadsheet). If not, select the smallest capacitance value that meets the I_{RIPPLE} requirement. Many capacitor manufacturers provide factors that increases the ripple current rating as the capacitor operating temperature rises. This information can be used to reduce capacitor size.

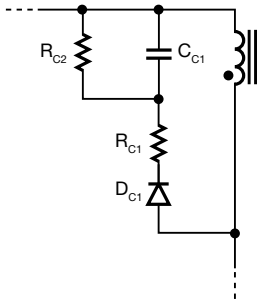
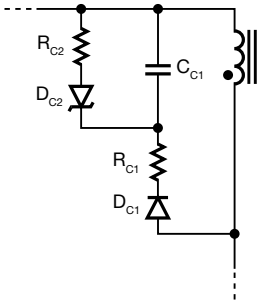
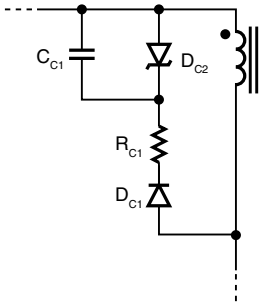
Common Primary Clamp Configurations		
RCD	**RCDZ (Zener Bleed)**	**RDZ (Zener)**
 PI-5107-110308	 PI-7315-070814	 PI-5109-041308
D_{C1}: 1N4007, 1 A, 1000 V R_{C1}: 100 Ω - 300 Ω, 1/4 W C_{C1}: 470 pF - 1000 pF R_{C2}: 330 kΩ - 680 kΩ, 1/2 W	D_{C1}: 1N4007, 1 A, 1000 V D_{C2}: BZY97Cxxx (xxx = 90 V to 120 V) R_{C1}: 100 Ω - 300 Ω, 1/4 W R_{C2}: 47 kΩ - 150 kΩ, 1/2 W C_{C1}: 470 pF - 1000 pF	D_{C1}: 1N4007, 1 A, 1000 V R_{C1}: 100 Ω - 300 Ω, 1/4 W C_{C1}: 470 pF - 1000 pF (optional) D_{C2}: P6KExxx (xxx = 150 V to 200 V)

Table 9. Primary Clamp Configurations Suitable for LYTSwitch-2 Designs.

To reduce the physical size of the output capacitor an output LC post filter can be used to reduce the ESR related switching noise. In this case, select either a 1 µH to 3.3 µH inductor with a current rating greater than or equal to I_O. A ferrite bead can be used for designs with I_O of less than approximately 1 A. The second capacitor is typically 100 µF or 220 µF with low ESR for good transient response. As the secondary ripple current does not pass through this capacitor there are no specific ESR or ripple current requirements.

The output capacitor required may also be split between two capacitors. Here the overall ripple current rating is equal to the sum of the ratings of each capacitor.

Step 10 – Selection of Primary Clamp Components

Three common primary clamp arrangements, shown in Table 9 is generally suitable for LYTSwitch-2 designs.

The RCD configuration is the lowest cost. For RCD and RCDZ type circuits, minimize the value of C_{C1} and maximize R_{C2} while limiting the peak drain voltage to less than 680 V. Larger values of C_{C1} may cause higher output ripple voltages due to the longer settling time of the clamp voltage impacting the sampled voltage on the feedback winding.

For RDZ configurations, CC1 is optional and helps recover some of the leakage inductance energy. Resistor RC1 dampens ringing and should be tuned to minimize undershoot (see Design Tips section) and reduce conducted EMI. The RCDZ circuit maintains the low EMI of the RCD configuration but lowers no-load input power consumption. As the current through the Zener diode is limited by R_{C2} to only a few mA's, the stress is very low, allowing the use of non-TVS Zener diodes without reliability concerns. The RDZ configuration provides lowest no-load consumption, but at the cost of higher EMI and the need for a TVS type Zener diode (rated for high instantaneous power).

Transformer Winding Arrangement Examples (Including E-Shields™)

Once the PIXIs spreadsheet design is complete all the necessary information is available to create a transformer design. In this section some practical tips are presented on winding order and how to use Power Integrations proprietary E-Shield techniques. Shield windings improve conducted EMI performance and simplify the input filter stage by eliminating the need for a common mode choke and reducing the value of or eliminating the Y-class capacitor connected between the primary and secondary. Refer to Figures 17 and 18 to reference winding numbers (WD1).

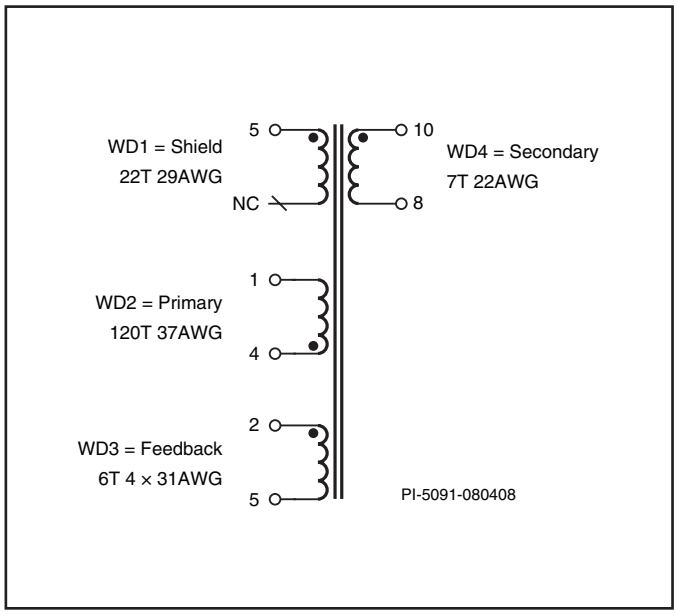


Figure 17. Typical Transformer Schematic with E-Shield (WD1).

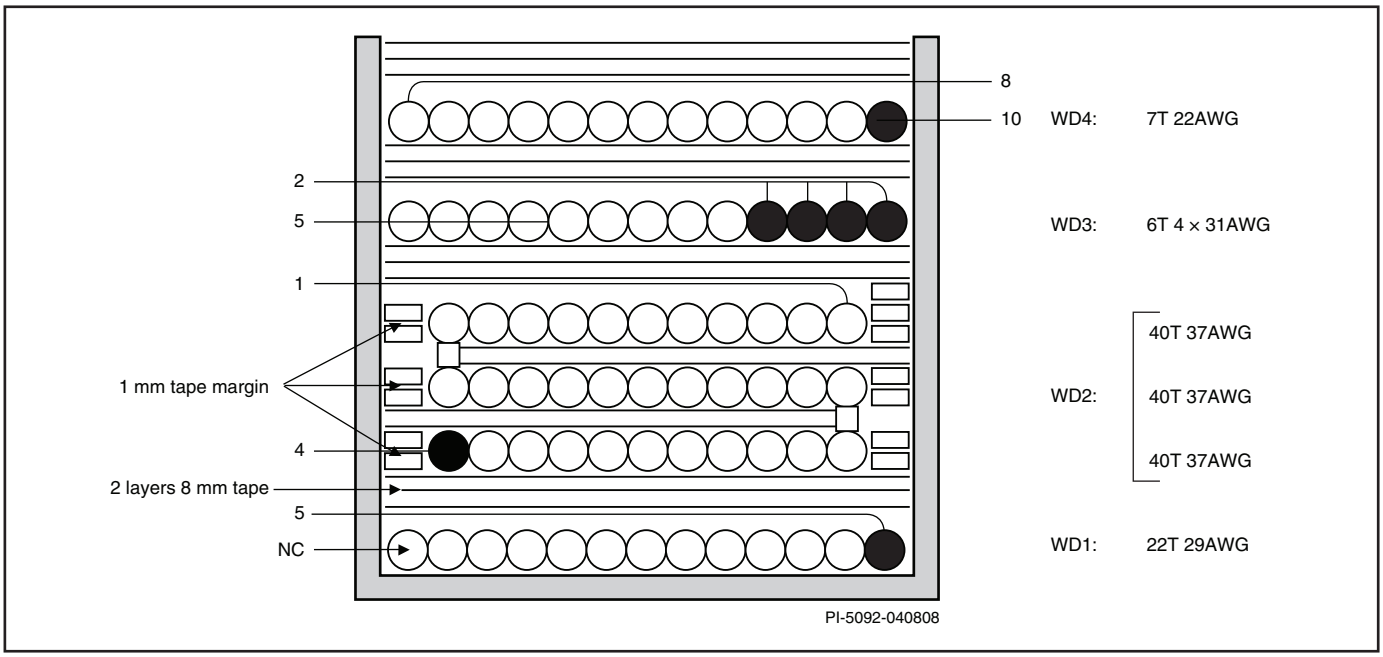


Figure 18. Typical Mechanical Construction of LYTSwitch-2 Transformer with Shield Winding.

Shield Winding

The first layer of the transformer is a shield winding (WD1). Calculate the number of turns by taking the number of primary turns NP [D74] from PIXls and dividing it by the number of layers L [D56]. Divide the result by 2 (NSHEILD = 0.5 × (NP/L)). This gives a starting value. Note that the start (black dot) of the shield winding is on the opposite side of the bobbin to the start of the primary winding. The finish end of the shield winding is floating. Select a wire gauge that completely fills the bobbin width.

Primary Winding

The second winding (WD2) is the primary. From PIXls find the number of turns NP [D74], number of layers L [D56] and the wire gauge AWG [D86]. A 1 mm tape layer can be used to improve EMI repeatability by making the transformer design less sensitive to production variation. To include the tape margin, enter a margin value of 1 mm into cell [B55] of the PIXls spreadsheet.

Feedback Winding

The feedback winding is the third winding (WD3) on the bobbin. From PIXls find the number of turns NFB [D30]. To reduce conducted EMI emissions, this winding must cover the complete bobbin width. A multi-filar winding is used to achieve this and some experimentation may be needed to find the optimum wire gauge and number of parallel winding wires. Generally more than 4 filar is not recommended due to manufacturability considerations when multi-filar windings are terminated onto a single bobbin pin.

Secondary Winding

The final winding is the Secondary Winding (WD4). From PIXls find the number of secondary turns NS [D57]. Start the secondary winding on the same side of the bobbin as the start of the feedback winding. Select a wire gauge to completely fill the width of bobbin winding window. Triple-insulated wire is recommended for the secondary winding to avoid the need for wide tape margins to meet safety spacing requirements (6 mm to 6.2 mm typical) and minimize the transformer core size required.

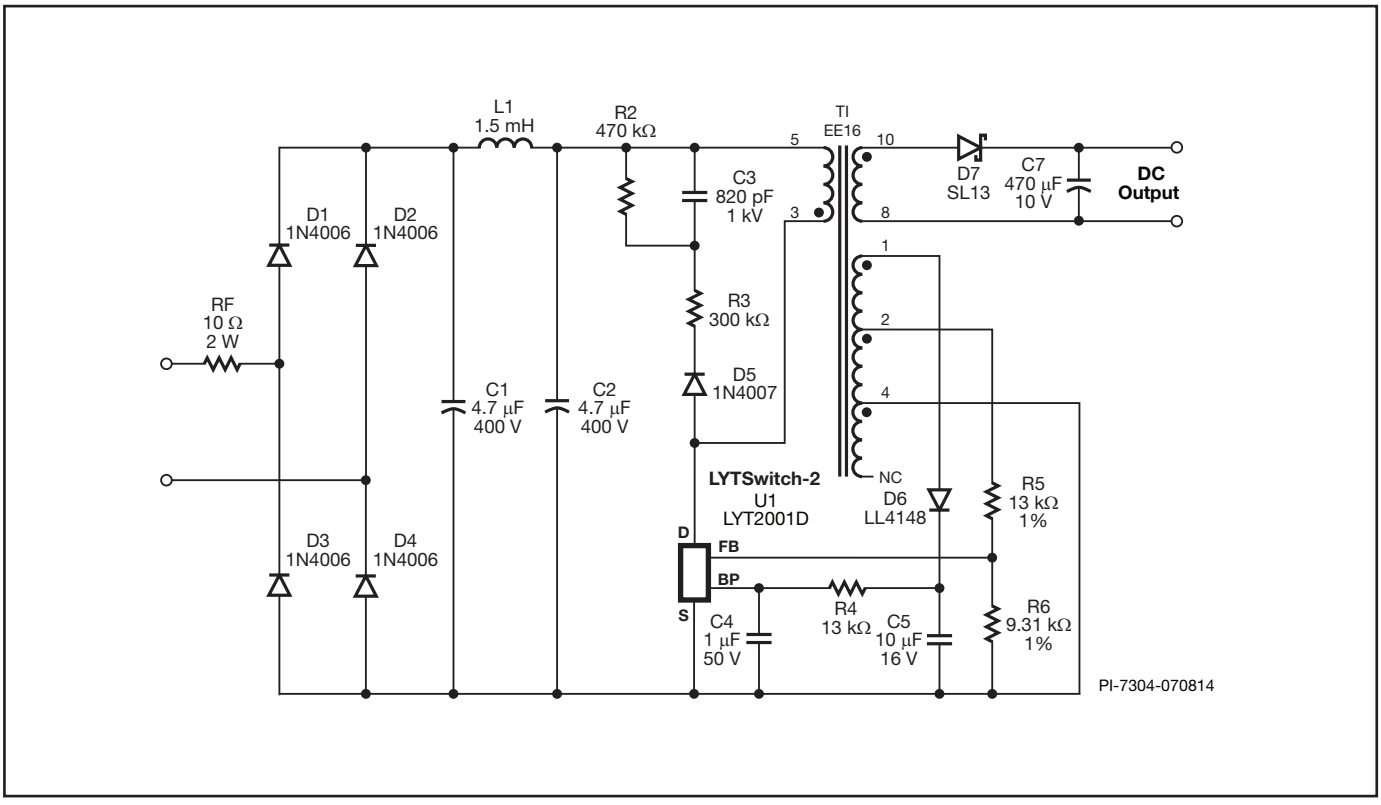


Figure 19. LYTSwitch-2 Flyback Power Supply with Bias Circuit for Reduced No-load Input Power and Higher Light Load Efficiency.

Example of a Transformer with the Additional Bias Winding
Figures 20 and 21 show the schematic and build diagram, respectively, for a transformer that requires a bias winding.

The construction technique for this transformer is the same as that for a transformer without a bias winding, except the bias winding is inserted between the primary and the feedback winding layers. The number of additional turns added to the feedback winding is (NB) shown in cell [D37] of PIXls.

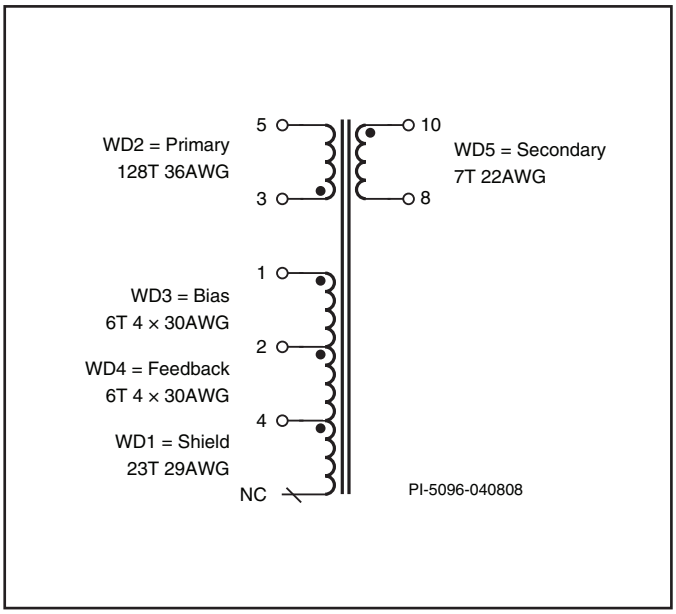


Figure 20. Transformer Schematic with Additional Bias Winding.

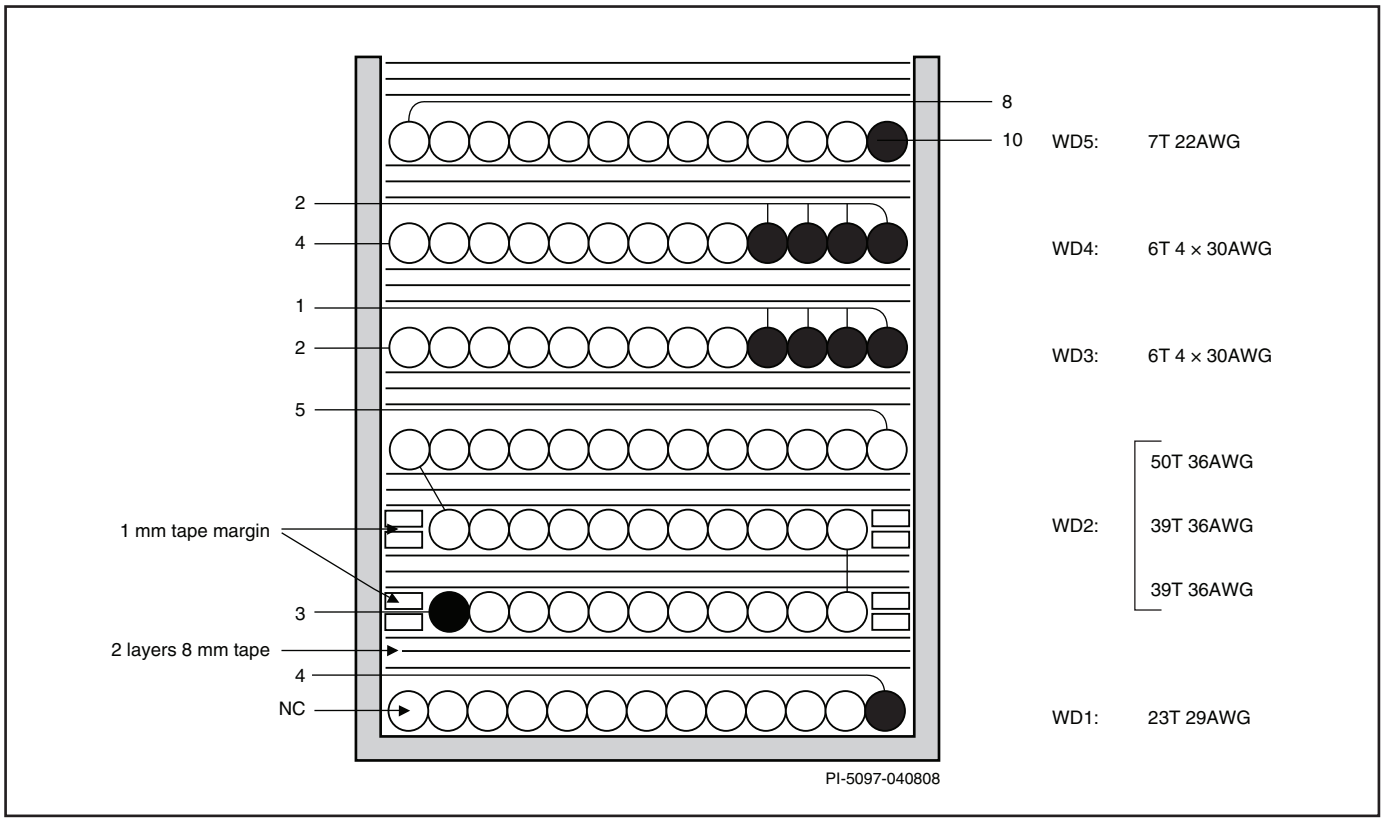


Figure 21. Transformer with Additional Bias Winding and Shield Winding Build Diagram.

Design Tips

Reflected Output Voltage (V_{OR}) Adjustment

Users of design spreadsheets for other Power Integrations device families may notice that some critical parameters (K_P, V_{OR}, N_S and N_P) cannot be changed directly in the LYTSwitch-2 spreadsheet. To change these parameters, use the relationships shown below:

- K_P: Reducing F_S or increasing C_{IN} will increase K_P.
- V_{OR}: Increasing D_{CON} or F_S will decrease the value of V_{OR}
- N_S: Increasing D_{CON} will increase N_S
- N_P: Determined by $B_{M(TARGET)}$

Output Tolerance

Each LYTSwitch-2 device is factory-trimmed to ensure a very accurate initial CC tolerance using a representative power supply test module. This is represented in the data sheet by the parameter I_O, Normalized Output Current.

The accurate tolerances of the FEEDBACK pin voltage (V_{FBth}) and small temperature coefficient (TCVFB) provide accurate regulation of the output voltage during CV operation.

In the E and K package, LYTSwitch-2 provides an accurate output over all tolerances (including line, component variation, and temperature) for the output voltage in CV operation and ±5% for the output current during CC operation, over a junction temperature range of 0 °C to 100 °C.

For the D package (SO-8C) additional CC variance may occur due to stress caused by the manufacturing flow (i.e. solder-wave immersion or I_R reflow). A sample power supply build is therefore recommended to verify production tolerances for each design.

Design Recommendations

Circuit Board Layout

The LYTSwitch-2 family of IC's presents a highly integrated power supply solution that integrates, both, the controller and the high-voltage power MOSFET onto a single die. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply. See Figure 22 and 23 for the recommended circuit board layout for LYTSwitch-2 E and SO-8C package respectively (K package is similar in layout to an SO-8C).

When designing a printed circuit board layout for the LYTSwitch-2 based power supply, it is important to follow the following guidelines:

Single-Point Grounding

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LYTSwitch-2 SOURCE pin and bias-winding return. This improves surge and ESD immunity by returning surge currents from the bias winding directly to the input filter capacitor.

BYPASS Pin Capacitor

The BYPASS pin capacitor should be located as close as possible to the SOURCE and BYPASS pins.

FEEDBACK Pin Resistors

Place the feedback resistors directly adjacent to the FEEDBACK pins of the LYTSwitch-2 device. This minimizes noise coupling. A R_{UPPER} should be located as close as possible to the FEEDBACK pin and R_{LOWER} between the SOURCE and FEEDBACK pins.

Thermal Considerations (D and K package)

The copper area connected to the SOURCE pins provides heat sinking. A good estimate of expected power dissipation is to

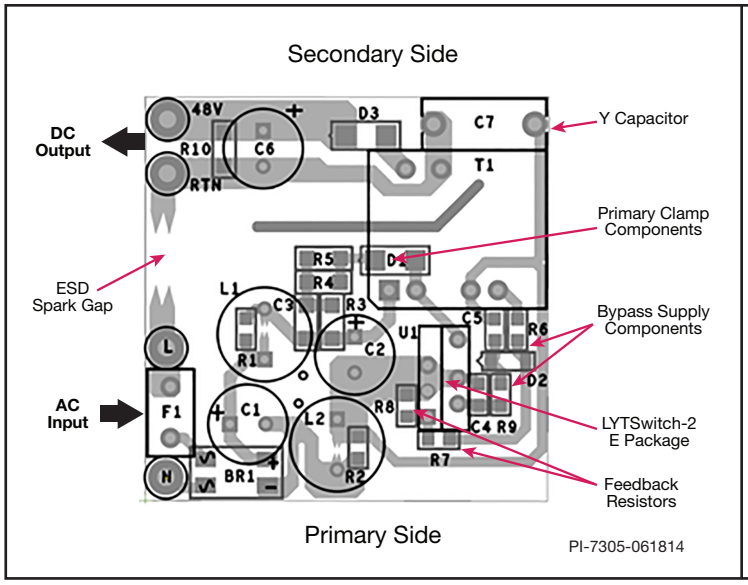


Figure 22. PCB Layout Example using eSIP Package.

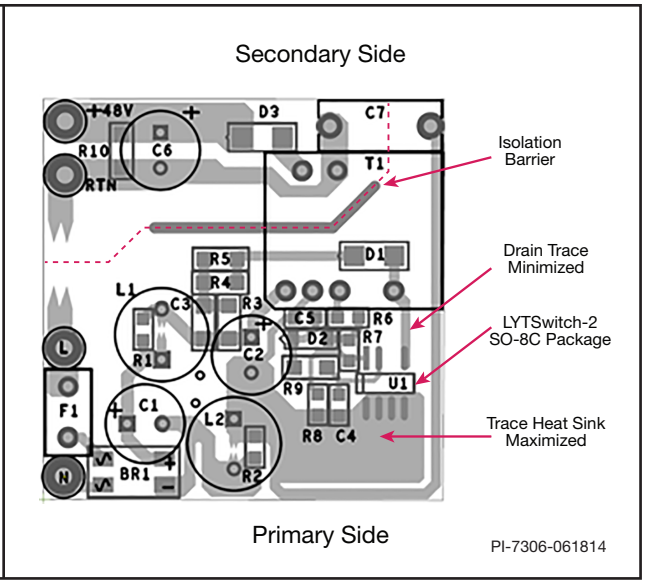


Figure 23. PCB Layout Example using SO-8C Package.

assume that the LYTSwitch-2 will dissipate 5% of the output power. Provide enough copper area to keep the SOURCE pin temperature below 100 °C.

Higher temperatures are allowable but output current (CC) tolerance will increase.

Secondary and Bias Loop Area
To minimize reflected trace inductance and EMI, minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, provide sufficient copper area at the anode and cathode of the diode for heat sinking. Provide a larger area at the quiet cathode terminal as a large anode area can increase high frequency radiated EMI.

Apply the same layout consideration for the bias supply loop area.

Electrostatic Discharge Spark Gap
A trace is placed at one of the AC line inputs to form one electrode of a spark gap. The other electrode on the secondary is formed by the output return node. The spark gap directs most ESD energy from the secondary back to the AC input during a surge event. The trace from the AC input to the spark gap electrode should be spaced away from other traces to prevent damage. In Figure 22, if R1 and R2 are removed additional spark gaps across the EMI filter inductors (L1 and L2) should be included to prevent excessive build-up of voltage across them during surge and damage due to internal arcing.

Drain Clamp Optimization
LYTSwitch-2 senses the feedback winding on the primary-side of the isolation barrier to regulate the output. The voltage that appears on the feedback winding is a reflection of the secondary winding voltage while the internal MOSFET is off. Therefore, any leakage-inductance-induced ringing can affect output regulation.

Optimizing the drain clamp to minimize high frequency ringing gives the best regulation. Figure 24 shows the desired drain voltage waveform. Compare this to Figure 25 with a large undershoot, caused by ringing due to leakage inductance. This ringing, and its effects, degrades output voltage regulation. To reduce this ringing (and the undershoot it causes) adjust the value of the resistor in series with the clamp diode.

Y Capacitor Connection
When using a Y capacitor the recommended connection across the transformer is the bulk (+) input in the primary and secondary output winding return as shown in Figure 26. However, connecting to bulk (-) in the primary is not uncommon in this area so follow the single-point grounding layout recommendation where the connection should be directly at the negative terminal of the input filter capacitor.

Quick Design Checklist

As with any power supply design, verify your LYTSwitch-2 design on the bench to make sure that component specifications are not exceeded under worst-case conditions.

The following minimum set of tests is strongly recommended:

- Maximum drain voltage – Verify that the peak V_{DS} does not exceed 680 V at the highest input voltage and maximum output power.
- Drain current – At maximum ambient temperature, maximum and minimum input voltage and maximum output load, review drain current waveforms at start-up for any signs of transformer saturation or excessive leading edge current spikes. LYTSwitch-2 devices have a leading edge blanking time to prevent premature termination of the ON-cycle, but limit leading edge spikes to less than the maximum specified in the data sheet.

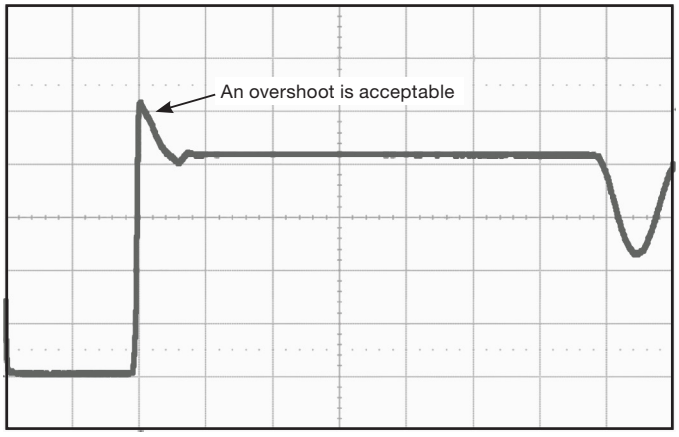


Figure 24. Desired Drain Voltage Waveform with Minimal Leakage Ringing Undershoot.

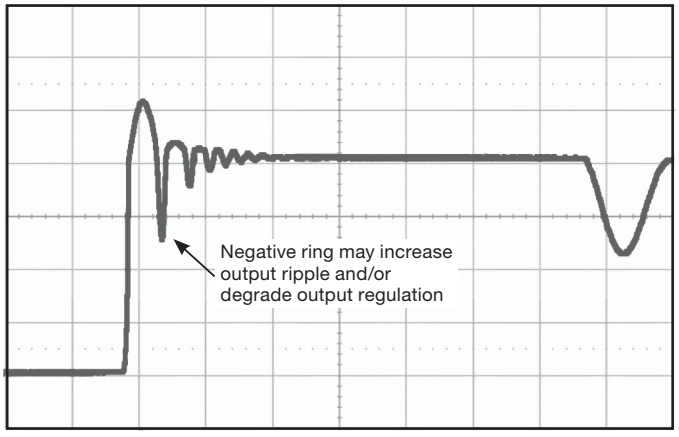


Figure 25. Undesirable Drain Voltage Waveform with Large Leakage Ringing Undershoot.

- Thermal check – At maximum output power, for both minimum and maximum input voltage and maximum ambient temperature; verify that temperature limits are not exceeded for LYTSwitch-2, transformer, output diodes and output capacitors. Thermal margin should be provided to allow for part-to-part variation in the $R_{DS(ON)}$ of the LYTSwitch-2 device. For optimum regulation, a SOURCE pin temperature below 100 ºC is recommended.

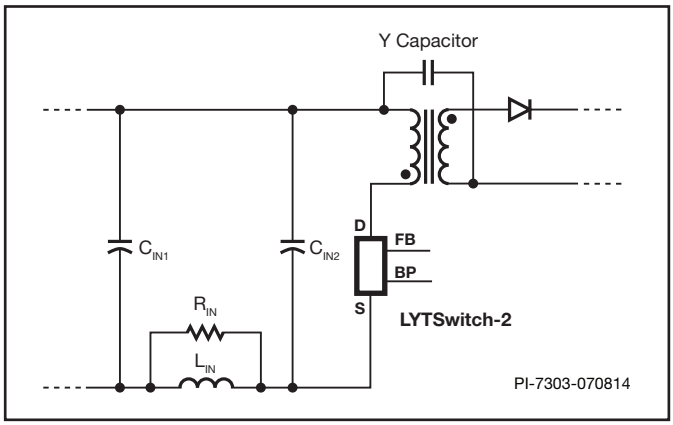


Figure 26. Correct Location of Input Inductor When using a Y Capacitor.

Revision	Notes	Date
A	Initial Release.	12/14

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