Series SDR CR-P351/P451/P101

User Manual

Version Records:

Data	Version	Description
2023.05.25	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

Content

Part 1: Product Overview

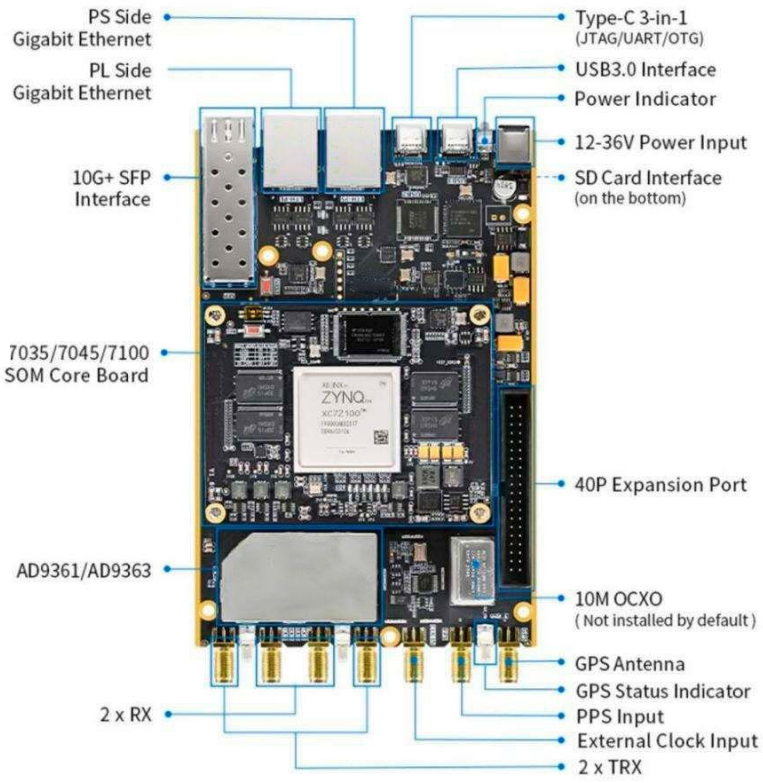
Part 1.1: Product Overview

This article introduces the CR-P351/P451/P101, these three hardware is fully compatible, direct software replacement can be used. The CR-P351/P451/P101 used XILINX's XC7Z035-2FFG900I, XC7Z045-2FFG900I and XC7Z100-2FFG900I as the main controller, equipped with ADI's AD9361 RF chip constitutes the main structure of the product. The main difference between these three is that the logic resources of the processor are different, so users can choose the corresponding products according to the actual requirements.

The CR-P351/P451/P101 integrated a variety of RF and other hardware interfaces, rich resources, easy to use, the following Product Function Block Diagram is an overview of the internal resource structure, it adopts the SOM (core board) and the carrier board, direct replacement of the SOM (core board) can be completed to replace and update.

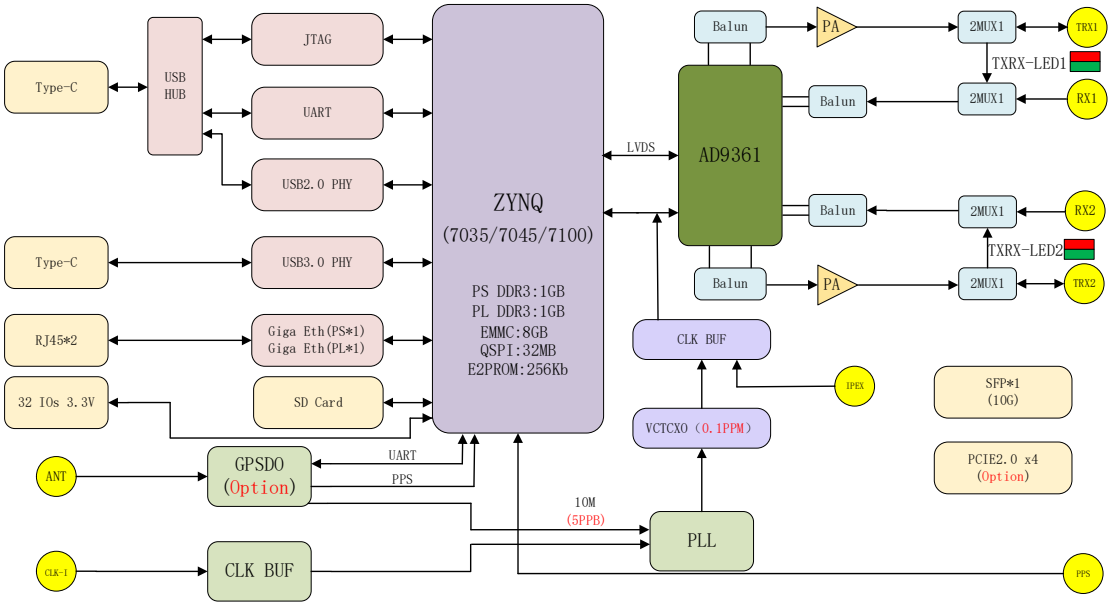
The PCBA Board Form Factors is 155mm * 100mm (6.10 inch * 3.94 inch), and the customized shell form factor is 162mm * 105mm (6.38inch * 4.13inch), the whole shell also plays a role in heat dissipation, to ensure the stable operation of the product.

The product is designed in accordance with industrial-grade standards, operating temperature -40℃-85 ℃, using a 0.1ppm high-precision clock, all interfaces are made of static electricity protection.



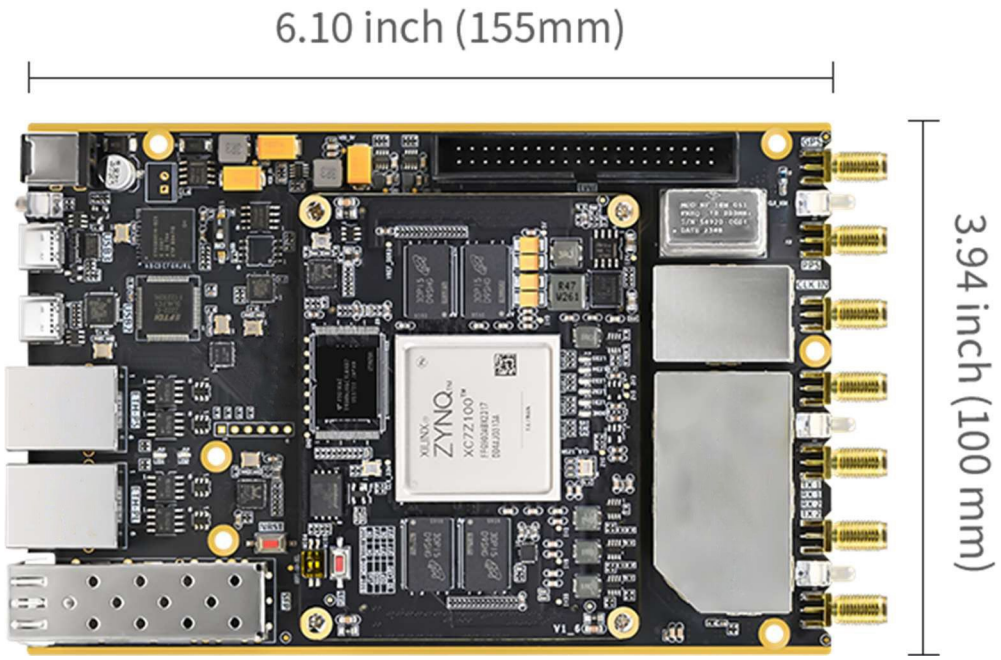
Part 1.2: Product Function Block Diagram

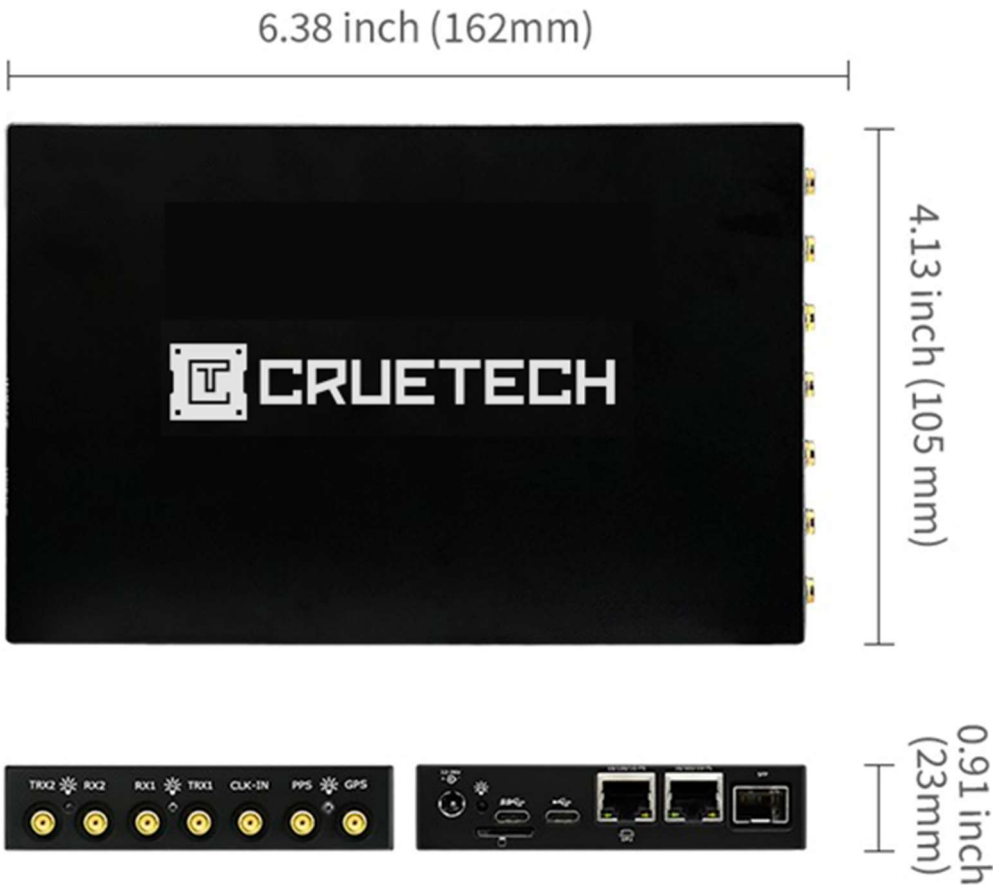
In this section, we will show the configuration details of the product in detail through the product block diagram and product specifications, as shown below.



Part 1.3: Form Factors

PCBA Board form factors is 155mm * 100mm, and the customized shell form factor is 162mm * 105mm




6.38 inch (162mm)
4.13 inch (105 mm)
CRUETECH
TRX2
RX2
RX1
TRX1
CLK-IN
PPS
GPS
0.91 inch
(23mm)

Part 2: SOM FPGA Core Board

Part 2.1: SOM Introduction

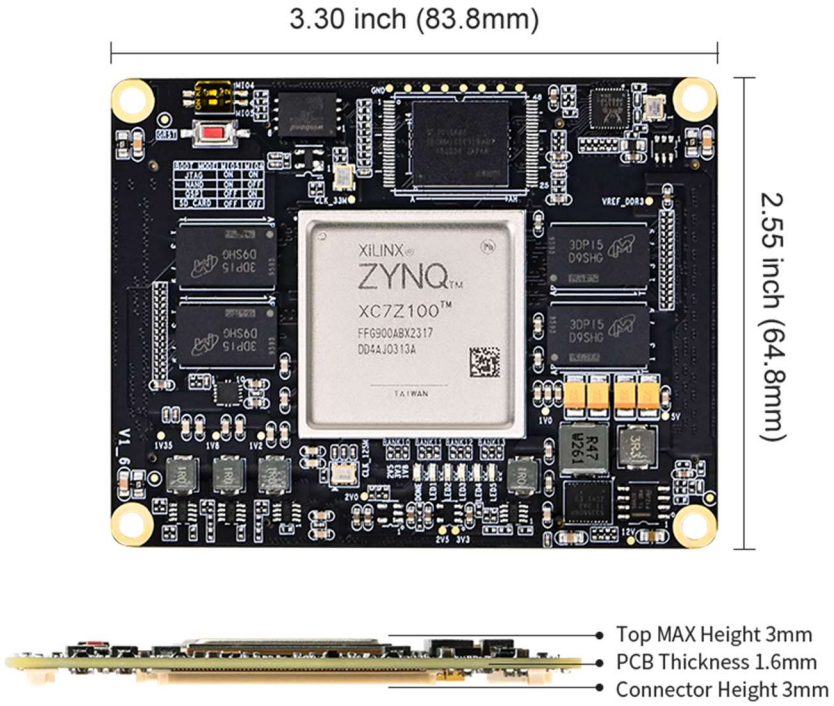
The CR7035/45/100 core board adopts XILINX's Zynq7035/7045/7100 chip as the main controller. The core board is connected with the carrier board by four gold-plated connectors with a spacing of 0.6mm and 120P. Four 3.5mm fixing holes are placed on the four feet of the core board, which can be fastened with the carrier board by screws. That is to to ensure stable operation in the environment of strong vibration, in addition, the core board uses industrial grade components, stable operation from -40°C to +85°C.

CR-P351/ P451/ P101 Industrial Grade SOM Specification			
FPGA	XC7Z035-2FFG900I	XC7Z045-2FFG900I	XC7Z100-2FFG900I
Processor Core	Dual-Core ARM Cortex-A9, Main Frequency 800Mhzz		
Logic Cells	275K	350K	444K
Look-up Tables (LUTs)	171900	218600	277400
Flip-Flops	343800	437200	554800
DSP Slices	900	900	2020
Block RAM	17.6Mb	19.2Mb	26.5Mb
DDR3/DD3L	PS-side 1GB, PL-side 1GB		
QSPI FLASH	32Mb, to store startup files and user files		
EMMC	8GB, to store startup files and user files		
Start Method	JTAG/QSPI/NAND/SD, onboard DIP switch selection		
Gigabit Ethernet	1 (PS Side)		
User LED	5		
IO Number			
Number of GTX ports	BANK, 16 Paris of TX/RX each		
Working Voltage/Max. Current	8-12V/2A (8V recommended)		
Working Temperature	-40°C~+85°C		
Form Factors Technology	83.8 x 63.8mm, Immersion Gold Process 0.6mm 120P Connectors X 4		
Connectors Height	3mm		

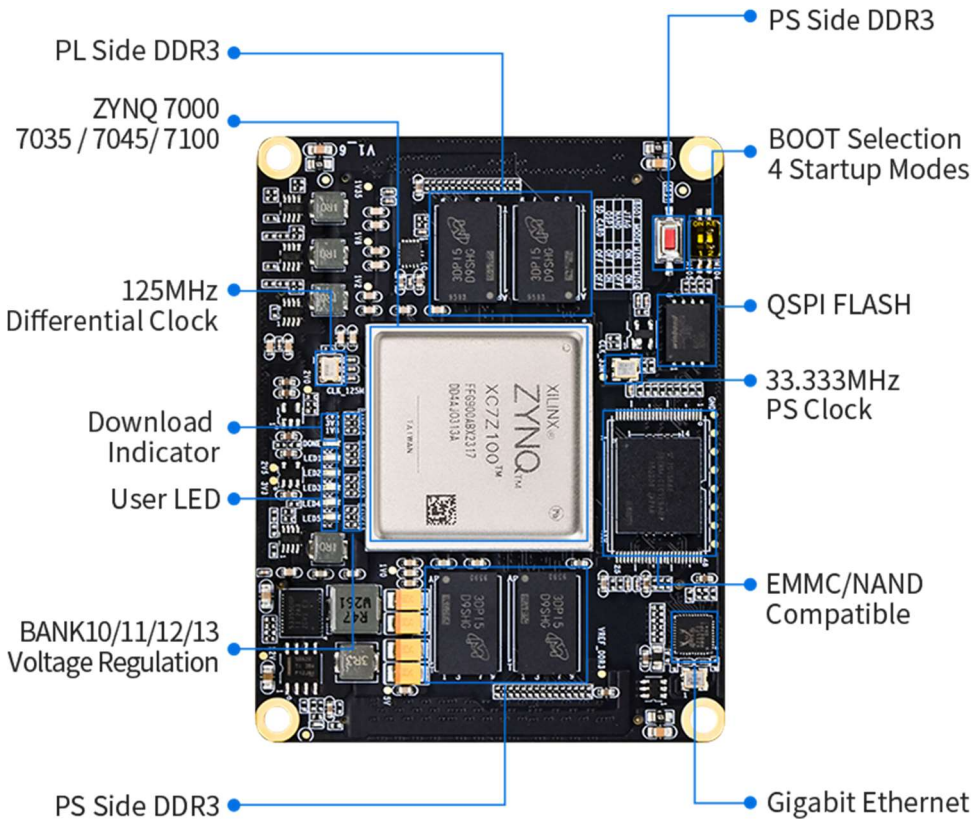
Part 2.2: SOM Form Factors and Specification

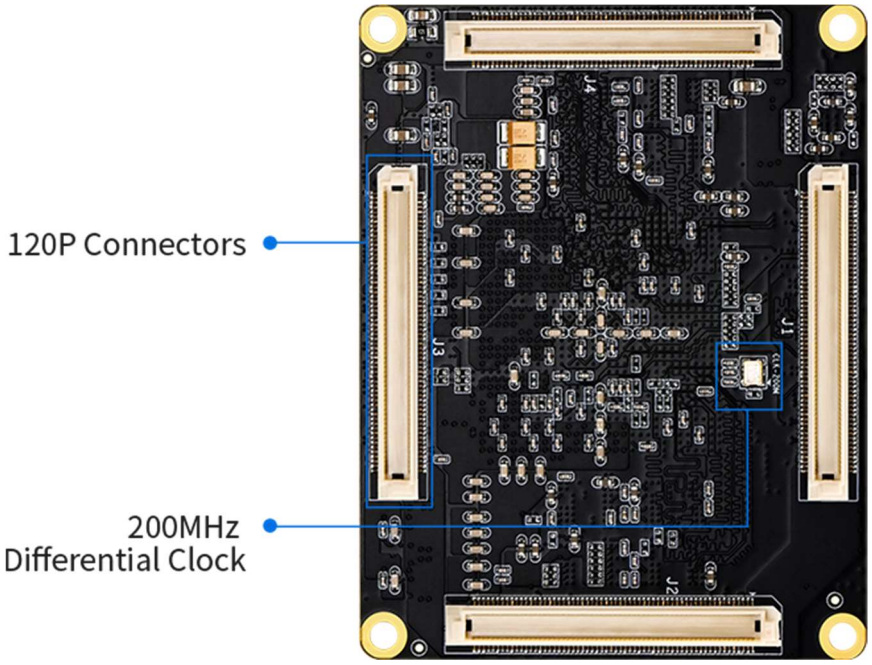
The core board form factors is 83.8 mm x 64.8mm (3.30 inch x 2.55 inch). The core board

is connected to the carrier board via four 0.6mm/120P gold-plated high-speed connectors on the reversal side.



The following figure shows the location of each major electronic component on the core board for easy identification.



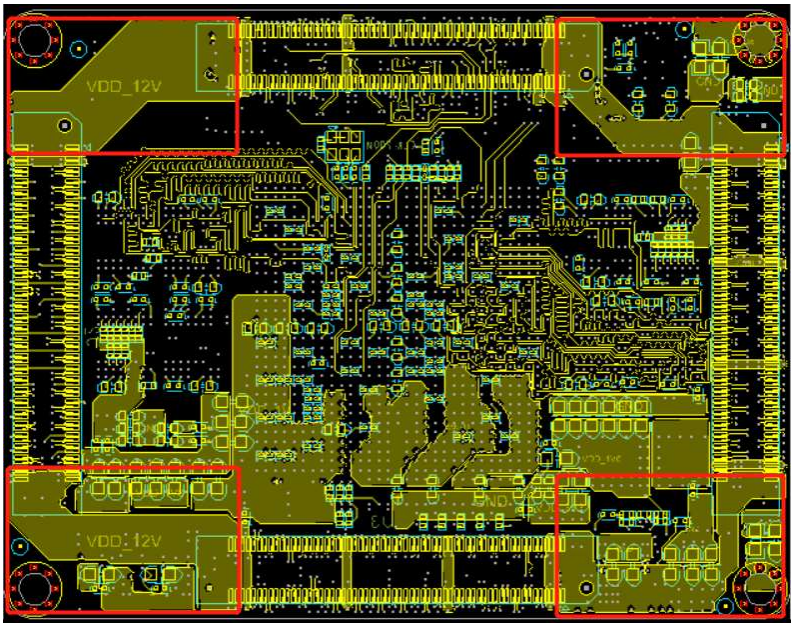


Part 2.3: Power Connection

The power supply voltage range of the FPGA core board is 7-12V. The Power input pins are reserved at the four corners of the module, and the power pins have been connected inside the module. When designed, it only needs to connect the power pin core board at one corner to work. The power connection needs to be connected with copper and enough holes are made to ensure the power flow ability. All GND signals on the module need to be connected to the base plate, and each GND is connected to the carrier board through two through-holes to ensure through-flow capability.

The output voltage of the power supply supplying the module needs to be stable. If the power supply is unstable, one stage of DCDC should be added before the input of the module power supply to switch from high voltage to low voltage. The current output capacity of DCDC can be about 4A.

Two **220uF/ 25V-470uF /25V** capacitors should be placed in the power input of the core board to ensure the quality of the power supply. Since the current of the core board is relatively large, it is recommended to use DCDC power supply alone for the core board if the cost permits, and use another power supply for other peripherals. The power supply should be separated.

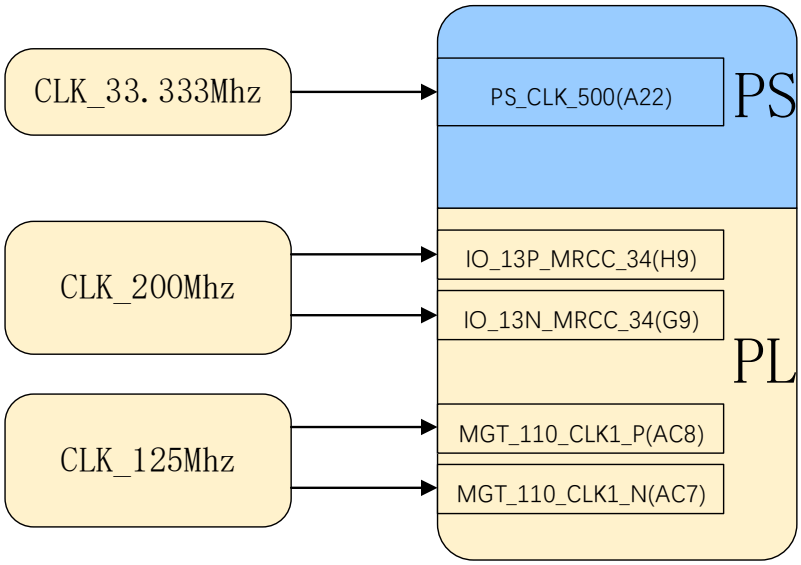


Part 2.4: System Clock

The core board provides a clock input of 33.333333Mhz for the PS side, and the input pin position is PS_CLK_500. The 200Mhz differential clock input is provided for the PL side. The clock input pin of the PL side is FPGA_13P_MRCC_34/FPGA_13N_MRCC_34, and the pin position is H9/G9. The 125Mhz differential clock input is provided for GTX, the input position is CLK1 of BANK110 GTX, and the pin number is AC8/AC7. The connection mode is listed in the following figure.

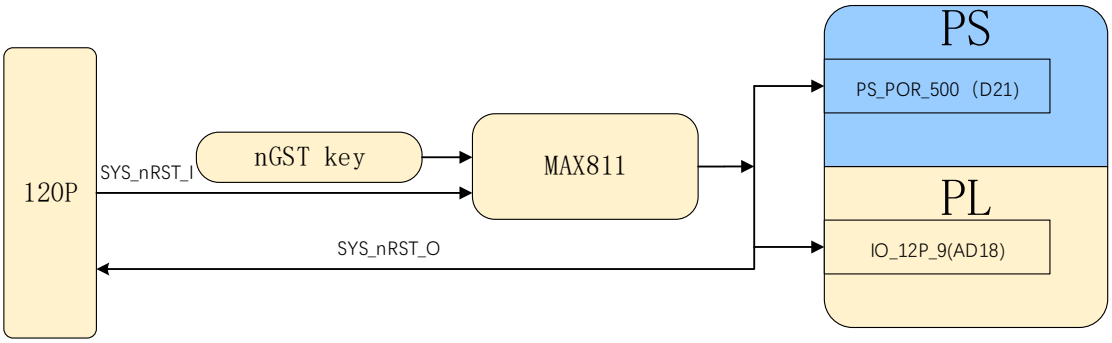
Note that the GTX CLK on the core board can be used to Bank109/110/111

If BANK112 is used, it is necessary to add a differential 125M clock on the carrier board, you can refer to the FPGA development board schematic diagram connected to the clock circuit of BANK112.



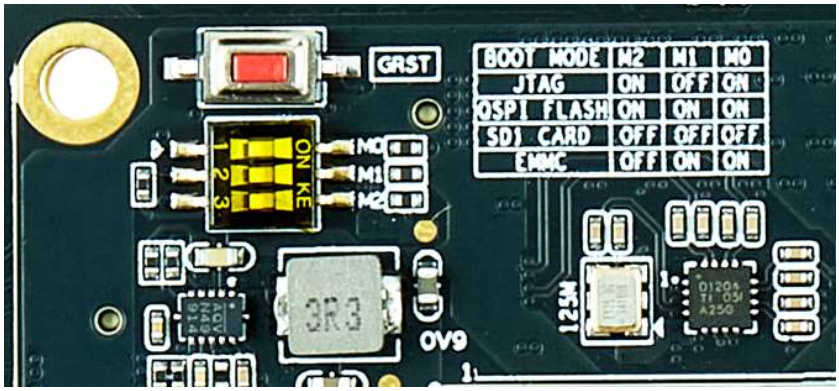
Part 2.5: Global Reset

nGST reset key is provided on the core board, which is the system reset key and is active in low level. This pin also leads to the connector, with the signal name **SYS_nRST_I**, to facilitate the user to add a reset key or design a watchdog reset circuit. At the same time, in order to stabilize the system, we add a reset chip on the core board, and the reset output signal is also led to the connector, the signal name is **SYS_nRST_O**, this signal can be used for the reset of other peripherals on the board, the signal level is 3.3V. The reset pin is shared by **PS/PL** side and is connected to **PS_POR_500** on PS side and **IO_12P_9** (pin position **AD18**) on PL side respectively.



Part 2.6: Boot Mode Selection

The core board supports four boot modes, namely JTAG, QSPI Flash, NAND FLASH (no NAND by default, it is EMMC), and SD card. The first three modes are installed on the board, and users can realize the SD card mode by connecting on the carrier board. Four startup methods can be selected through the onboard DIP switch. The following figure has listed the position of each mode DIP switch.



Part 2.7: SOM DDR3

The PS side is equipped with two industrial-grade DDR3L chips, a single capacity of

512MB, two total capacity of 1GB, model MT41K256M16TW-107IT:P, DDR3L pin allocation can directly call the system allocation. You can also refer to the Demos provided by our company.

The PL side is equipped with two industrial-grade DDR3L chips, each with a capacity of 512MB, and the total capacity of the two is 1GB, the model is MT41K256M16TW-107IT:P, DDR3L pin distribution is shown in the following table.

DDR3L Pin	Pin Name	Pin Posiion
DDR3_D0	IO-L1N-33	J3
DDR3_D1	IO-L4N-33	L2
DDR3_D2	IO-L1P-33	J4
DDR3_D3	IO-L4P-33	L3
DDR3_D4	IO-L2N-33	K1
DDR3_D5	IO-L6P-33	K6
DDR3_D6	IO-L5N-33	J5
DDR3_D7	IO-L5P-33	K5
DDR3_DM0	IO-L2P-33	L1
DDR3_DQS_P0	IO-L3P-33	K3
DDR3_DQS_N0	IO-L3N-33	K2
DDR3_D8	IO-L11P-33	H4
DDR3_D9	IO-L10N-33	G1
DDR3_D10	IO-L8P-33	H6
DDR3_D11	IO-L7N-33	F2
DDR3_D12	IO-L10P-33	H2
DDR3_D13	IO-L12N-33	G4
DDR3_D14	IO-L8N-33	G6
DDR3_D15	IO-L11N-33	H3
DDR3_DM1	IO-L12P-33	G5
DDR3_DQS_P1	IO-L9P-33	J1
DDR3_DQS_N1	IO-L9N-33	H1
DDR3_D16	IO-L18P-33	E1
DDR3_D17	IO-L17P-33	E3
DDR3_D18	IO-L16N-33	D3
DDR3_D19	IO-L14P-33	F4
DDR3_D20	IO-L18N-33	D1
DDR3_D21	IO-L13N-33	E5
DDR3_D22	IO-L16P-33	D4
DDR3_D23	IO-L17N-33	E2
DDR3_DM2	IO-L14N-33	F3
DDR3_DQS_P2	IO-L15P-33	E6
DDR3_DQS_N2	IO-L15N-33	D5
DDR3_D24	IO-L22P-33	C2
DDR3_D25	IO-L24N-33	A2

DDR3_D26	IO-L20N-33	B4
DDR3_D27	IO-L20P-33	B5
DDR3_D28	IO-L22N-33	C1
DDR3_D29	IO-L24P-33	A3
DDR3_D30	IO-L19P-33	C4
DDR3_D31	IO-L23P-33	B2
DDR3_DM3	IO-L23N-33	B1
DDR3_DQS_P3	IO-L21P-33	A5
DDR3_DQS_N3	IO-L21N-33	A4
DDR3_A0	IO-L18P-34	H7
DDR3_A1	IO-L21P-34	L8
DDR3_A2	IO-L7N-34	H11
DDR3_A3	IO-L10N-34	D10
DDR3_A4	IO-L15N-34	H8
DDR3_A5	IO-L8N-34	D11
DDR3_A6	IO-L19P-34	L7
DDR3_A7	IO-L10P-34	E10
DDR3_A8	IO-L23P-34	L10
DDR3_A9	IO-L9P-34	H12
DDR3_A10	IO-L18N-34	G7
DDR3_A11	IO-L20N-34	J9
DDR3_A12	IO-L14P-34	F9
DDR3_A13	IO-L7P-34	J11
DDR3_A14	IO-L22N-34	K10
DDR3_BA0	IO-L22P-34	K11
DDR3_BA1	IO-L21N-34	K8
DDR3_BA2	IO-L9N-34	G11
DDR3_CS	IO-L16P-34	F8
DDR3_RAS	IO-L14N-34	E8
DDR3_CAS	IO-L17P-34	E7
DDR3_WE	IO-L16N-34	F7
DDR3_ODT	IO-L20P-34	J10
DDR3_RESET	IO-L8P-34	E11
DDR3_CLK_P	IO-L12P-34	D9
DDR3_CLK_N	IO-L12N-34	D8
DDR3_CKE	IO-L17N-34	D6

Part 2.8: QSPI FLASH Introduction

The FPGA Core board has a 32MB QSPI FLASH onboard, the model is W25Q128JVSIQ, which can be used to store startup files and user files. The following table shows the

correspondence between QSPI Flash signals and FPGA pins.

QSPI FLASH PIN	PIN Name	PIN Position
DATA0	MIO2	F23
DATA1	MIO3	C23
DATA2	MIO4	E23
DATA3	MIO5	C24
QSPI_CS	MIO1	D23
QSPI_CLK	MIO6	D24

Part 2.9: EMMC Pin Definition

The 8GB EMMC "**THGBMFG6C1LBAIL**" is placed on the FPGA core board, and the operating temperature is -40℃--+85℃. The following table shows the correspondence between the EMMC signal and the ZYNQ pin.

EMMC Pin	ZYNQ Pin Name	Pin Position
EMMC_D0	MIO10	E22
EMMC_D1	MIO13	F22
EMMC_D2	MIO14	B22
EMMC_D3	MIO15	C22
EMMC_CLK	MIO12	E21
EMMC_CMD	MIO11	A23

Part 2.10: NAND FLASH Pin Definition

NAND FLASH and EMMC adopt compatible designs on the core board. You can only choose one of the two types of welding. You need to specify the welding based on specific requirements.

FLASH Pin	Pin Name	Pin Position
DATA0	MIO5	C24
DATA1	MIO6	D24
DATA2	MIO4	E23
DATA3	MIO13	F22
DATA4	MIO9	A24
DATA5	MIO10	E22
DATA6	MIO11	A23
DATA7	MIO12	E21
RE	MIO8	C21
CE	MIO0	F24
CLE	MIO7	B24

ALE	MIO2	F23
WE	MIO3	C23
R/B	MIO14	B22

Part 2.11: PS Side Gigabit Ethernet Chip

The gigabit Ethernet chip is placed on the core board, and the Ethernet chip and ZYNQ chip are connected through the RGMII interface. The corresponding pins are shown in the following table, and the chip address is PHY_AD[2:0]=001

RMGII Signal	Pin Name	Pin Position
GTX_CLK	MIO16_501	L19
TXD0	MIO17_501	K21
TXD1	MIO18_501	K20
TXD2	MIO19_501	J20
TXD3	MIO20_501	M20
TX_EN	MIO21_501	J19
RX_CLK	MIO22_501	L20
RXD0	MIO23_501	J21
RXD1	MIO24_501	M19
RXD2	MIO25_501	G19
RXD3	MIO26_501	M17
RX_CTL	MIO27_501	G20
PHY_nRST (Power on Reset by Default)	IO_L6P_9	Y20
MDC	MIO52_501	D19
MDIO	MIO53_501	C18

Part 3: Carrier Board Introduction

In this section, will describe in detail all the interface resources on the carrier board.

Part 3.1: AD9361 Introduction

The RF part of the product uses ADI's AD9361, and in this subsection will introduce in details, from the RF link, data channel, and clock part.

Part 3.1.1: RF Front-end Circuits

The RF front-end circuit involves three parts: balun, amplifier, and RF switch. The bandwidth of the balun is 10M-6Ghz, which covers the communication bandwidth of the AD9361.

The bandwidth of the amplifier is 50M-6Ghz, which also covers the communication bandwidth of AD9361, but the gain flatness of the amplifier in the whole communication bandwidth is slightly different. The following table can see the amplifier's indicators for each frequency point in detail.

FREQ	Gain	Isolation	Input Return Loss	Output Return Loss	Stability		IP-3 Output	1dB Comp. Output	Noise Figure
(MHz)	(dB)	(dB)	(dB)	(dB)	K	Measure	(dBm)	(dBm)	(dB)
50.00	17.73	23.19	14.21	18.51	1.14	0.76	31.53	17.82	2.10
80.00	17.14	22.43	16.76	18.87	1.14	0.73	32.21	17.91	1.97
100.00	16.93	22.26	18.14	19.00	1.15	0.72	32.46	17.83	2.00
200.00	16.55	22.00	21.40	19.27	1.18	0.72	32.09	17.88	1.96
400.00	16.32	21.92	22.06	19.17	1.19	0.72	32.80	17.69	2.18
500.00	16.22	21.95	21.60	19.08	1.20	0.73	32.65	17.75	2.22
600.00	16.12	21.91	20.87	18.92	1.21	0.73	32.75	17.73	2.18
800.00	15.90	21.94	19.22	18.59	1.23	0.75	32.97	17.68	2.22
1000.00	15.63	21.95	17.75	18.27	1.24	0.77	32.35	17.74	2.14
1200.00	15.34	21.94	16.45	17.96	1.26	0.79	33.10	17.70	2.27
1400.00	15.03	21.96	15.29	17.73	1.29	0.81	33.34	17.71	2.28
1500.00	14.88	21.96	14.70	17.47	1.29	0.82	32.76	17.78	2.31
1600.00	14.70	21.96	14.37	17.59	1.31	0.83	33.06	17.69	2.35
1800.00	14.38	21.98	13.49	17.43	1.33	0.85	33.66	17.56	2.36
2000.00	14.04	21.97	12.88	17.64	1.36	0.87	33.23	17.81	2.39
2200.00	13.72	21.93	12.29	17.75	1.38	0.89	33.13	17.99	2.45
2400.00	13.42	21.90	11.83	17.77	1.40	0.91	33.38	17.82	2.44
2500.00	13.27	21.94	11.64	17.87	1.41	0.92	33.32	17.96	2.50
2600.00	13.13	21.94	11.46	17.91	1.43	0.93	33.58	17.80	2.61
2800.00	12.85	21.83	11.14	17.97	1.44	0.95	33.46	17.78	2.65
3000.00	12.57	21.81	10.87	17.73	1.46	0.96	33.43	17.84	2.57
3200.00	12.35	21.77	10.64	17.84	1.47	0.97	32.91	17.81	2.70
3400.00	12.09	21.84	10.61	18.20	1.52	0.98	33.34	17.88	2.73
3500.00	12.00	21.75	10.43	17.93	1.51	0.98	33.57	17.63	2.89
3600.00	11.89	21.62	10.24	17.62	1.50	0.99	33.63	17.80	2.78
3800.00	11.68	21.57	10.12	17.40	1.52	0.99	33.53	17.82	2.91
4000.00	11.51	21.44	9.87	17.10	1.51	1.00	33.78	17.77	3.01
4200.00	11.36	21.39	9.75	16.86	1.52	1.00	33.67	17.67	2.96
4400.00	11.24	21.35	9.57	16.39	1.51	1.01	33.48	17.50	3.04
4500.00	11.08	21.33	9.53	16.36	1.54	1.01	33.53	17.62	3.12
4600.00	11.06	21.42	9.49	16.15	1.55	1.01	33.33	17.68	3.19
4800.00	10.90	21.23	9.20	15.40	1.52	1.02	33.45	17.59	3.25
5000.00	10.75	21.21	9.09	15.04	1.53	1.02	33.46	17.18	3.27
5200.00	10.64	21.03	8.71	14.21	1.49	1.02	33.61	17.24	3.34
5400.00	10.55	20.98	8.50	13.69	1.48	1.02	33.92	16.79	3.45
5500.00	10.50	20.92	8.35	13.36	1.47	1.02	33.27	17.75	3.44
5600.00	10.67	21.34	8.50	13.68	1.51	1.03	33.63	17.27	3.51
5700.00	10.57	21.11	8.18	13.01	1.46	1.03	33.71	17.19	3.51
5800.00	10.48	20.92	7.96	12.52	1.43	1.03	33.58	17.27	3.59
5900.00	10.40	20.86	7.76	12.12	1.41	1.03	33.69	17.15	3.70
6000.00	10.37	20.82	7.64	12.03	1.40	1.03	34.30	16.80	3.72
6500.00	10.12	20.52	6.68	10.59	1.30	1.04	33.96	16.82	4.00
7000.00	9.73	20.58	5.74	9.16	1.23	1.05	33.55	16.34	4.12
7500.00	8.78	20.45	5.07	7.72	1.19	1.04	32.63	15.47	4.72
8000.00	7.49	21.63	4.30	6.09	1.27	1.01	30.33	15.48	5.32

The RF switch adopts SPDT one-in-two-out, with a bandwidth of 9K-8G, and the RF switch has an internal integrated electrostatic protection circuit, which effectively protects the RF port. The switching logic of the corresponding RF switch can be referred to the following table, for the TX/RX switching of AD9361, you can refer to the schematic for the actual connection relationship to correspond to the adjustment.

LS	CTRL	RFC-RFC1	RFC-RFC1
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

In addition, for the RF front-end we have involved 4-way LED indication, port setting 1 corresponds to LED on and port setting 0 corresponds to LED off. The following table lists the LED pin correspondences.

LED	Pin Name	Pin Position
LED_RF_TX1	IO_13P_MRCC_12	AE28
LED_RF_RX1	IO_13N_MRCC_12	AF28
LED_RF_TX2	IO_18P_12	AE25
LED_RF_RX2	IO_18N_12	AF25

Part 3.1.2: AD9361 Control and Data Ports

The AD9361 digital port is divided into data port and control port, the data port can be defined as LVCMOS, can also be defined as LVDS, LVCMOS communication rate is not high, so the project provided by Cruetech, default LVDS interface to define the data port, the following table lists the pin correspondence, you can also refer to the schematic.

AD9361 Interface	Pin Name	Pin Position
AD9631_TX_P0	IO_4P_10	AJ16
AD9631_TX_N0	IO_4N_10	AK16
AD9631_TX_P1	IO_15P_10	AF18
AD9631_TX_N1	IO_15N_10	AF17
AD9631_TX_P2	IO_12P_MRCC_10	AF14
AD9631_TX_N2	IO_12N_MRCC_10	AG14
AD9631_TX_P3	IO_2P_10	AH18
AD9631_TX_N3	IO_2N_10	AJ18
AD9631_TX_P4	IO_6P_10	AH17
AD9631_TX_N4	IO_6N_10	AH16
AD9631_TX_P5	IO_5P_10	AJ15
AD9631_TX_N5	IO_5N_10	AK15
AD9631_TX_FRAME_P	IO_8P_10	AH14
AD9631_TX_FRAME_N	IO_8N_10	AH13

AD9631_FB_CLK_P	IO_14P_MRCC_10	AF15
AD9631_FB_CLK_N	IO_14N_MRCC_10	AG15
AD9631_RX_P0	IO_22P_10	AB15
AD9631_RX_N0	IO_22N_10	AB14
AD9631_RX_P1	IO_19P_10	AC14
AD9631_RX_N1	IO_19N_10	AC13
AD9631_RX_P2	IO_16P_10	AE16
AD9631_RX_N2	IO_16N_10	AE15
AD9631_RX_P3	IO_17P_10	AE18
AD9631_RX_N3	IO_17N_10	AE17
AD9631_RX_P4	IO_23P_10	AC17
AD9631_RX_N4	IO_23N_10	AC16
AD9631_RX_P5	IO_3P_10	AJ14
AD9631_RX_N5	IO_3N_10	AJ13
AD9631_RX_FRAME_P	IO_18P_10	AD16
AD9631_RX_FRAME_N	IO_18N_10	AD15
AD9631_DATA_CLK_P	IO_13P_MRCC_10	AG17
AD9631_DATA_CLK_N	IO_13N_MRCC_10	AG16
AD9631_CLK_OUT	IO_13P_MRCC_11	AG21
AD9631_SPI_CLK	IO_16P_11	AK17
AD9631_SPI_nCS	IO_16N_11	AK18
AD9631_SPI_DI	IO_20P_11	W21
AD9631_SPI_DO	IO_20N_11	Y21
AD9631_nRST	IO_10N_11	AE21
AD9631_ENABLE	IO_17P_11	AH19
AD9631_EN_AGC	IO_17N_11	AJ19
AD9631_SYNC_IN	IO_23P_11	AA22
AD9631_TXNRX	IO_23N_11	AA23
AD9631_CTRL_OUT0	IO_11P_MRCC_10	AE13
AD9631_CTRL_OUT1	IO_11N_MRCC_10	AF13
AD9631_CTRL_OUT2	IO_9P_10	AD14
AD9631_CTRL_OUT3	IO_9N_10	AD13
AD9631_CTRL_OUT4	IO_21P_10	AB12
AD9631_CTRL_OUT5	IO_21N_10	AC12
AD9631_CTRL_OUT6	IO_24P_10	AB17
AD9631_CTRL_OUT7	IO_24N_10	AB16
AD9631_CTRL_IN0	IO_7P_10	AE12
AD9631_CTRL_IN1	IO_7N_10	AF12
AD9631_CTRL_IN2	IO_10P_10	AG12
AD9631_CTRL_IN3	IO_10N_10	AH12

Part 3.1.3: AD9361 Clock Circuit

The input clock of AD9361 adopts 40M VCTCXO with an accuracy of up to 0.1ppm. In addition, the board has reserved ADF4002BRUZ chip, so if there is a higher requirement for the clock accuracy, it can be adjusted by inputting it to ADF4002BRUZ through RF header.

For detailed use of the clock you can refer to the schematic.

Part 3.2: GPS Module

The GPS module is integrated on the carrier board, which can implement GPS and BeiDou positioning function. We can provide UART to configure and read the GPS module data, in addition the module provides PPS signal. The following table lists the pin correspondences of the GPS module, details refer to the schematic.

GPS Module	Pin Name	Pin Position
GPS_UART_TXD	IO_20N_12	AK30
GPS_UART_RXD	IO_10P_12	AD25
GPS_nRESET	IO_20P_12	AJ30
GPS_PPS	IO_24N_12	AK26

Part 3.3: SD Card Slot Interface

The SD card holder is placed on the carrier board, which is connected to the BANK501 on the PS side of ZYNQ, because the level of BANK501 is 1.8V, but the data level of SD is 3.3V, We use the TXS02612RTWR for level shifting. The following is the pin assignment and schematic diagram of SD card interface, details refer to the schematic.

SD Card Slot	Pin Name	Pin Position
SD_CLK	MIO40	B20
SD_CMD	MIO41	J18
SD_DATA0	MIO42	D20
SD_DATA1	MIO43	E18
SD_DATA2	MIO44	E20
SD_DATA3	MIO45	H18

Part 3.4: PL Side Gigabit Ethernet

The Gigabit Ethernet chip is placed on the carrier board, and the Ethernet chip is interconnected with the ZYNQ chip through the PL side, connecting the corresponding pins as shown in the following table Chip address PHY_AD[2:0]=010.

RMGII Signal	Pin Name	Pin Position
GPHY1_GTX_CLK	IO_16P_35	D16
GPHY1_TXD0	IO_8P_35	G15
GPHY1_TXD1	IO_15N_35	E17
GPHY1_TXD2	IO_15P_35	F17

GPHY1_TXD3	IO_16N_35	C16
GPHY1_TX_EN	IO_13N_MRCC_35	E15
GPHY1_RX_CLK	IO_13P_MRCC_35	E16
GPHY1_RXD0	IO_18P_35	B17
GPHY1_RXD1	IO_18N_35	A17
GPHY1_RXD2	IO_17P_35	C17
GPHY1_RXD3	IO_17N_35	B16
GPHY1_RX_DV	IO_1N_35	L14
GPHY1_MDC	IO_8N_35	G14
GPHY1_MDIO	IO_1P_35	L15

Part 3.5: USB2.0 Interface

The USB2.0 chip is integrated on the carrier board. The following table lists the correspondence between the USB PHY and the main chip. For detailed information, please refer to the schematic of the carrier board.

USB2.0 Signal	Pin Name	Pin Position
USBPHY_DATA0	MIO32	K17
USBPHY_DATA1	MIO33	G22
USBPHY_DATA2	MIO34	K18
USBPHY_DATA3	MIO35	G21
USBPHY_DATA4	MIO28	L17
USBPHY_DATA5	MIO37	B21
USBPHY_DATA6	MIO38	A20
USBPHY_DATA7	MIO39	F18
USBPHY_STP	MIO30	L18
USBPHY_NXT	MIO31	H21
USBPHY_DIR	MIO29	H22
USBPHY_CLKOUT	MIO36	H17
USBPHY_nRSET	MIO50	A19

Part 3.6: USB3.0 Interface

The USB3.0 chip is integrated on the carrier board, reserved for user use. The pin correspondence of USB3.0 can be referred to the schematic.

Part 3.7: SFP Interface

The carrier board is designed with one way SFP communication interface, the communication rate is up to 10G. The SFP clock can use the 125M integrated on the core board or the 156.25M designed on the base board, and users can choose which clock to use according to their specific needs. Detalis information refer to th carrier board schematic.

SFP Interface	Pin Name	Pin Position
SFP1_TX_P	MGT_111_TX_P3	V2
SFP1_TX_N	MGT_111_TX_N3	V1
SFP1_RX_P	MGT_111_RX_P3	AA4
SFP1_RX_N	MGT_111_RX_N3	AA3
CLK_P_156.25M	MGT_111_CLK0_P	U8
CLK_N_156.25M	MGT_111_CLK0_N	U7