



**DDR4 2133 / 2400 / 2666 / 2933 /3200  
8GB With 1024Mx8 260Pin SO-DIMM**

**NEO FORZA DDR4 8GB-2133 / 2400 / 2666 / 2933 / 3200 SO-DIMM**

**GENERAL DESCRIPTION**

This chapter gives an overview of the 260-pin SO DDR4 Dual-In-Line memory modules product family and describes its main characteristics.

**FEATURES**

1. 260-Pin SO-DIMM (Lead-Free) DDR4 SDRAM Memory Module.
2. Data transfer rates: . PC4-17000 / 19200 / 21300 / 23400 / 25600
3. Power supply: VDD: 1.20V ± 0.06V
4. Module organization: 1024Meg × 64.  
Chip organization: 1024M × 8.
5. Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
6. Low-power auto self refresh (LPASR)
7. Data bus inversion (DBI) for data bus
8. On-die VREFDQ generation and calibration
9. On-board I<sup>2</sup> serial presence-detect (SPD) EEPROM
10. 16 internal banks; 4 groups of 4 banks each
11. Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
12. Selectable BC4 or BL8 on-the-fly (OTF)
13. Fly-by topology
14. Terminated control command and address bus

**Ordering Information for Compliant Products**

| Product Type         | Compliance Code          | Description     | DRAM Organisation | # of SDRAMs |
|----------------------|--------------------------|-----------------|-------------------|-------------|
| MM4S8GE3PG-2133C-A00 | 8GB DDR4-2133 - 15/15/15 | 1 Rank, Non-ECC | 1024Mx8           | 8           |
| MM4S8GE3PG-2400C-A00 | 8GB DDR4-2400 - 17/17/17 | 1 Rank, Non-ECC | 1024Mx8           | 8           |
| MM4S8GE3PG-2666C-A00 | 8GB DDR4-2666 - 19/19/19 | 1 Rank, Non-ECC | 1024Mx8           | 8           |
| MM4S8GE3PG-2933C-A00 | 8GB DDR4-2933 - 21/21/21 | 1 Rank, Non-ECC | 1024Mx8           | 8           |
| MM4S8GE3PG-3200C-A00 | 8GB DDR4-3200 - 22/22/22 | 1 Rank, Non-ECC | 1024Mx8           | 8           |
|                      |                          |                 |                   |             |



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## PIN OUT

| 260-Pin DDR4 SODIMM Front |                 |     |                  |     |                  |     |                    | 260-Pin DDR4 SODIMM Back |                  |     |                    |     |                    |     |                  |
|---------------------------|-----------------|-----|------------------|-----|------------------|-----|--------------------|--------------------------|------------------|-----|--------------------|-----|--------------------|-----|------------------|
| Pin                       | Symbol          | Pin | Symbol           | Pin | Symbol           | Pin | Symbol             | Pin                      | Symbol           | Pin | Symbol             | Pin | Symbol             | Pin | Symbol           |
| 1                         | V <sub>SS</sub> | 67  | DQ29             | 133 | A1               | 199 | DM5_n/<br>DBI5_n   | 2                        | V <sub>SS</sub>  | 68  | V <sub>SS</sub>    | 134 | EVENT_n,<br>NF     | 200 | DQS5_t           |
| 3                         | DQ5             | 69  | V <sub>SS</sub>  | 135 | V <sub>DD</sub>  | 201 | V <sub>SS</sub>    | 4                        | DQ4              | 70  | DQ24               | 136 | V <sub>DD</sub>    | 202 | V <sub>SS</sub>  |
| 5                         | V <sub>SS</sub> | 71  | DQ25             | 137 | CK0_t            | 203 | DQ46               | 6                        | V <sub>SS</sub>  | 72  | V <sub>SS</sub>    | 138 | CK1_t/NF           | 204 | DQ47             |
| 7                         | DQ1             | 73  | V <sub>SS</sub>  | 139 | CK0_c            | 205 | V <sub>SS</sub>    | 8                        | DQ0              | 74  | DQS3_c             | 140 | CK1_c/NF           | 206 | V <sub>SS</sub>  |
| 9                         | V <sub>SS</sub> | 75  | DM3_n/<br>DBI3_n | 141 | V <sub>DD</sub>  | 207 | DQ42               | 10                       | V <sub>SS</sub>  | 76  | DQS3_t             | 142 | V <sub>DD</sub>    | 208 | DQ43             |
| 11                        | DQS0_c          | 77  | V <sub>SS</sub>  | 143 | PARITY           | 209 | V <sub>SS</sub>    | 12                       | DM0_n/<br>DBI0_n | 78  | V <sub>SS</sub>    | 144 | A0                 | 210 | V <sub>SS</sub>  |
| 13                        | DQS0_t          | 79  | DQ30             | 145 | BA1              | 211 | DQ52               | 14                       | V <sub>SS</sub>  | 80  | DQ31               | 146 | A10/AP             | 212 | DQ53             |
| 15                        | V <sub>SS</sub> | 81  | V <sub>SS</sub>  | 147 | V <sub>DD</sub>  | 213 | V <sub>SS</sub>    | 16                       | DQ6              | 82  | V <sub>SS</sub>    | 148 | V <sub>DD</sub>    | 214 | V <sub>SS</sub>  |
| 17                        | DQ7             | 83  | DQ26             | 149 | CS0_n            | 215 | DQ49               | 18                       | V <sub>SS</sub>  | 84  | DQ27               | 150 | BA0                | 216 | DQ48             |
| 19                        | V <sub>SS</sub> | 85  | V <sub>SS</sub>  | 151 | WE_n/<br>A14     | 217 | V <sub>SS</sub>    | 20                       | DQ2              | 86  | V <sub>SS</sub>    | 152 | RAS_n/<br>A16      | 218 | V <sub>SS</sub>  |
| 21                        | DQ3             | 87  | CB5/NC           | 153 | V <sub>DD</sub>  | 219 | DQS6_c             | 22                       | V <sub>SS</sub>  | 88  | CB4/NC             | 154 | V <sub>DD</sub>    | 220 | DM6_n/<br>DBI6_n |
| 23                        | V <sub>SS</sub> | 89  | V <sub>SS</sub>  | 155 | ODT0             | 221 | DQS6_t             | 24                       | DQ12             | 90  | V <sub>SS</sub>    | 156 | CAS_n/<br>A15      | 222 | V <sub>SS</sub>  |
| 25                        | DQ13            | 91  | CB1/NC           | 157 | CS1_n            | 223 | V <sub>SS</sub>    | 26                       | V <sub>SS</sub>  | 92  | CB0/NC             | 158 | A13                | 224 | DQ54             |
| 27                        | V <sub>SS</sub> | 93  | V <sub>SS</sub>  | 159 | V <sub>DD</sub>  | 225 | DQ55               | 28                       | DQ8              | 94  | V <sub>SS</sub>    | 160 | V <sub>DD</sub>    | 226 | V <sub>SS</sub>  |
| 29                        | DQ9             | 95  | DQS8_c           | 161 | ODT1             | 227 | V <sub>SS</sub>    | 30                       | V <sub>SS</sub>  | 96  | DM8_n/<br>DBI_n/NC | 162 | C0/<br>CS2_n/NC    | 228 | DQ50             |
| 31                        | V <sub>SS</sub> | 97  | DQS8_t           | 163 | V <sub>DD</sub>  | 229 | DQ51               | 32                       | DQS1_c           | 98  | V <sub>SS</sub>    | 164 | V <sub>REFCA</sub> | 230 | V <sub>SS</sub>  |
| 33                        | DM1_n/<br>DBI_n | 99  | V <sub>SS</sub>  | 165 | C1, CS3_n,<br>NC | 231 | V <sub>SS</sub>    | 34                       | DQS1_t           | 100 | CB6/NC             | 166 | SA2                | 232 | DQ60             |
| 35                        | V <sub>SS</sub> | 101 | CB2/NC           | 167 | V <sub>SS</sub>  | 233 | DQ61               | 36                       | V <sub>SS</sub>  | 102 | V <sub>SS</sub>    | 168 | V <sub>SS</sub>    | 234 | V <sub>SS</sub>  |
| 37                        | DQ15            | 103 | V <sub>SS</sub>  | 169 | DQ37             | 235 | V <sub>SS</sub>    | 38                       | DQ14             | 104 | CB7/NC             | 170 | DQ36               | 236 | DQ57             |
| 39                        | V <sub>SS</sub> | 105 | CB3/NC           | 171 | V <sub>SS</sub>  | 237 | DQ56               | 40                       | V <sub>SS</sub>  | 106 | V <sub>SS</sub>    | 172 | V <sub>SS</sub>    | 238 | V <sub>SS</sub>  |
| 41                        | DQ10            | 107 | V <sub>SS</sub>  | 173 | DQ33             | 239 | V <sub>SS</sub>    | 42                       | DQ11             | 108 | RESET_n            | 174 | DQ32               | 240 | DQS7_c           |
| 43                        | V <sub>SS</sub> | 109 | CKE0             | 175 | V <sub>SS</sub>  | 241 | DM7_n/<br>DBI7_n   | 44                       | V <sub>SS</sub>  | 110 | CKE1               | 176 | V <sub>SS</sub>    | 242 | DQS7_t           |
| 45                        | DQ21            | 111 | V <sub>DD</sub>  | 177 | DQS4_c           | 243 | V <sub>SS</sub>    | 46                       | DQ20             | 112 | V <sub>DD</sub>    | 178 | DM4_n/<br>DBI4_n   | 244 | V <sub>SS</sub>  |
| 47                        | V <sub>SS</sub> | 113 | BG1              | 179 | DQS4_t           | 245 | DQ62               | 48                       | V <sub>SS</sub>  | 114 | ACT_n              | 180 | V <sub>SS</sub>    | 246 | DQ63             |
| 49                        | DQ17            | 115 | BG0              | 181 | V <sub>SS</sub>  | 247 | V <sub>SS</sub>    | 50                       | DQ16             | 116 | ALERT_n            | 182 | DQ39               | 248 | V <sub>SS</sub>  |
| 51                        | V <sub>SS</sub> | 117 | V <sub>DD</sub>  | 183 | DQ38             | 249 | DQ58               | 52                       | V <sub>SS</sub>  | 118 | V <sub>DD</sub>    | 184 | V <sub>SS</sub>    | 250 | DQ59             |
| 53                        | DQS2_c          | 119 | A12              | 185 | V <sub>SS</sub>  | 251 | V <sub>SS</sub>    | 54                       | DM2_n/<br>DBI2_n | 120 | A11                | 186 | DQ35               | 252 | V <sub>SS</sub>  |
| 55                        | DQS2_t          | 121 | A9               | 187 | DQ34             | 253 | SCL                | 56                       | V <sub>SS</sub>  | 122 | A7                 | 188 | V <sub>SS</sub>    | 254 | SDA              |
| 57                        | V <sub>SS</sub> | 123 | V <sub>DD</sub>  | 189 | V <sub>SS</sub>  | 255 | V <sub>DDSPD</sub> | 58                       | DQ22             | 124 | V <sub>DD</sub>    | 190 | DQ45               | 256 | SA0              |
| 59                        | DQ23            | 125 | A8               | 191 | DQ44             | 257 | V <sub>PP</sub>    | 60                       | V <sub>SS</sub>  | 126 | A5                 | 192 | V <sub>SS</sub>    | 258 | V <sub>TT</sub>  |
| 61                        | V <sub>SS</sub> | 127 | A6               | 193 | V <sub>SS</sub>  | 259 | V <sub>PP</sub>    | 62                       | DQ18             | 128 | A4                 | 194 | DQ41               | 260 | SA1              |
| 63                        | DQ19            | 129 | V <sub>DD</sub>  | 195 | DQ40             | -   | -                  | 64                       | V <sub>SS</sub>  | 130 | V <sub>DD</sub>    | 196 | V <sub>SS</sub>    | -   | -                |
| 65                        | V <sub>SS</sub> | 131 | A3               | 197 | V <sub>SS</sub>  | -   | -                  | 66                       | DQ28             | 132 | A2                 | 198 | DQS5_c             | -   | -                |



## DDR4 2133 / 2400 / 2666 / 2933 /3200 8GB With 1024Mx8 260Pin SO-DIMM

### Pin Descriptions

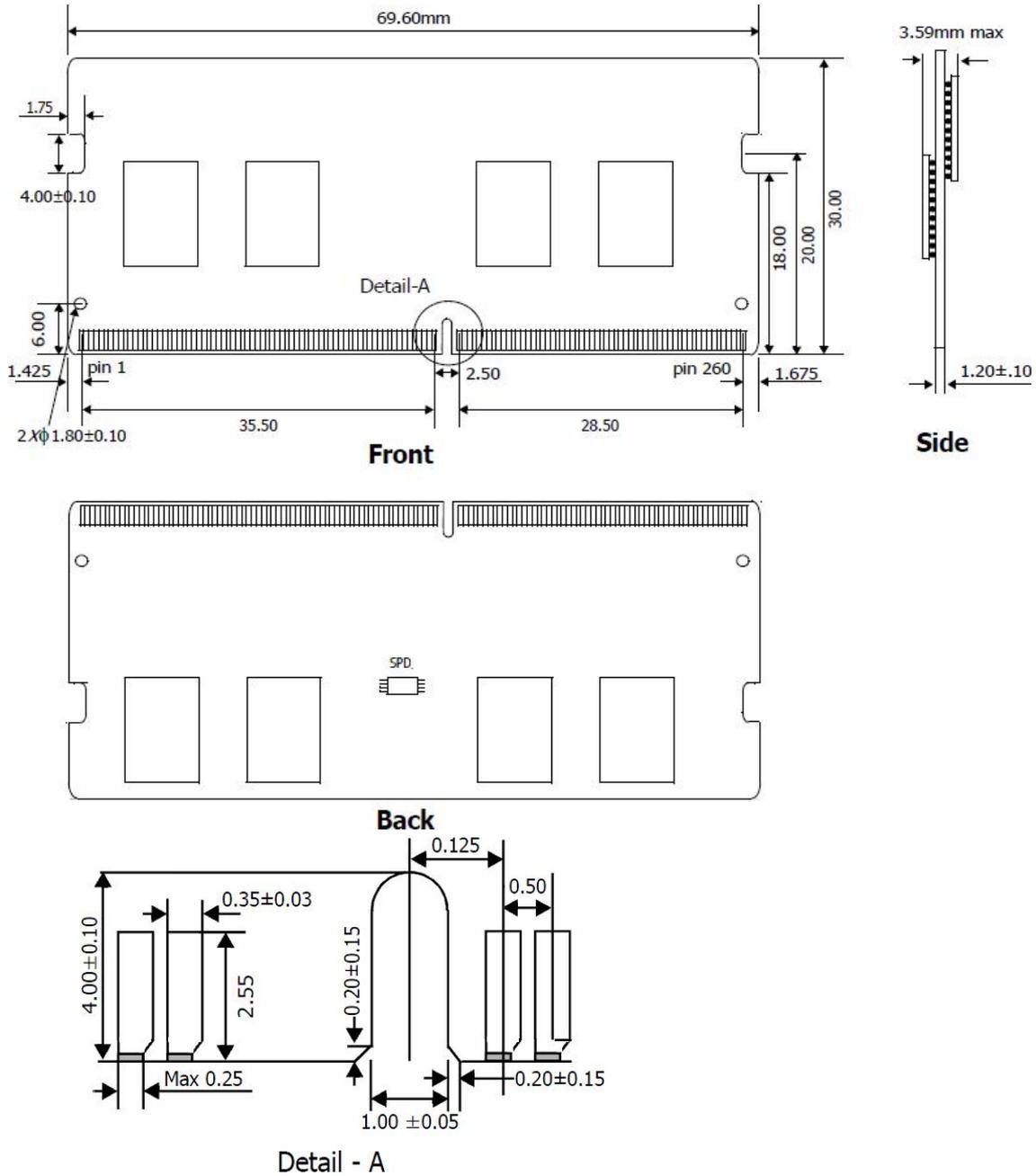
| Pin Name   | Description  | Pin Name           | Description   |
|--|--|--------------------|---|
| A0-A17 <sup>1</sup>  | SDRAM address bus  | SCL                | I <sup>2</sup> C serial bus clock for SPD-TSE         |
| BA0, BA1   | SDRAM bank select  | SDA                | I <sup>2</sup> C serial bus line for SPD-TSE          |
| BG0, BG1   | SDRAM bank group select  | SA0-SA2            | I <sup>2</sup> C slave address select for SPD-TSE     |
| RAS <sub>n</sub> <sup>2</sup>  | SDRAM row address strobe   | PARITY             | SDRAM parity input                                    |
| CAS <sub>n</sub> <sup>3</sup>  | SDRAM column address strobe  | VDD                | SDRAM I/O and core power supply                       |
| WE <sub>n</sub> <sup>4</sup>   | SDRAM write enable   | C0, C1, C2         | Chip ID lines   |
| CS0 <sub>n</sub> , CS1 <sub>n</sub> ,  | DIMM Rank Select Lines   | 12V                | Optional power Supply on socket but not used on UDIMM |
| CKE0, CEK1   | SDRAM clock enable lines input   | VREFCA             | SDRAM command/address reference supply                |
| ODT0, ODT1   | SDRAM on-die termination control lines input   | VSS                | Power supply return (ground)                          |
| ACT <sub>n</sub>   | SDRAM activate   | VDDSPD             | Serial SPD-TSE positive power supply                  |
| DQ0-DQ63   | DIMM memory data bus   | ALERT <sub>n</sub> | SDRAM ALERT <sub>n</sub> output                       |
| CB0-CB7  | DIMM ECC check bits  | VPP                | SDRAM Supply  |
| TDQS0 <sub>t</sub> -<br>TDQS8 <sub>t</sub><br>TDQS0 <sub>c</sub> -<br>TDQS8 <sub>c</sub> | Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs. |                    |   |
| DQS0 <sub>t</sub> -<br>DQS8 <sub>t</sub>   | SDRAM data strobes (positive line of differential pair)                                |                    |   |
| DQS0 <sub>c</sub> -<br>DQS8 <sub>c</sub>   | SDRAM data strobes (negative line of differential pair)                                | RESET <sub>n</sub> | Set DRAMs to a Known State                            |
| DM0 <sub>n</sub> -<br>DM8 <sub>n</sub> ,<br>DBI0 <sub>n</sub> -<br>DBI8 <sub>n</sub>     | SDRAM data masks/data bus inersion (x8-based x72 DIMMs)                                | EVENT <sub>n</sub> | SPD signals a thermal event has occurred              |
| CK0 <sub>t</sub> , CK1 <sub>t</sub>  | SDRAM clock (positive line of differential pair)                                       | VTT                | SDRAM I/O termination supply                          |
| CK0 <sub>c</sub> , CK1 <sub>c</sub>  | SDRAM clock (negative line of differential pair)                                       | RFU                | Reserved for future use                               |

- Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs, this connection pin is NC.
- RAS<sub>n</sub> is a multiplexed function with A16.
- CAS<sub>n</sub> is a multiplexed function with A15.
- WE<sub>n</sub> is a multiplexed function with A14.



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**PACKAGE DIMENSION**



**Note:**

- ◆ Tolerances on all dimensions  $\pm 0.15$  unless otherwise specified.
- ◆ The dimensional diagram is for reference only.

**Units : Millimeters**