CRUETECH

SDR series of boards

CR-P079D Hardware Description

Document Revision History:

time	Version	illustrate
2025.1.25	V1.0	Initial release

This tutorial will be continuously revised, optimized and supplemented based on actual development experience, providing you with more and better routines to help you become industry experts and do your best.

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Chapter 1 : Product Overview

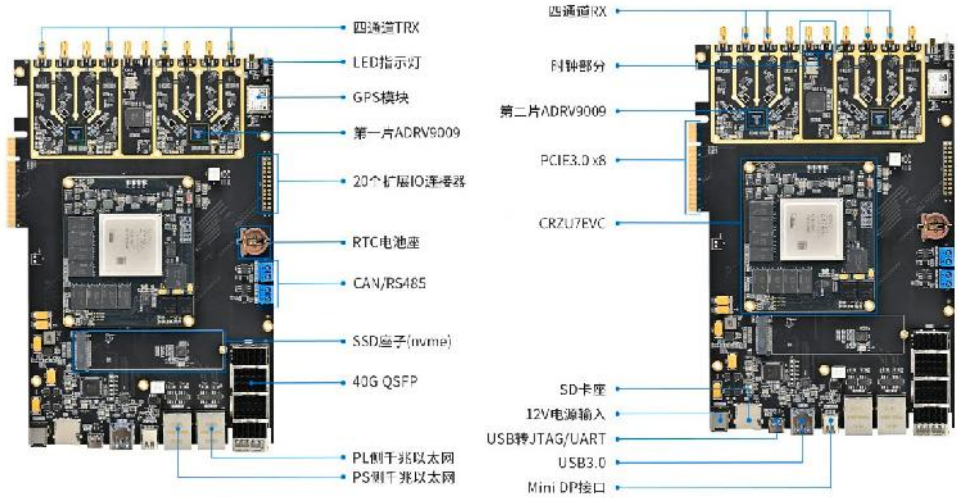
1.1 Product Overview

software-defined radios includes many product categories. This article introduces the CR-P079D product designed for Cruetech. This product uses the XCZU7EV-2FFVC1156I of Xilinx as the main controller and is equipped with the ADRV9009BBCZ RF chip of ADI to form the main structure of the product. The CR-P079D integrates multiple RF and other hardware interfaces, is rich in resources, and is easy to use.

At the same time, CR-P079D integrates two ADRV9009BBCZ chips, realizing the function of multi-chip synchronization. The following figure provides an overview of the product's internal resource structure.

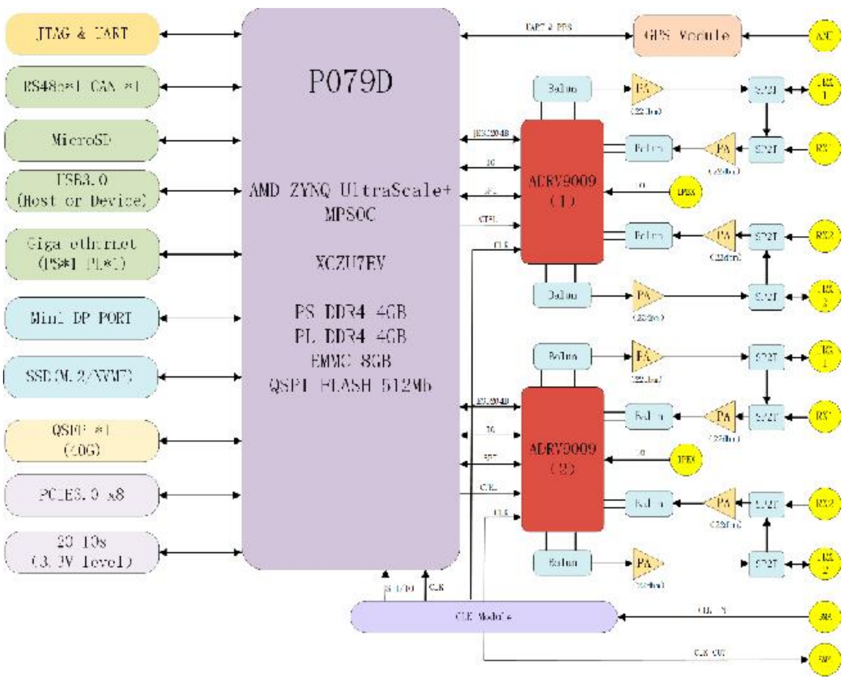
The PCB size of CR-P079D is length*width=220*143mm. Multiple fixing holes are reserved on the PCB to facilitate users to directly integrate it into the device. In addition, we have equipped the product with a beautiful shell, which plays a role in heat dissipation and ensures the stable operation of the product.

The product is designed according to industrial standards, with an operating temperature of -40 to 85° C, uses a high-precision clock, and all interfaces are protected against static electricity.



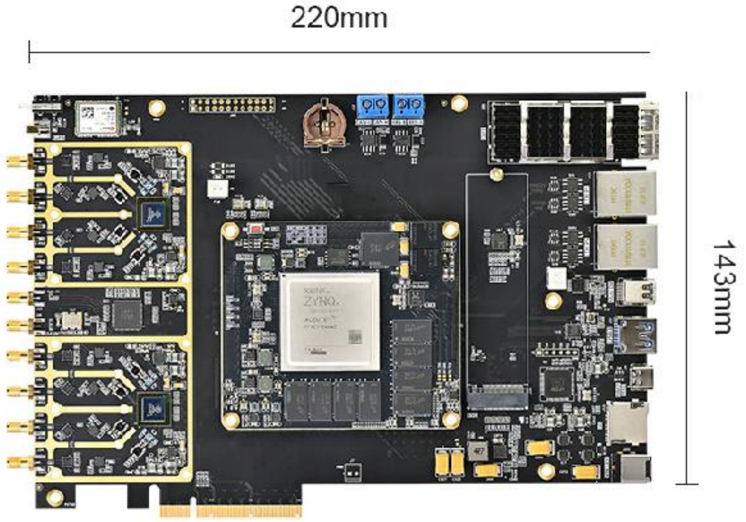
1.2 Product resources and block diagram

The following block diagram lists the product onboard resources, and the following table shows all the functions included in the development board.



1.3 Product size and housing

The following figures show the product PCBA dimensions.



Chapter 2: Hardware Instructions

At the beginning of this chapter, we will systematically introduce the various hardware functions of CR-P079D so that users can quickly get started.

2.1 Overview of CR-P079D Framework

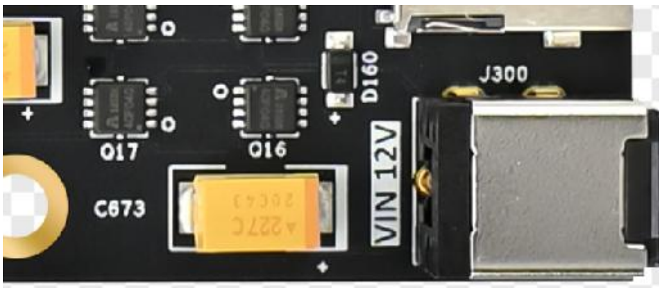
The following table lists the parameters of CR-P079D and the external resources of the board design. The board uses two ADRV9009BBCZ chips to design 4T4R RF channels and multiple high-speed data transmission interfaces, completing the transceiver function of the entire RF link. For more detailed information, please refer to the drawings provided by our company.

主要参数

开发板	P079D
射频芯片	ADRV9009BBCZ
覆盖频率	75MHz-6GHz
位宽	ADC 16bit，DAC 14bit
信号宽带	发送高达450MHz，接收高达200MHz
功率放大	TX和RX均支持全带宽高线性22dbm (最大发射成功率25dbm)
主控制器	XCZU7EV-2FFVC1156I
处理器	ARM：4 x Cortex-A53 (1.3Ghz) RPU：2 x Cortex-R5 (533Mhz) CPU：Mali-400MP2 (667Mhz)
DDR4/DDR4L	PS侧4GB、PL侧4GB
QSPI FLASH	256Mb+256Mb，双FLASH启动，启动更快
EMMC	8GB，存储启动文件和用户文件
射频时钟	1路输入/1路输出
时钟输入	1路
千兆以太网	PS侧1路、PL侧1路
USB3.0/USB2.0 OTG	1路
UART	1路
JTAG	1路
SD卡	1路
GPS	1路
供电/电流	12/3V
温度等级	工业级 (-40°C~+85°C)
尺寸	220x143mm

2.2 About power supply

CR-P079D uses a DC-007B power interface or PCIE interface to provide 12V/3A power supply for the entire board. After the 12V power supply is connected, it is subdivided into other DCDC channels to power other peripherals.



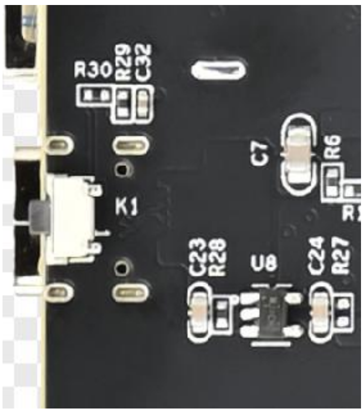
2.3 Clock part

Multiple clocks are designed on the CR-P079D board to meet different functions. For more detailed information, please refer to the drawings provided by our company. It should be noted that the 33.33M and 200M clocks are on the core board, and the other clocks are on the baseboard.

1) A 33.33Mhz clock input is designed for the PS side, and the input pin location is PS_REF_CLK,
   This clock provides the clock source for the ARM side and its pin location is R24.
2) Provides 200M clock for the PL side, the input pin location is IO_L13P_GC_66/IO_L13N_GC_66, this clock provides the clock source for the PL side, the pin location is AH12/AJ12.
3) Two clocks are provided for MGT, 125Mhz and 156.25Mhz respectively. The corresponding relationship of the clock input pins is that 125Mhz is connected to MGT_REF_CLK_P0_227/ MGT_REF_CLK_N0_227, and the pin position is T8/T7; 156.25Mhz is connected to MGT_REF_CLK_P1_227/ MGT_REF_CLK_N1_227, and the pin position is R10/R9;
4) The GTR part provides 26Mhz/27Mhz/100hz, which are used for the three peripheral interfaces of USB3.0/ MiniDP /SSD respectively.
5) A dedicated clock chip HMC7044LP10BE is provided for the RF circuit, which outputs multiple clocks and provides them to the JESD204B interface. For the clock corresponding interface, please refer to our drawings.

2.5 Reset button

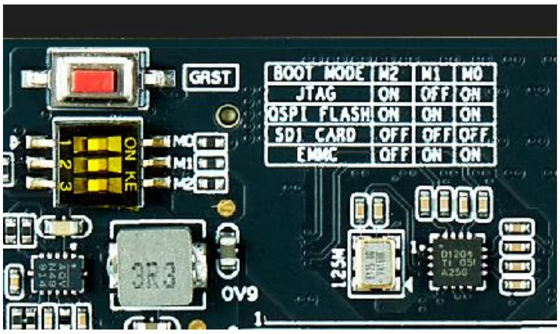
The CR-P079D board provides a nGST reset button near the edge of the board, which is a system reset button and is valid at low level. This pin is connected to the PS_POR_ B (M24) on the PS side and the IO_T1U_67/68(E13) pin on the PL side.



2.5 Master Startup Mode

CR-P079D supports four boot modes, namely JTAG, QSPI Flash, EMMC, and SD card. The DIP switch is located on the core board. The core board has the first three boot modes onboard, and the SD card mode can be achieved by connecting it on the bottom board. The four boot modes can be selected through the onboard DIP switch. The following figure lists the locations of the DIP switches for each mode.

BOOT MODE	M2	M1	M0
JTAG	ON	OFF	ON
QSPI FLASH	ON	ON	ON
SD1 CARD	OFF	OFF	OFF
EMMC	OFF	ON	ON



2.6 Introduction to DDR4

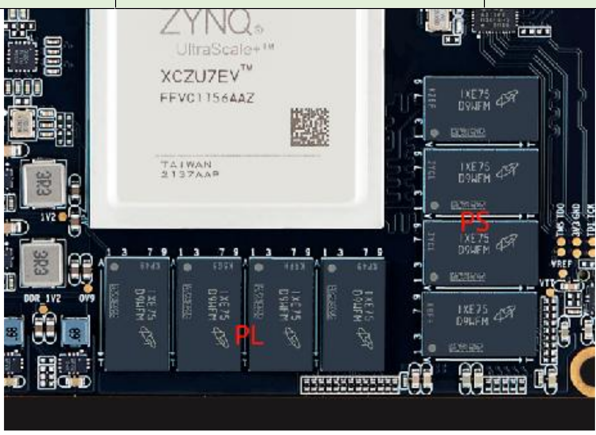
The PS side is designed with four industrial-grade DDR4 chips, each with a capacity of 1GB, and a total capacity of 4GB. Four industrial-grade DDR4 chips are also designed on the side, with a single chip capacity of 1GB and a total capacity of 4GB. The model is MT40A512M16LY-062E IT:E. The DDR4 pin allocation on the PS side can be directly called by the system allocation. The DDR4 pin allocation on the PL side can refer to the table below or the routine provided by our company.

DDR4 pin	Pin Name	Pin Location
DDR4_D0	IO-L2P-64	AN13
DDR4_D1	IO-L6P-64	AN17
DDR4_D2	IO-L5N-64	AP15
DDR4_D3	IO-L5P-64	AP16
DDR4_D4	IO-L2N-64	AP13
DDR4_D5	IO-L3N-64	AN18
DDR4_D6	IO-L6N-64	AN16

DDR4_D7	IO-L3P-64	AM18
DDR4_DM0	IO-L1P-64	AP18
DDR4_DQS_P0	IO-L4P-64	AM14
DDR4_DQS_N0	IO-L4N-64	AN14
DDR4_D8	IO-L8N-64	AL15
DDR4_D9	IO-L11N-64	AK17
DDR4_D10	IO-L8P-64	AL16
DDR4_D11	IO-L9P-64	AK18
DDR4_D12	IO-L12N-64	AJ15
DDR4_D13	IO-L12P-64	AJ16
DDR4_D14	IO-L9N-64	AL18
DDR4_D15	IO-L11P-64	AJ17
DDR4_DM1	IO-L7P-64	AM16
DDR4_DQS_P1	IO-L10P-64	AK15
DDR4_DQS_N1	IO-L10N-64	AK14
DDR4_D16	IO-L18P-64	AG15
DDR4_D17	IO-L14P-64	AF18
DDR4_D18	IO-L17P-64	AF16
DDR4_D19	IO-L15N-64	AF17
DDR4_D20	IO-L17N-64	AF15
DDR4_D21	IO-L14N-64	AG18
DDR4_D22	IO-L18N-64	AG14
DDR4_D23	IO-L15P-64	AE17
DDR4_DM2	IO-L13P-64	AH18
DDR4_DQS_P2	IO-L16P-64	AH14
DDR4_DQS_N2	IO-L16N-64	AJ14
DDR4_D24	IO-L23N-64	AB14
DDR4_D25	IO-L24N-64	AD16
DDR4_D26	IO-L21N-64	AB15
DDR4_D27	IO-L24P-64	AD17
DDR4_D28	IO-L23P-64	AA14
DDR4_D29	IO-L20P-64	AC17
DDR4_D30	IO-L21P-64	AB16
DDR4_D31	IO-L20N-64	AC16
DDR4_DM3	IO-L19P-64	AD15
DDR4_DQS_P3	IO-L22P-64	AA16
DDR4_DQS_N3	IO-L22N-64	AA15
DDR4_D32	IO-L3P-65	AP21
DDR4_D33	IO-L5P-65	AN22
DDR4_D34	IO-L3N-65	AP22
DDR4_D35	IO-L5N-65	AP23
DDR4_D36	IO-L2N-65	AN19
DDR4_D37	IO-L6P-65	AM23

DDR4_D38	IO-L2P-65	AM19
DDR4_D39	IO-L6N-65	AN23
DDR4_DM4	IO-L1P-65	AP19
DDR4_DQS_P4	IO-L4P-65	AM21
DDR4_DQS_N4	IO-L4N-65	AN21
DDR4_D40	IO-L9P-65	AJ19
DDR4_D41	IO-L11P-65	AJ20
DDR4_D42	IO-L11N-65	AK20
DDR4_D43	IO-L8N-65	AL23
DDR4_D44	IO-L9N-65	AK19
DDR4_D45	IO-L12N-65	AJ22
DDR4_D46	IO-L8P-65	AL22
DDR4_D47	IO-L12P-65	AJ21
DDR4_DM5	IO-L7P-65	AL20
DDR4_DQS_P5	IO-L10P-65	AK22
DDR4_DQS_N5	IO-L10P-65	AK23
DDR4_D48	IO-L15N-65	AG20
DDR4_D49	IO-L17N-65	AF22
DDR4_D50	IO-L14N-65	AH21
DDR4_D51	IO-L14P-65	AG21
DDR4_D52	IO-L15P-65	AG19
DDR4_D53	IO-L18P-65	AE23
DDR4_D54	IO-L17P-65	AF21
DDR4_D55	IO-L18N-65	AE24
DDR4_DM6	IO-L13P-65	AH22
DDR4_DQS_P6	IO-L16P-65	AF23
DDR4_DQS_N6	IO-L16N-65	AG23
DDR4_D56	IO-L21P-65	AD20
DDR4_D57	IO-L20P-65	AB19
DDR4_D58	IO-L21N-65	AE20
DDR4_D59	IO-L20N-65	AC19
DDR4_D60	IO-L23P-65	AC18
DDR4_D61	IO-L24N-65	AA20
DDR4_D62	IO-L23N-65	AD19
DDR4_D63	IO-L24P-65	AA19
DDR4_DM7	IO-L19P-65	AE18
DDR4_DQS_P7	IO-L22P-65	AA18
DDR4_DQS_N7	IO-L22N-65	AB18
DDR4_A0	IO-L17P-66	AG11
DDR4_A1	IO-L21N-66	AF13
DDR4_A2	IO-L11P-66	AJ10
DDR4_A3	IO-L20N-66	AE14
DDR4_A4	IO-L18N-66	AG8

DDR4_A5	IO-L21P-66	AE13
DDR4_A6	IO-L18P-66	AF8
DDR4_A7	IO-L15P-66	AG13
DDR4_A8	IO-L10N-66	L8
DDR4_A9	IO-L15N-66	AH13
DDR4_A10	IO-L17N-66	AG10
DDR4_A11	IO-L10P-66	AK8
DDR4_A12	IO-L16N-66	H9
DDR4_A13	IO-L11N-66	AK10
DDR4_A14	IO-L22N-66	AD12
DDR4_A15	IO-L16P-66	G9
DDR4_A16	IO-L12P-66	AJ9
DDR4_A17	IO-L12N-66	AK9
DDR4_BA0	IO-L23N-66	AF12
DDR4_BA1	IO-L9N-66	AL12
DDR4_BG0	IO-L23P-66	AE12
DDR4_nCS	IO-L8N-66	AL10
DDR4_nACT	IO-L22P-66	AC12
DDR4_ODT	IO-L20P-66	AD14
DDR4_RESET	IO-L19N-66	AF10
DDR4_CLK_P	IO-L14P-66	AH11
DDR4_CLK_N	IO-L14N-66	AJ11
DDR4_CKE	IO-L8P-66	AL11
DDR4_TEN	IO-L9P-66	AK12
DDR4_PARITY	IO-L19P-66	AF11
DDR4_nALERT	IO-L7N-66	AL13

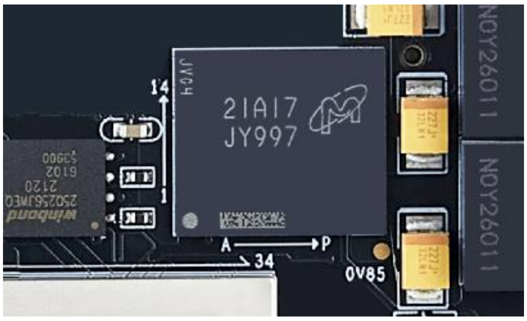


2.7 EMMC Introduction

The CR-P079D is designed with an 8GB EMMC that users can use to store startup files and user files.

The pin definitions are shown in the following table.

EMMC pin	Pin Name	Pin Location
EMMC_D0	MIO13	D27
EMMC_D1	MIO14	A27
EMMC_D2	MIO15	E27
EMMC_D3	MIO16	A28
EMMC_D4	MIO17	C29
EMMC_D5	MIO18	F27
EMMC_D6	MIO19	B28
EMMC_D7	MIO20	E29
EMMC_CLK	MIO22	F28
EMMC_CMD	MIO21	C28
EMMCn_RST	MIO23	B29

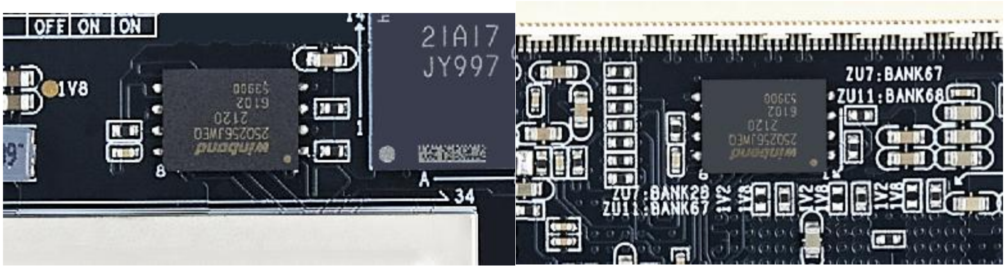


2.8 QSPI FLASH Introduction

CR-P079D is designed with two 256Mb QSPI FLASH, totaling 512Mb, forming x8 mode. It can be used to store startup files and user files. The pin definitions are shown in the following table.

QSPI0 FLASH	Pin Name	Pin Location
QSPI0_DQ0	MIO2	A25
QSPI0_DQ1	MIO3	C24
QSPI0_DQ2	MIO4	B24
QSPI0_DQ3	MIO5	E25
QSPI0_CS	MIO1	D25
QSPI0_CLK	MIO6	A24

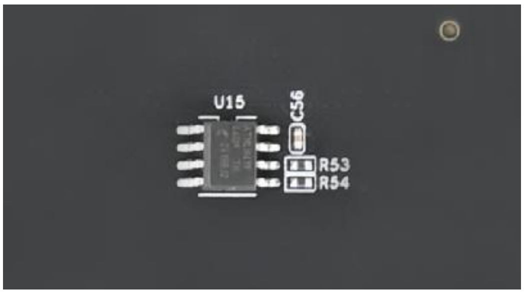
QSPI1 FLASH	Pin Name	Pin Location
QSPI1_DQ0	MIO2	D26
QSPI1_DQ1	MIO3	C26
QSPI1_DQ2	MIO4	F26
QSPI1_DQ3	MIO5	B26
QSPI1_CS	MIO1	B25
QSPI1_CLK	MIO6	C27



2.9 E2PROM Introduction

An E2PROM with a capacity of 256Kb is reserved on the board. The pin definitions are shown in the following table.

E2PROM Pinout	Pin Name	Pin Location
E2PROM_I2C_SCL	IO_L1N_87/88	N12
E2PROM_I2C_SDA	IO_L7P_87/88	L8

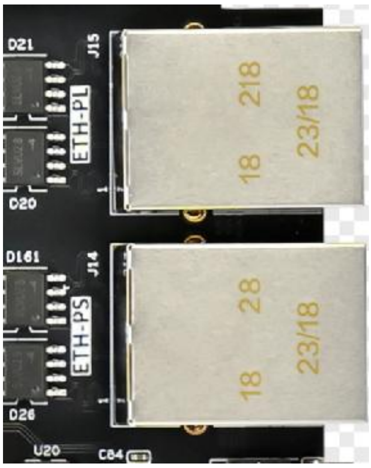


2. 10 Gigabit Ethernet

CR-P079D is designed with two Gigabit Ethernets, one on the PS side and the other on the PL side. The corresponding address on the PS side is PHY_AD[2:0]=001 , and the corresponding address on the PL side is PHY_AD[2:0]=0 10. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface. The corresponding pins are shown in the table below.

GPHY0 Signal	Pin Name	Pin Location
GPHY0_G TX_CLK	MIO26_501	A29
GPHY0_TXD0	MIO27_501	A30
GPHY0_TXD1	MIO28_501	A31
GPHY0_TXD2	MIO29_501	A32
GPHY0_TXD3	MIO30_501	A33
GPHY0_T X_EN	MIO31_501	B30
GPHY0_R X_CLK	MIO32_501	B31
GPHY0_RXD0	MIO33_501	B33
GPHY0_R XD1	MIO34_501	B34
GPHY0_RXD2	MIO35_501	C31
GPHY0_RXD3	MIO36_501	C32

GPHY0_RX_DV	MIO37_501	C33
GPHY0_MDC	MIO76_502	L33
GPHY0_MDIO	MIO77_502	L34
GPHY1 Signal	Pin Name	Pin Location
GPHY1_GTX_CLK	IO_L18P_28/67	G25
GPHY1_TXD0	IO_L4N_28/67	K23
GPHY1_TXD1	IO_L4P_28/67	K22
GPHY1_TXD2	IO_L1N_28/67	L22
GPHY1_TXD3	IO_L1P_28/67	L21
GPHY1_TX_EN	IO_L14P_28/67	G23
GPHY1_RX_CLK	IO_L13P_28/67	F23
GPHY1_RXD0	IO_L17P_28/67	D22
GPHY1_RXD1	IO_L17N_28/67	C23
GPHY1_RXD2	IO_L3P_28/67	J21
GPHY1_RXD3	IO_L3N_28/67	J22
GPHY1_RX_DV	IO_L13N_28/67	E23
GPHY1_MDC	IO_L15P_28/67	C21
GPHY1_MDIO	IO_L15N_28/67	C22



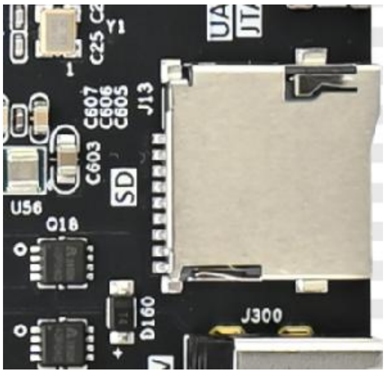
2.11 SD Card

An SD card holder is designed on the board and connected to BANK501 on the PS side. Because the level of BANK501 is 1.8V, but the data level of SD is 3.3V, TXS02612RTWR is used for level conversion.

The following is the pin assignment of the SD card. For more detailed circuit, please refer to the schematic diagram.

SD Card	Pin Name	Pin Location
SD_CLK	MIO51	F34
SD_CMD	MIO50	F33
SD-CD	MIO45	E33
SD_DATA0	MIO46	E34
SD_DATA1	MIO47	F30
SD_DATA2	MIO48	F31

SD_DATA3	MIO49	F32

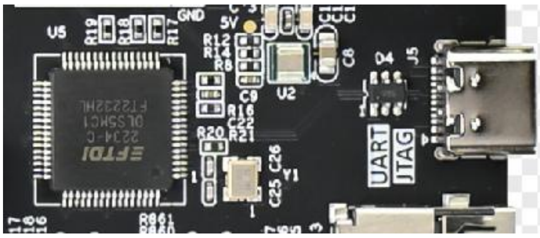


2.12 USB to JTAG and UART

CR-P079D is designed with a USB to JTAG/UART interface. The JTAG is connected to the JTAG interface of the main control chip, and the UART is connected to the UART0 pin of the main control.

The following is the pin assignment of UART0. For more detailed circuit, please refer to the schematic diagram.

UART0	Pin Name	Pin Location
UART0_TX	MIO43	E30
UART0_RX	MIO42	D34



2.13 RS485 interface

CR-P079D uses SP3485EN chip to realize RS485 communication. The TX/RX signal of RS485 is connected to BANK501 of MPSOC. The interface level is 1.8V, so the interface is converted to 3.3V and connected to RS485 chip.

The following is the signal correspondence table and schematic diagram. The TX /RX direction is defined at the MPSOC end.

RS485 Pinout	Pin Name	Pin Location
RS485_TX	MIO40	D31
RS485_RX	MIO41	D32

2.14 CAN interface

CR-P079D uses SN65HVD230D chip to realize CAN communication. CAN's TX/RX signal is connected to MPSOC 's B ANK501. The interface level is 1.8V, so the signal interface is converted to 3.3V and connected to the CAN chip.

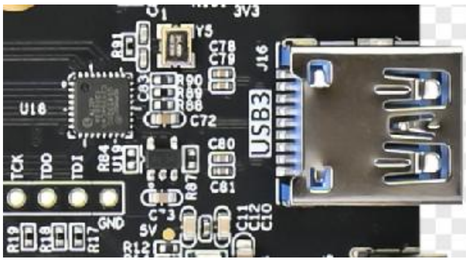
The following is a signal correspondence table. The TX/RX direction is defined by the MPSOC end. For detailed circuits, refer to the development board schematic diagram.

CAN pin	Pin Name	Pin Location
CAN0_TX	MIO39	D30
CAN0_RX	MIO38	C34

2.15 USB 3.0 interface

CR-P079D is designed with a USB3.0 interface, the interface type is Type-A, which can be flexibly defined as Host mode or Device mode. The following table lists the correspondence between USB PHY and the main chip. For more information, see the baseboard schematic diagram.

USB Signal	Pin Name	Pin Location
USBPHY_DATA0	MIO56	G34
USBPHY_DATA1	MIO57	H29
USBPHY_DATA2	MIO54	G31
USBPHY_DATA3	MIO59	H32
USBPHY_DATA4	MIO60	H33
USBPHY_DATA5	MIO61	H34
USBPHY_DATA6	MIO62	J29
USBPHY_DATA7	MIO63	J30
USBPHY_STP	MIO58	H31
USBPHY_NXT	MIO55	G33
USBPHY_DIR	MIO53	G30
USBPHY_CLKOUT	MIO52	G29
USB_nRSET	MIO 64	E32
GT2_USB3_SSTXP	PS_MGTRTXP2_505	P31
GT2_USB3_SSTXN	PS_MGTRTXN2_505	P32
GT2_USB3_SSRXP	PS_MGTRRXP2_505	R33
GT2_USB3_SSRXN	PS_MGTRRXN2_505	R34
CLK_FPGA_26M_P	MGT_505_TX_P 2	M27
CLK_FPGA_26M_N	MGT_505_TX_N 2	M28

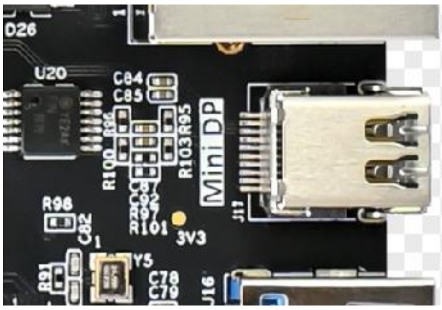


2.16 Mini DP port

Mini DP output interface is designed on CR-P079D, and the interface signal is connected to FPGA 's BANK50/BANK505. For details, please refer to the schematic diagram.

The following is the pin assignment of Mini DP. For detailed circuit, please refer to the development board schematic diagram.

MiniDP Pinout	Pin Name	Pin Location
GT3_ DP_LINE_P0	MGT_505_TX_P3	N29
GT3_ DP_LINE_N0	MGT_505_TX_N3	N30
DP_HPD	IO_L11N_87/88	G7
DP_AUX_OUT	IO_L12N_87/88	G8
DP_OE	IO_L12P_87/88	H8
DP_AUX_IN	IO_L11P_87/88	H7
DP_CLK_P_27M	MGT_505_CLK_P2	M31
DP_CLK_N_27M	MGT_505_CLK_N2	M32



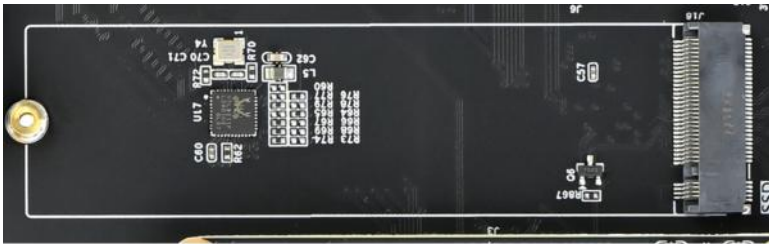
2.17 SSD interface

The CR-P079D's PS side is designed with an SSD (x2 mode), the interface type is M.2, and it uses the NVME protocol.

the SSD interface are shown in the following table. For detailed circuits, please refer to the development board schematic diagram.

SSD interface	Pin Name	Pin Location
SSD_nRST	MIO 642	J31

CLK_FPGA_100M_P	MGT_505_CLK_P0	T27
CLK_FPGA_100M_N	MGT_505_CLK_N0	T28
GT0_SSD_TX_P0	MGT_505_TX_P0	U29
GT0_SSD_TX_N0	MGT_505_TX_N0	U30
GT0_SSD_RX_P0	MGT_505_RX_P0	U33
GT0_SSD_RX_N0	MGT_505_RX_N0	U34
GT0_SSD_TX_P 1	MGT_505_TX_P 1	R29
GT0_SSD_TX_N 1	MGT_505_TX_N 1	R30
GT0_SSD_RX_P 1	MGT_505_RX_P 1	T31
GT0_SSD_RX_N 1	MGT_505_RX_N 1	T32

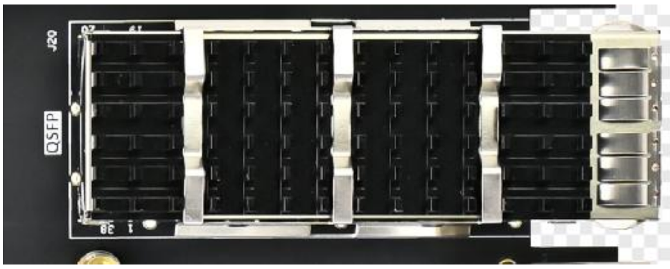


2.18 QSFP interface

SFP interface is designed on CR-P079D, and the interface signal is connected to BANK227 of MPSOC. For details, please refer to the schematic diagram.

The following is the pin assignment of Q SFP . For detailed circuit, please refer to the development board schematic diagram.

Q SFP Pinout	Pin Name	Pin Location
QSFP-TX-P0	MGT_TX_P3_227	H4
QSFP-TX-N0	MGT_TX_N3_227	H3
QSFP-TX-P1	MGT_TX_P2_227	K4
QSFP-TX-N1	MGT_TX_N2_227	K3
QSFP-TX-P2	MGT_TX_P1_227	L6
QSFP-TX-N2	MGT_TX_N1_227	L5
QSFP-TX-P3	MGT_TX_P0_227	M4
QSFP-TX-N3	MGT_TX_N0_227	M3
QSFP-RX-P0	MGT_RX_P3_227	G2
QSFP-RX-N0	MGT_RX_N3_227	G1
QSFP-RX-P1	MGT_RX_P2_227	J2
QSFP-RX-N1	MGT_RX_N2_227	J1
QSFP-RX-P2	MGT_RX_P1_227	L2
QSFP-RX-N2	MGT_RX_N1_227	L1
QSFP-RX-P3	MGT_RX_P0_227	N2
QSFP-RX-N3	MGT_RX_N0_227	N1
QSFP_LPMODE	IO_1P_94	M11
QSFP_I2C_SCL	IO_2P_94	K9
QSFP_I2C_SDA	IO_2N_94	J9



2.19 PCIE3.0 x8 interface

CR-P079D is designed with PCIE 3.0, which is a x8 interface. The following table lists the PCIE interface correspondence.

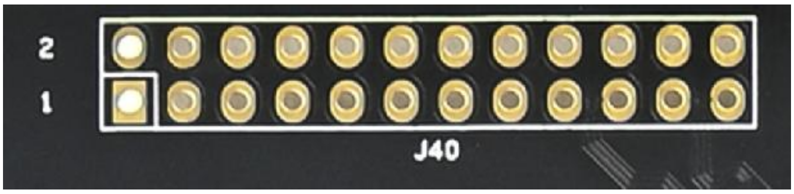
PCIE3.0	Pin Name	Pin Location
PERST_N	IO_ 4P _ 87_88	N11
REF_CLK_P	MGT_CLK_P0 _223	AD8
REF_CLK_N	MGT_CLK_ N 0 _223	AD7
PER0_P	MGT_TX_P3_224	AD4
PER0_N	MGT_TX_N3_224	AD3
PER1_P	MGT_TX_P2_224	AE6
PER1_N	MGT_TX_N2_224	AE5
PER2_P	MGT_TX_P1_224	AG6
PER2_N	MGT_TX_N1_224	AG5
PER3_P	MGT_TX_P0_224	AH4
PER3_N	MGT_TX_N0_224	AH3
PER4_P	MGT_TX_P3_223	AJ6
PER4_N	MGT_TX_N3_223	AJ5
PER5_P	MGT_TX_P2_223	AL6
PER5_N	MGT_TX_N2_223	AL5
PER6_P	MGT_TX_P1_223	AM4
PER6_N	MGT_TX_N1_223	AM3
PER7_P	MGT_TX_P0_223	AN6
PER7_N	MGT_TX_N0_223	AN5
PET0_P	MGT_RX_P3_224	AE2
PET0_N	MGT_RX_N3_224	AE1
PET1_P	MGT_RX_P2_224	AF4
PET1_N	MGT_RX_N2_224	AF3
PET2_P	MGT_RX_P1_224	AG2
PET2_N	MGT_RX_N1_224	AG1
PET3_P	MGT_RX_P0_224	AJ2
PET3_N	MGT_RX_N0_224	AJ1
PET4_P	MGT_RX_P3_223	AK4
PET4_N	MGT_RX_N3_223	AK3
PET5_P	MGT_RX_P2_223	AL2
PET5_N	MGT_RX_N2_223	AL1
PET6_P	MGT_RX_P1_223	AN2
PET6_N	MGT_RX_N1_223	AN1
PET7_P	MGT_RX_P0_223	AP4
PET7_N	MGT_RX_N0_223	AP3

2.19 20P expansion interface

CR-P079D reserves a 20P 2.54 mm pitch connector for extended signal connection.

BANK68/87/88 of FPGA, and the level is 3.3V. The chip location of the signal is marked as follows. For detailed connection relationship, refer to the schematic diagram.

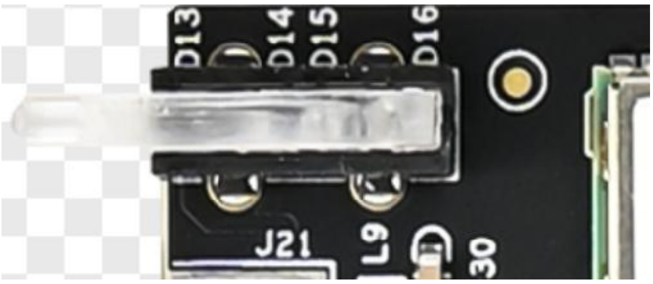
JM 1 signal sequence	Pin Name	Pin Location	JM 1 signal sequence	Pin Name	Pin Location
5	IO_L10N_88	A5	6	IO_L5N_87	M8
7	IO_L10P_88	B5	8	IO_L5P_87	M9
9	IO_L9N_87	J6	10	IO_L6N_87	L10
11	IO_L9P_87	J7	12	IO_L6P_87	M10
13	IO_L3N_87	M12	14	IO_L10N_87	G6
15	IO_L3P_87	N13	16	IO_L10P_87	H6
17	IO_L10N_68	D9	18	IO_L22N_68	A10
19	IO_L10P_68	E9	20	IO_L22P_68	B10
21	IO_L23N_68	A7	22	IO_L4N_68	J11
23	IO_L23P_68	A8	24	IO_L4P 68	K12



2.20 LED Indicator

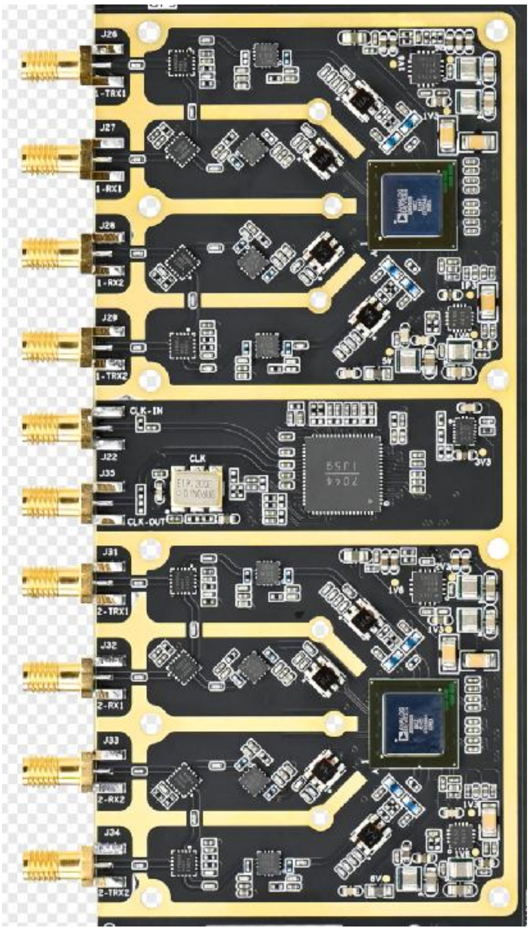
CR-P079D is designed with four LEDs, two of which can be controlled by GPIO, and the other two are power indication and GPS-PPS status indication. The two controllable LED lights are used to indicate the system status and RF status, high level lights on, low level off. For detailed circuits, please refer to the development board schematics.

LED position number	Pin Name	Pin Location
LED_RF	IO_L4P_88_89	E3
LED_SYS	IO_L4N_88_89	E2



2.21 ADRV9009 Introduction

The RF part of CR-P079D uses ADRV9009 from ADI. In this section, we will introduce the RF link, data channel, and clock in detail.



2.21.1 RF front-end circuit

The RF front-end circuit involves three parts: balun, power amplifier, and RF switch. The bandwidth of the balun is 10M-8Ghz, covering the communication bandwidth of ADRV9009.

The bandwidth of the power amplifier is 10M-10Ghz, which also covers the communication bandwidth of ADRV9009. The gain linearity of the power amplifier within the entire communication bandwidth is very good. The following table shows the detailed indicators of the power amplifier at each frequency point.

FREQ	Gain	Isolation	Input Return Loss	Output Return Loss	Stability		IP-3 Output	1dB Comp. Output	Noise Figure
(MHz)	(dB)	(dB)	(dB)	(dB)	K	Measure	(dBm)	(dBm)	(dB)
10	20.46	27.17	9.18	14.25	1.15	0.87	25.43	19.41	8.92
100	22.20	25.13	22.46	21.95	1.05	0.50	30.65	22.45	1.37
200	22.28	25.07	23.42	23.85	1.04	0.48	28.68	22.50	1.06
300	22.29	25.08	23.27	24.74	1.05	0.49	29.17	22.55	1.02
400	22.29	25.15	22.98	25.12	1.05	0.50	27.58	22.54	0.97
500	22.29	25.19	22.58	25.57	1.05	0.50	29.99	22.55	0.96
1000	22.28	25.22	19.66	27.67	1.05	0.52	29.94	22.67	0.94
1200	22.28	25.25	18.42	27.51	1.05	0.52	31.22	22.78	0.96
1400	22.27	25.35	17.29	26.20	1.06	0.54	29.62	22.80	0.91
1600	22.26	25.42	16.20	24.55	1.06	0.55	29.97	22.83	0.94
1800	22.25	25.45	15.30	22.84	1.06	0.55	31.54	22.80	0.96
2000	22.23	25.55	14.44	21.32	1.06	0.57	32.31	22.68	0.97
2200	22.21	25.62	13.69	20.06	1.07	0.58	33.26	22.75	0.93
2400	22.18	25.67	13.06	19.05	1.07	0.58	29.73	22.78	1.07
2600	22.17	25.86	12.58	18.29	1.08	0.60	28.43	22.65	0.98
2800	22.16	25.88	12.19	17.80	1.08	0.61	30.87	22.38	1.05
3000	22.16	25.94	11.94	17.47	1.08	0.62	29.72	22.10	0.99
3200	22.16	26.04	11.74	17.30	1.08	0.63	28.81	21.77	1.06
3400	22.16	26.12	11.63	17.22	1.09	0.64	28.42	21.40	1.04
3600	22.16	26.20	11.60	17.21	1.09	0.64	28.39	21.13	1.06
3800	22.18	26.24	11.60	17.36	1.09	0.65	28.66	21.56	1.05
4000	22.20	26.27	11.70	17.64	1.09	0.65	29.25	21.51	1.16
4200	22.22	26.35	11.87	18.05	1.10	0.66	30.11	21.70	1.14
4400	22.24	26.42	12.10	18.50	1.10	0.67	28.80	21.74	1.19
4600	22.27	26.45	12.36	19.04	1.10	0.67	29.16	21.61	1.14
4800	22.32	26.55	12.67	19.61	1.11	0.68	29.37	21.83	1.19
5000	22.37	26.55	13.02	20.26	1.11	0.68	30.08	21.69	1.21
5200	22.43	26.66	13.44	20.86	1.12	0.69	28.61	21.57	1.22
5400	22.48	26.67	13.87	21.44	1.12	0.68	29.58	21.33	1.27
5600	22.55	26.67	14.42	21.98	1.12	0.68	28.42	21.15	1.23
5800	22.61	26.80	15.06	22.61	1.12	0.69	29.99	21.12	1.22
6000	22.66	26.85	15.80	23.09	1.13	0.69	28.20	21.28	1.22
6200	22.73	26.92	16.75	23.01	1.13	0.69	28.94	21.09	1.10
6400	22.77	26.98	17.74	22.66	1.14	0.69	29.82	21.04	1.20
6600	22.81	27.06	19.02	21.83	1.15	0.69	30.01	21.24	1.14
6800	22.86	27.19	20.71	20.64	1.16	0.70	29.50	21.05	1.15
7000	22.91	27.25	22.82	19.57	1.16	0.70	28.62	20.90	1.17
7200	22.94	27.35	24.91	18.68	1.17	0.70	29.79	20.90	1.14
7400	22.94	27.41	26.72	17.99	1.18	0.70	28.14	20.60	1.16
7600	22.93	27.57	26.69	17.33	1.20	0.71	30.13	20.20	1.15
7800	22.92	27.73	25.02	16.70	1.22	0.72	28.81	20.10	1.19
8000	22.89	27.96	23.01	16.34	1.25	0.74	29.42	19.59	1.23
8200	22.84	28.11	20.99	16.14	1.27	0.75	28.14	19.10	1.23
8400	22.78	28.34	19.42	16.02	1.30	0.77	28.40	18.78	1.23
8600	22.70	28.59	18.18	16.27	1.34	0.79	27.50	18.22	1.25
8800	22.59	28.83	17.09	16.71	1.39	0.82	27.89	18.12	1.33
9000	22.46	29.19	16.24	17.37	1.45	0.84	28.51	18.14	1.45
9200	22.31	29.42	15.50	18.23	1.51	0.87	28.63	17.44	1.59
9400	22.13	29.81	14.75	19.22	1.60	0.89	27.39	17.01	1.65
9600	21.89	30.15	14.06	20.07	1.69	0.92	28.06	16.83	1.83
9800	21.59	30.58	13.41	20.21	1.80	0.94	26.04	16.17	2.00
10000	21.25	31.03	12.70	19.46	1.94	0.96	27.73	16.12	2.14

The RF switch uses SPDT with one input and two outputs, with a bandwidth of 9K-8G, and an electrostatic protection circuit is integrated inside the RF switch to effectively protect the RF port. The switching logic of the corresponding RF switch can be referred to the table below. For the TX/RX switching of ADRV9009, you can refer to the actual connection relationship in the schematic diagram to make corresponding adjustments.

LS	CTRL	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

2.21.2 ADRV9009 Communication Ports

The ADRV9009 digital port is divided into two parts: data port and control port. The pin correspondence of the data port is listed in the following table. You can also refer to the CR-P079D schematic diagram and the corresponding engineering code.

1_ADRV9009 interface	Pin Name	Pin Location
1_ADRV9009_SERDIN_P0	MGT_TX_P3_226	N6
1_ADRV9009_SERDIN_N0	MGT_TX_N3_226	N5
1_ADRV9009_SERDIN_P1	MGT_TX_P2_226	R6
1_ADRV9009_SERDIN_N1	MGT_TX_N2_226	R5
1_ADRV9009_SERDIN_P2	MGT_TX_P1_226	T4
1_ADRV9009_SERDIN_N2	MGT_TX_N1_226	T3
1_ADRV9009_SERDIN_P3	MGT_TX_P0_226	U6
1_ADRV9009_SERDIN_N3	MGT_TX_N0_226	U5
1_ADRV9009_SYNCIN_P0	IO_L21P_68_69	B6
1_ADRV9009_SYNCIN_N0	IO_L21N_68_69	A6
1_ADRV9009_SYNCIN_P1	IO_L9P_68_69	F8
1_ADRV9009_SYNCIN_N1	IO_L9N_68_69	E8
1_ADRV9009_SERDOUT_P0	MGT_RX_P3_226	P4
1_ADRV9009_SERDOUT_N0	MGT_RX_N3_226	P3
1_ADRV9009_SERDOUT_P1	MGT_RX_P2_226	R2
1_ADRV9009_SERDOUT_N1	MGT_RX_N2_226	R1
1_ADRV9009_SERDOUT_P2	MGT_RX_P1_226	U2
1_ADRV9009_SERDOUT_N2	MGT_RX_N1_226	U1
1_ADRV9009_SERDOUT_P3	MGT_RX_P0_226	V4
1_ADRV9009_SERDOUT_N3	MGT_RX_N0_226	V3
1_ADRV9009_SYNCOUT_P0	IO_L24P_68_69	B11
1_ADRV9009_SYNCOUT_N0	IO_L24N_68_69	A11
1_ADRV9009_SYNCOUT_P1	IO_L6P_67_68	C13
1_ADRV9009_SYNCOUT_N1	IO_L6N_67_68	C12
1_ADRV9009_TX_ENABLE1	IO_L20N_68_69	B8
1_ADRV9009_TX_ENABLE2	IO_L8P_68_69	C9
1_ADRV9009_RX_ENABLE1	IO_L5N_68_69	J14
1_ADRV9009_RX_ENABLE2	IO_L20P_68_69	B9
1_ADRV9009_SPI_CLK	IO_L15P_68_69	H13
1_ADRV9009_SPI_CS	IO_L15N_68_69	H12
1_ADRV9009_SPI_DI	IO_L3N_68_69	L11
1_ADRV9009_SPI_DO	IO_L6N_68_69	K13
1_ADRV9009_nRST	IO_L7N_68_69	E7
1_ADRV9009_GP_INT	IO_L1P_68_69	M13
1_ADVR9009_GPIO_0	IO_L8N_68_69	C8
1_ADVR9009_GPIO_1	IO_L3P_68_69	L12
1_ADVR9009_GPIO_2	IO_L1N_68_69	L13
1_ADVR9009_GPIO_3	IO_L6P_68_69	L14
1_ADVR9009_GPIO_4	IO_L19N_68_69	C6
1_ADVR9009_GPIO_5	IO_L19P_68_69	C7

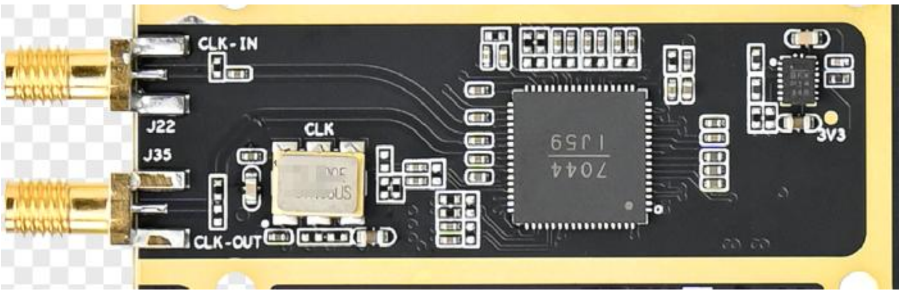
1_ADVR9009_GPIO_6	IO_L17P_68_69	F12
1_ADVR9009_GPIO_7	IO_L17N_68_69	E12
1_ ADVR9009_GPIO_8	IO_L5N_68_69	A12
1_ADVR9009_GPIO_9	IO_L5P_68_69	A13
1_ADVR9009_GPIO_10	IO_L10N_67_68	F13
1_ADVR9009_GPIO_11	IO_L5P_68_69	K14
1_ADVR9009_GPIO_12	IO_L13N_68_69	G11
1_ADVR9009_GPIO_13	IO_L13P_68_69	H11
1_ADVR9009_GPIO_14	IO_L18P_68_69	D12
1_ADVR9009_GPIO_15	IO_L18N_68_69	C11
1_ADVR9009_GPIO_16	IO_L12P_68_69	G10
1_ADVR9009_GPIO_17	IO_L12N_68_69	F10
1_ADVR9009_GPIO_18	IO_L7P_68_69	F7

2_ADRV9009 Interface	Pin Name	Pin Location
2_ADRV9009_SERDIN_P0	MGT_TX_P3_225	W6
2_ADRV9009_SERDIN_N0	MGT_TX_N3_225	W5
2_ADRV9009_SERDIN_P1	MGT_TX_P2_225	Y4
2_ADRV9009_SERDIN_N1	MGT_TX_N2_225	Y3
2_ADRV9009_SERDIN_P2	MGT_TX_P1_225	AA6
2_ADRV9009_SERDIN_N2	MGT_TX_N1_225	AA5
2_ADRV9009_SERDIN_P3	MGT_TX_P0_225	AC6
2_ADRV9009_SERDIN_N3	MGT_TX_N0_225	AC5
2_ADRV9009_SYNCIN_P0	IO_L21P_67_68	K17
2_ADRV9009_SYNCIN_N0	IO_L21N_67_68	J17
2_ADRV9009_SYNCIN_P1	IO_L15P_67_68	H19
2_ADRV9009_SYNCIN_N1	IO_L15N_67_68	G19
2_ADRV9009_SERDOUT_P0	MGT_RX_P3_225	W2
2_ADRV9009_SERDOUT_N0	MGT_RX_N3_225	W1
2_ADRV9009_SERDOUT_P1	MGT_RX_P2_225	AA2
2_ADRV9009_SERDOUT_N1	MGT_RX_N2_225	AA1
2_ADRV9009_SERDOUT_P2	MGT_RX_P1_225	AB4
2_ADRV9009_SERDOUT_N2	MGT_RX_N1_225	AB3
2_ADRV9009_SERDOUT_P3	MGT_RX_P0_225	AC2
2_ADRV9009_SERDOUT_N3	MGT_RX_N0_225	AC1
2_ADRV9009_SYNCOUT_P0	IO_L13P_MRCC_67_68	F17
2_ADRV9009_SYNCOUT_N0	IO_L13N_MRCC_67_68	F16
2_ADRV9009_SYNCOUT_P1	IO_L12P_MRCC_67_68	E15
2_ADRV9009_SYNCOUT_N1	IO_L12N_MRCC_67_68	E14
2_ADRV9009_TX_ENABLE1	IO_L3P_67_68	A15
2_ADRV9009_TX_ENABLE2	IO_L18N_67_68	G16
2_ADRV9009_RX_ENABLE1	IO_L2N_67_68	B15
2_ADRV9009_RX_ENABLE2	IO_L3N_67_68	A14
2_ADRV9009_SPI_CLK	IO_L19N_67_68	K20
2_ADRV9009_SPI_CS	IO_L24P_67_68	L17
2_ADRV9009_SPI_DI	IO_L19P_67_68	L20

2_ADRV9009_SPI_DO	IO_L9P_67_68	E18
2_ADRV9009_nRST	IO_L2P_67_68	B16
2 _ADRV9009_GP_INT	IO_L7N_67_68	C16
2_ADVR9009_GPIO_0	IO_L18P_67_68	H16
2_ADVR9009_GPIO_1	IO_L9N_67_68	E17
2_ADVR9009_GPIO_2	IO_L8P_67_68	D17
2_ADVR9009_GPIO_3	IO_L8N_67_68	C17
2_ADVR9009_GPIO_4	IO_L22P_67_68	L15
2_ADVR9009_GPIO_5	IO_L22N_67_68	K15
2_ADVR9009_GPIO_6	IO_L17N_67_68	F18
2_ADVR9009_GPIO_7	IO_L4P_67_68	B14
2_ADVR9009_GPIO_8	IO_L4N_67_68	B13
2_ADVR9009_GPIO_9	IO_L10P_67_68	G14
2_ADVR9009_GPIO_10	IO_L20P_67_68	J16
2_ADVR9009_GPIO_11	IO_L20N_67_68	J15
2_ADVR9009_GPIO_12	IO_L1N_67_68	A16
2_ADVR9009_GPIO_13	IO_L1P_67_68	A17
2_ADVR9009_GPIO_14	IO_L24N_67_68	L16
2_ADVR9009_GPIO_15	IO_L23P_67_68	K19
2_ADVR9009_GPIO_16	IO_L16N_67_68	H17
2_ADVR9009_GPIO_17	IO_L16P_67_68	H18
2_ADVR9009_GPIO_18	IO_L23N_67_68	K18

2.21.3 ADRV9009 clock circuit

The input clock of ADRV9009 uses a high-precision VCXO clock with a frequency of 122.88Mhz. The required multi-channel clocks are generated through a dedicated clock chip. At the same time, CR-P079D reserves clock input and output interfaces. If the user needs a higher-precision clock, the clock can be injected from the outside and the required clock can be output. For the detailed use of the clock, please refer to the schematic diagram and code engineering provided by Puzhi for programming.



2.22 GPS Module

A GPS module is integrated on the baseboard, which can realize GPS and Beidou positioning functions. We can configure and read GPS module data through UART, and the module also provides PPS signal. The following table lists the pin correspondence of the GPS module. For more detailed explanation, please refer to the schematic diagram provided.

GPS Module	Pin Name	Pin Location
GPS_UART_TXD	IO_3P_88_89	A3
GPS_UART_RXD	IO_3N_88_89	A2
GPS_CLK_10M	IO_5N_88_89	C2
GPS_nRESET	IO_6P_88_89	B3
GPS_PPS	IO_6P_88_89	C3