

# Shenzhen Leadtek Electronics Co.,Ltd

## PRODUCT SPECIFICATION

### TFT-LCD MODULE

**Module No:** LTK040WVBLM13-V0

☒ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
<i>jona</i>	<i>tom</i>	<i>lan</i>

### Final Approval by Customer

Approved by	Comment

※The specification of "TBD" should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.



# 1.Document Revision History

Version	Contents	Date	Note
V0	Original	2022.12.21	



## 2. General Description

No	Item	Specification	Unit
1	Screen Size	3.97	inch
2	LCD Type	TFT	
3	Viewing Direction	Î ÈÒ'CLOCK	Best Image
4	Display Mode	480*3RGB (H) X800 (V)	
5	Resolution	Normally White	Pixel
6	Active Area	51.84 (H) *86.40 (V)	mm
7	ŠÔT ÁOutline Dimension	57.14 (H) *96.85 (V) *1.96 (T)	mm
8	Driver IC	ŠQİ Ė Ò	without RAM
9	Interface	2 lines MIPI	
10	Back Light	White Led*8	

## 3. Mechanical Drawing



## 4. Interface Specification

NO.	Symbol	Function	Remark
1	CPT-GND	Touch Ground	
2	CTP-VDD	Touch panel Power supply 2.8~3.3V	
3	CTP-SCL	Touch panel I2C clock	
4	CTP-SDA	Touch panel I2C data	
5	CTP-INT	Touch panel interrupt output	
6	CTP-RES	Touch panel reset	
7	GND	Power Ground	
8	GND	Power Ground	
9	MIPI_D0N	MIPI_DP0- are differential data signal line	
10	MIPI_D0P	MIPI_DP0+ are differential data signal line	
11	GND	Power Ground	
12	MIPI_CLKN	MIPI_CLKN Lane positive-end input pin	
13	MIPI_CLKP	MIPI_CLKP Lane engative-end input pin	
14	GND	Power Ground	
15	MIPI_D1N	MIPI_DP1- are differential data signal line	
16	MIPI_D1P	MIPI_DP1+ are differential data signal line	
17	GND	Power Ground	
18	RESET	Reset signal input terminal. Active at 'L'.	
19	TE	Tearing effect output pin is used to synchronize MCU	
20	IOVCC	Power supply for interface logic circuits(1.65~3.3V)	

21	VCI	LCM Analog supply voltage (2.8~3.3V)	
22	NC	Not connect	
23	LEDA	LED anode.	
24	NC	Not connect	
25	LEDK	LED cathode	

## 5.Electrical Characteristics

### 5.1TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	IOVCC	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VCC	2.6	2.8	3.6	V

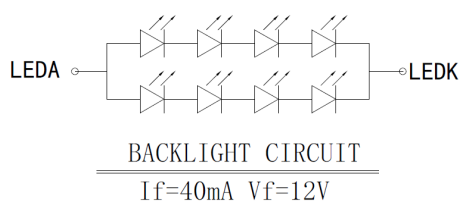
### 5.2 LED Backlight Specification

The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Item	Symbol	Min	Typ	Max	Unit	Notes
Backlight voltage	Vf	--	12.0	--	V	--
Forward current	IF	--	40	--	mA	--
Luminance(With LCD)	Lv	--	350	--	cd/m <sup>2</sup>	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:(1) The "LED life time" is defined as the module brightness decrease to 50% of original brightness at IL=20mA/LED. The LED life time could be decreased if operating IL is larger than 25mA/LED.

#### LED circuit:

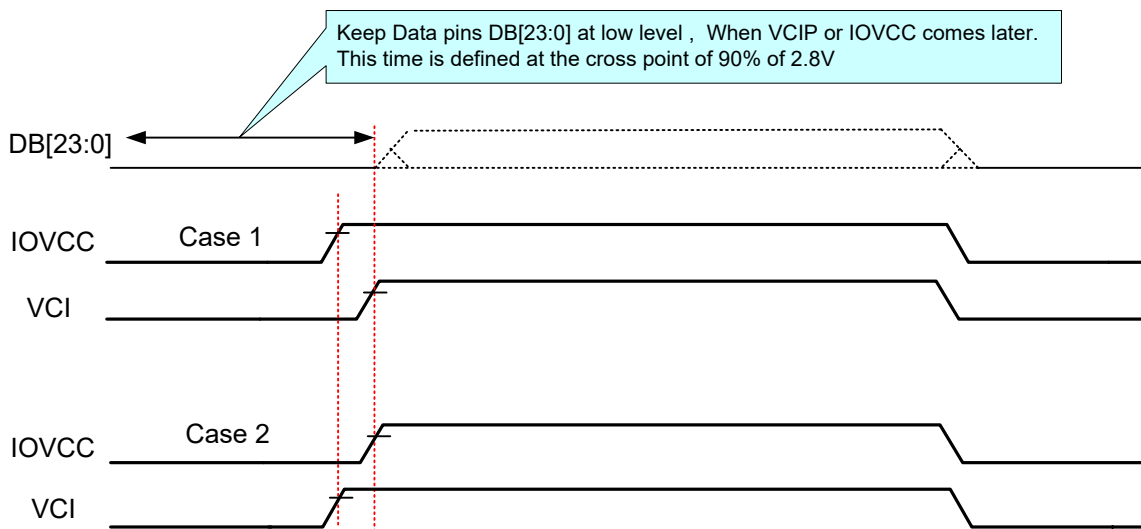


## 6. Power ON/OFF Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

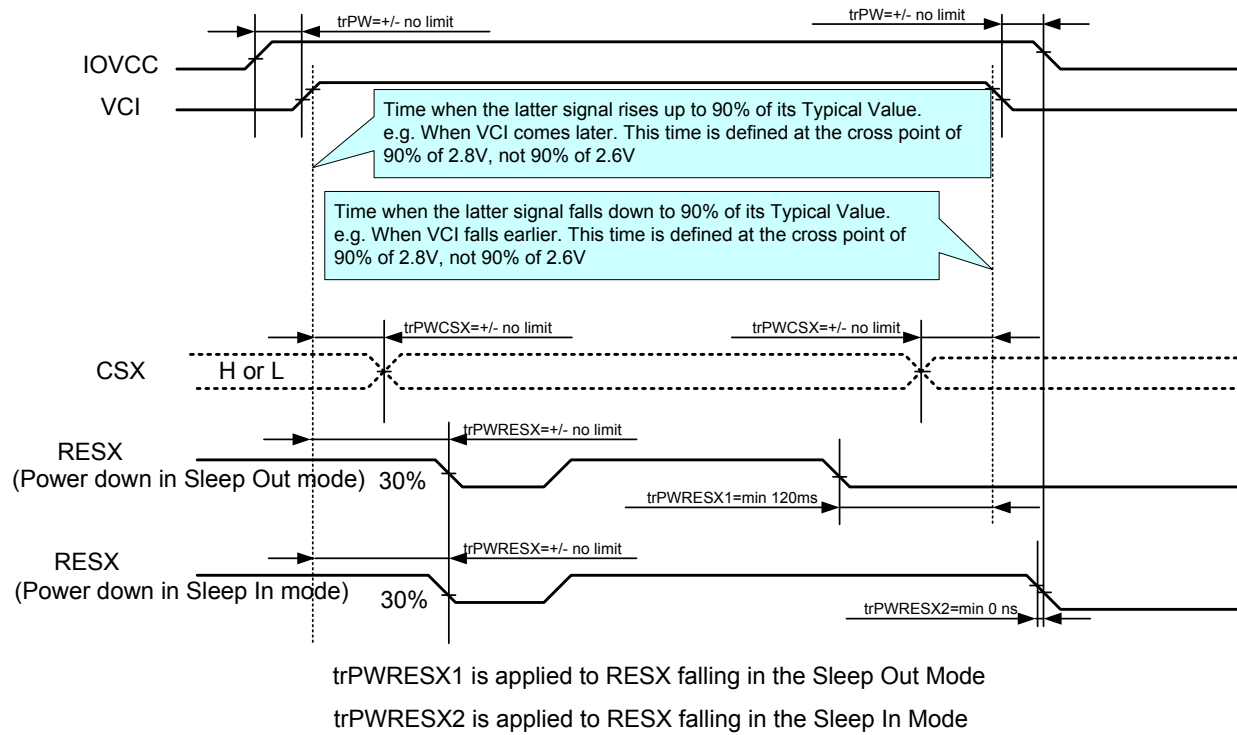
Note:

- There will be no damage to ILI9806E if the power sequences are not met.
- There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
- There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
- If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
- Keep data pins DB[23:0] at low level, when VCIP or IOVCC comes later.



## 6.1. Case 1 –RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.





## 7.0 DSI Timing Characteristics

### 7.1 High Speed Mode – Clock Channel Timing

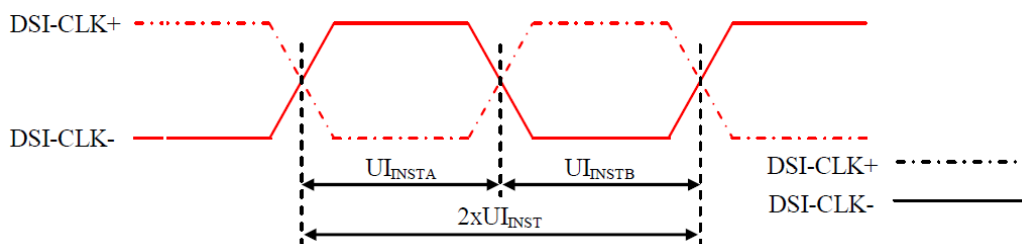


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2 \times UI_{INST}$	Double UI instantaneous	4	2	ns
DSI-CLK+/-	$UI_{INSTA}, UI_{INSTB}$	UI instantaneous Half	2	12.5	ns

Note:  $UI = UI_{INSTA} = UI_{INSTB}$

### 7.2 High Speed Mode – Data Clock Channel Timing

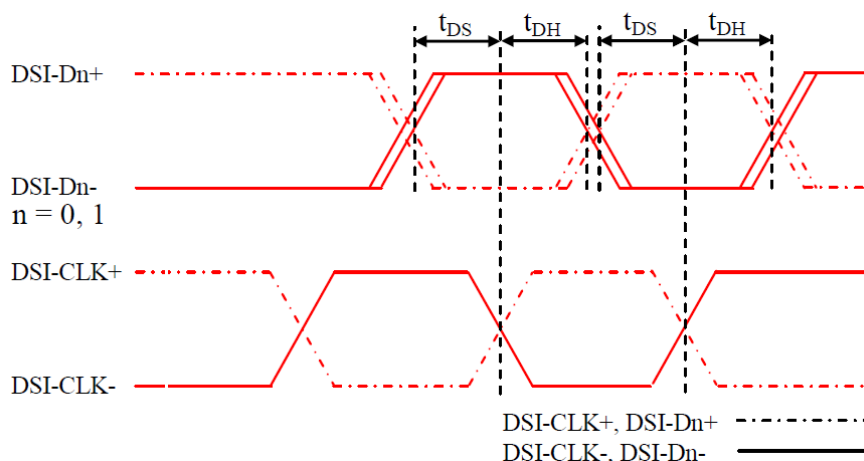


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	$t_{DS}$	Data to Clock Setup time	$0.15 \times UI$	-
	$t_{DH}$	Clock to Data Hold Time	$0.15 \times UI$	-

### 7.3 High Speed Mode – Rise and Fall Timings

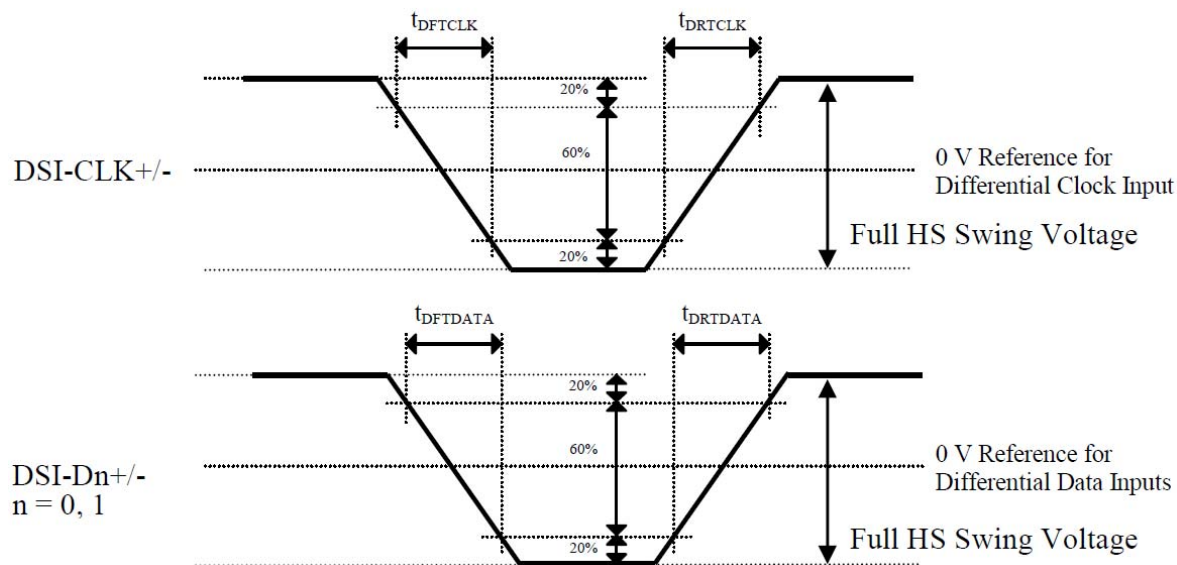


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Differential Rise Time for Clock	$t_{DRTCLK}$	DSI-CLK+/-	-	-	150 (Note )	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note )	ps
Differential Fall Time for Clock	$t_{DFTCLK}$	DSI-CLK+/-	-	-	150 (Note )	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note )	ps

Note: The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

## 7.4. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI9806E) sequence below.

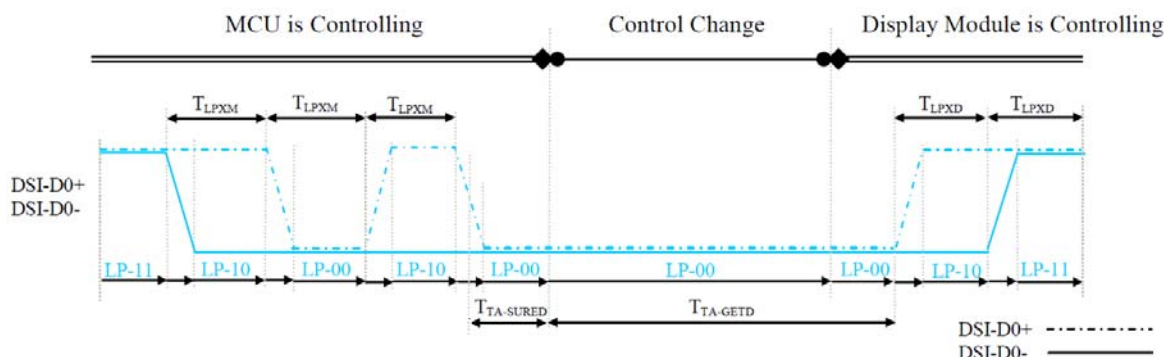


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (ILI9806E) to the MPU sequence below.

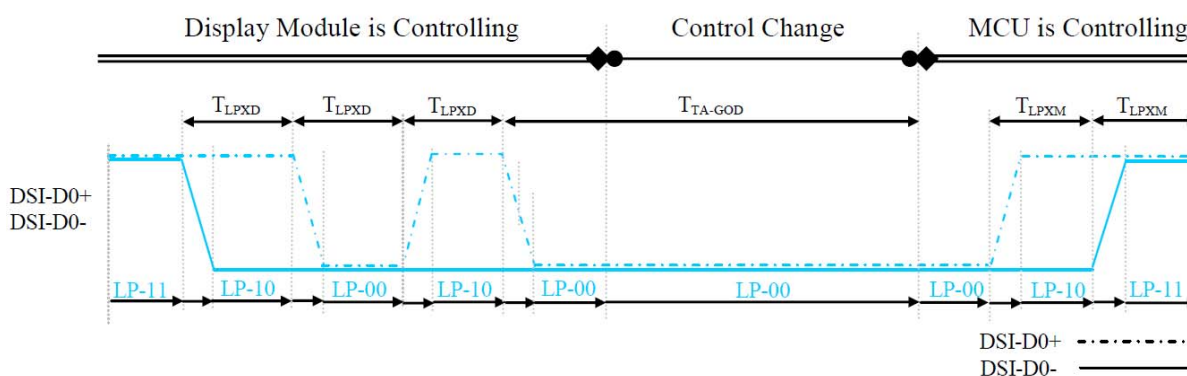


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	$T_{LPXM}$	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module (ILI9806E)	50	75	ns
DSI-D0+/-	$T_{LPXD}$	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9806E) → MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI9806E) starts driving	$T_{LPXD}$	$2 \times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9806E)	$5 \times T_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GOD}$	Time to drive LP-00 after turnaround request – MPU	$4 \times T_{LPXD}$	ns

## 7.5 Data Lanes from Low Power Mode to High Speed Mode

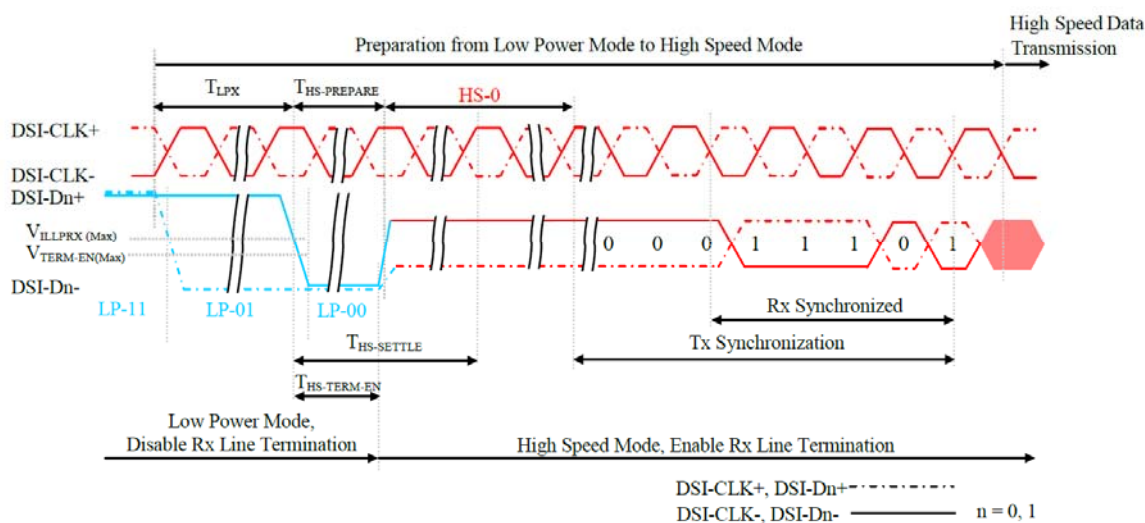


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{LPX}$	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xUI$	$85+6xUI$	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	$35+4xUI$	ns

## 7.6 Data Lanes from High Speed Mode to Low Power Mode

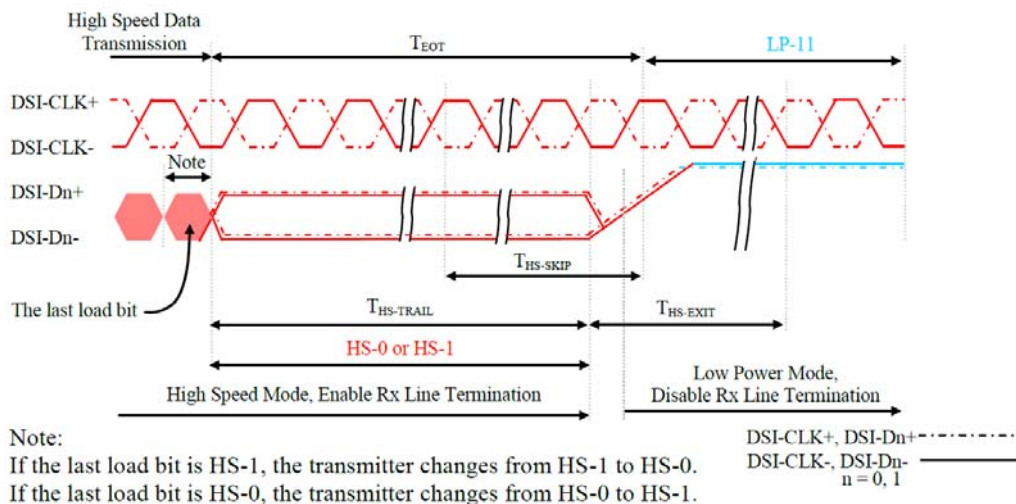
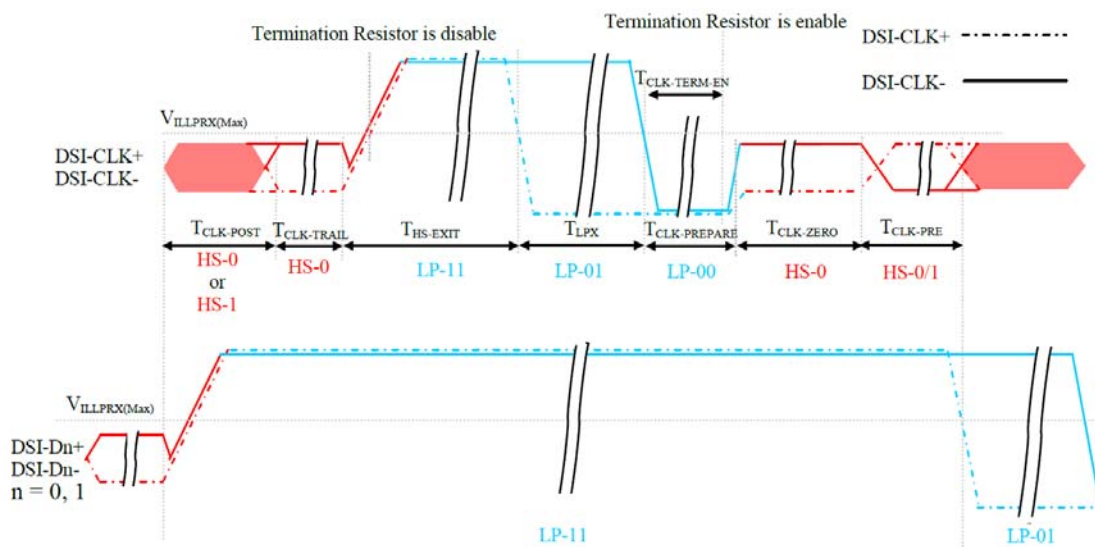


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9806E) to ignore transition period of EoT	40	$55+4xUI$	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	n

## 7.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode



**Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings**

**Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings**

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52 \times UI$	-	n
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	n
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	n
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	n
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8 \times UI$	-	n

## 8.0 OPTICAL SPECIFICATION

### 8.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance  $\leq 1\text{lux}$  and temperature =  $25\pm 2^{\circ}\text{C}$ ) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of  $\theta$  and  $\Phi$  equal to  $0^{\circ}$ . The center of the measuring spot on the Display surface shall stay fixed.

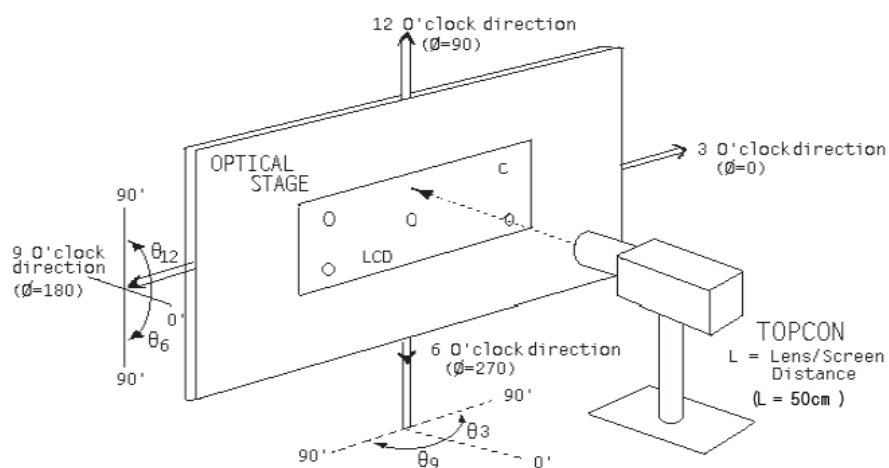
The backlight should be operating for 30 minutes prior to measurement.

### 8.2 Optical Specifications

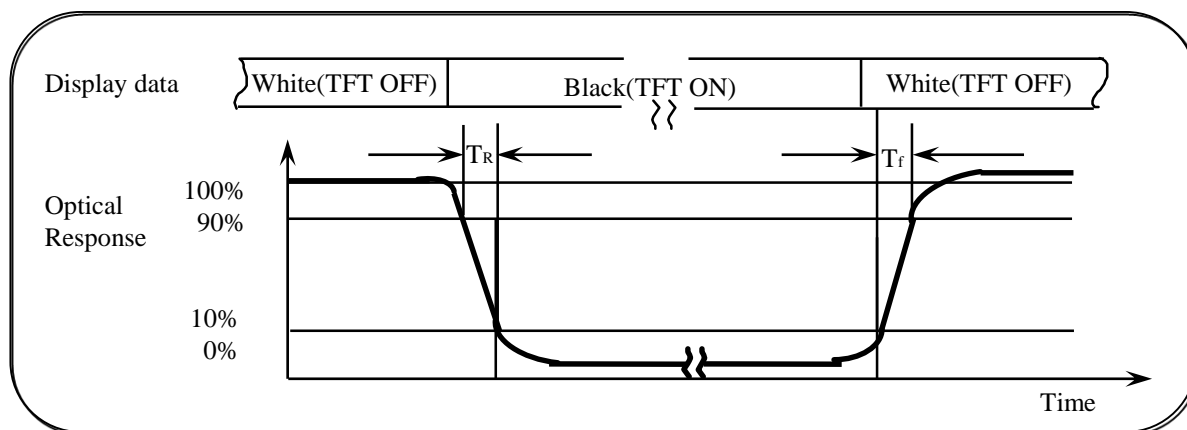
<Table 6. Optical Specifications >

Table 6: Optical Specifications								
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ3	CR>10	60	70	-	Deg.	Note1
		Θ9		60	70	-	Deg.	
	Vertical	Θ12		60	70	-	Deg.	
		Θ6		50	60	-	Deg.	
Contrast ratio		CR	Θ = 0°	500	700	-		Note2
Transmittance		Tr		3.6	4.0		%	Note3
Reproduction of color	Red	Rx	Θ = 0°	0.603	0.632	0.662		Note4 (Based on C Light)
		Ry		0.301	0.331	0.361		
	Green	Gx		0.247	0.277	0.307		
		Gy		0.515	0.545	0.575		
	Blue	Bx		0.109	0.139	0.169		
		By		0.106	0.136	0.166		

**Figure1 Measurement Set Up**



**Figure2 Response Time Testing**





## 9. Reliability Test Items

Item	Test Condition	Criterion
High Temperature Operation	60 °C, 48 hrs	Note1, Note2
Low temperature operation	-10 °C, 48 hrs	
High Temperature Storage	70 °C, 48 hrs	
Low Temperature Storage	-20 °C, 48 hrs	
High Temp. & High Humidity Storage	40 °C, 80% RH, 48hrs	
Thermal Shock (Static)	-20°C, 30 min /60°C, 30 min, 20 cycles	

Note1: Evaluation should be tested after storage at room temperature for two hours.

Note2:

Pass: Normal display image no line defect.

Fail: No display image, or line defects.

Partial transformation of the module parts should be ignored.

## 10. Precautions

Please pay attentions to the followings as using the LCD module.

### Handling

- (a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.
- (b) Because the polarizer is very fragile and easy to be damaged, do not hit, press or rub the display's surface with hard materials.
- (c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.
- (d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.



- (e) Avoid using Ketone type materials (e.g. Acetone), Toluene, Ethyl acid or Methyl chloride to clean the display surface. It might damage the touch panel surface permanently. The recommended solvents are water and Isopropyl alcohol.
- (f) Wipe off water droplets or oil immediately.
- (g) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.
- (h) Do not touch the output pins directly with bare hands.
- (i) Do not disassemble the LCD module.
- (j) Do not lift the FPC of Touch Panel.

## 11. Storage

- (a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.
- (b) Do not expose the LCD modules to sunlight directly.
- (c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.
- (d) Avoid condensation of water. It may cause improper operation.
- (e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

Operation (a) When mounting or dismounting the LCD modules, turn the power off.

- (b) Protect the LCD modules from electric shock.
- (c) The Driver IC control algorithms stated above should always be obeyed to avoid damaging the LSI and electronic circuit.
- (d) Be careful to avoid mixing up the polarity of power supply for backlight.
- (e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.
- (f) When a static image is displayed for a long time, remnant image is likely to occur.
- (g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.
- (h) Most of the touch screens have air vent to equalize the inside air pressure to the outside one. The air vent must

be open and liquid contact must be avoided as the liquid may be absorbed if the liquid is accumulated near the air vent.

(i) For the fragility of ITO film, it should avoid to use too tapering pen as the input material.

## 12.HSF Requirements

☒ RoHS( Restriction of the use of certain Hazardous Substances)

☐ HF (Halogen Free)

☐ REACH (Regulation the Registration, Evaluation, Authorization and Restriction of Chemicals)

☐ Other regulations

## 13.Packaging diagram

TBD

## 14.IIS Standard

### 14. INSPECTION STANDARD

#### 14.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

##### 14.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM CHENGHAO TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 TO 40 ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

##### 14.1.2. INCOMING INSPECTION

###### (A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

###### (B) THE STANDARD OF QUALITY

ISO-2859-1 ( SAME AS MIL-STD-105E ) , LEVEL SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

###### (C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED.

PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

##### 14.1.3. WARRANTY POLICY

CHENGHAO WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. U.R.T. WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF CHENGHAO.

#### 14.2. CHECKING CONDITION

14.2.1. CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

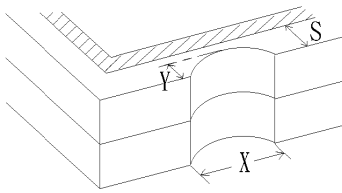
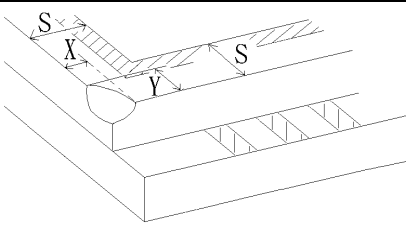
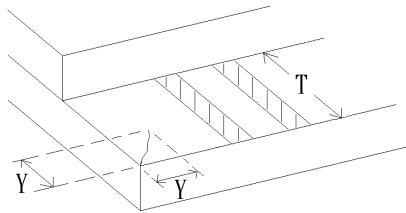
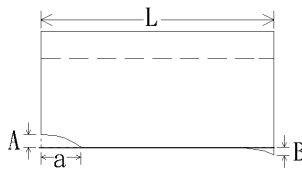
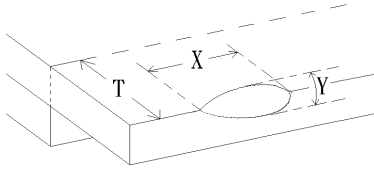
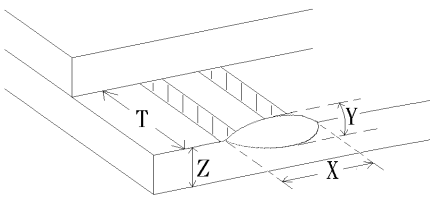
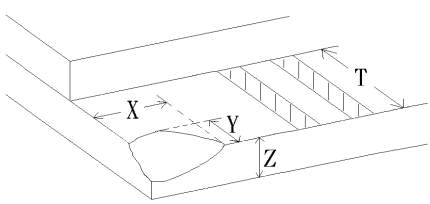
14.2.2. CHECKER SHALL SEE OVER 300±25 mm WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

### 14.3. INSPECTION PLAN :

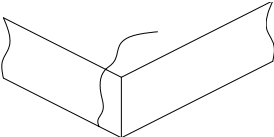
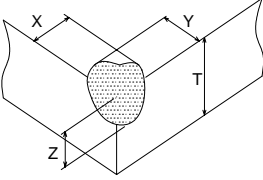
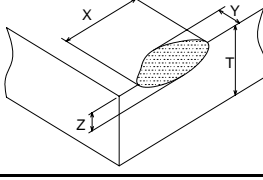
CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA .....REJECTED	Minor
	6. BLEMISH, BLACK SPOT, WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION ( INSIDE VIEWING AREA )	Minor
	7. BLEMISH, BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION ( INSIDE VIEWING AREA )	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION ( INSIDE VIEWING AREA )	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR ( OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE ( IF NEEDED, AND INSIDE VIEWING AREA )	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS ( CONTRAST, VOP, CHROMATICITY ... ETC )	ACCORDING TO SPECIFICATION OR DRAWING . ( INSIDE VIEWING AREA )	Critical
	11.MISSING LINE	MISSING DOT, LINE, CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT, WRONG PATTERN DISPLAY	NO DISPLAY, WRONG PATTERN DISPLAY, CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. DOT DEFECT (FOR COLOR AND TFT)	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

## 14.4. STANDARD OF VISUAL INSPECTION

NO.	CLASS	ITEM	JUDGEMENT																																	
14.4.1	MINOR	BLACK AND WHITE SPOT FOREIGN MATERIEL DUST IN THE CELL BLEMISH SCRATCH	<div>(A) ROUND TYPE: <span>unit : mm.</span><table><tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr><tr><td><math>\Phi \leq 0.1</math></td><td>DISREGARD</td></tr><tr><td><math>0.1 &lt; \Phi \leq 0.25</math></td><td>3 (D&gt;5mm)</td></tr><tr><td><math>0.25 &lt; \Phi</math></td><td>0</td></tr></table><div>NOTE: <math>\Phi=(\text{LENGTH}+\text{WIDTH})/2</math></div><div>(B) LINEAR TYPE: <span>unit : mm.</span><table><tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr><tr><td>-----</td><td><math>W \leq 0.03</math></td><td>DISREGARD</td></tr><tr><td><math>L \leq 5.0</math></td><td><math>0.03 &lt; W \leq 0.07</math></td><td>3 (D&gt;5mm)</td></tr><tr><td>-----</td><td><math>0.07 &lt; W</math></td><td>FOLLOW ROUND TYPE</td></tr></table></div></div>	DIAMETER (mm.)	ACCEPTABLE Q'TY	$\Phi \leq 0.1$	DISREGARD	$0.1 < \Phi \leq 0.25$	3 (D>5mm)	$0.25 < \Phi$	0	LENGTH	WIDTH	ACCEPTABLE Q'TY	-----	$W \leq 0.03$	DISREGARD	$L \leq 5.0$	$0.03 < W \leq 0.07$	3 (D>5mm)	-----	$0.07 < W$	FOLLOW ROUND TYPE													
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14.4.2	MINOR	BUBBLE IN POLARIZER DENT ON POLARIZER	<div><span>unit : mm.</span><table><tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr><tr><td><math>\Phi \leq 0.2</math></td><td>DISREGARD</td></tr><tr><td><math>0.2 &lt; \Phi \leq 0.5</math></td><td>2 (D&gt;5mm)</td></tr><tr><td><math>0.5 &lt; \Phi</math></td><td>0</td></tr></table></div>	DIAMETER	ACCEPTABLE Q'TY	$\Phi \leq 0.2$	DISREGARD	$0.2 < \Phi \leq 0.5$	2 (D>5mm)	$0.5 < \Phi$	0																									
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14.4.3	MINOR	Dot Defect	<div><table><tr><th>Items</th><th>ACC. Q'TY</th></tr><tr><td>Bright dot</td><td><math>N \leq 4</math> (D&gt;5mm)</td></tr><tr><td>Dark dot</td><td><math>N \leq 4</math> (D&gt;5mm)</td></tr></table><div>Pixel Define<table><tr><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td></tr><tr><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td></tr><tr><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td></tr></table></div><div>Not 1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot. Not 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. Not 3: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green ,blue pattern.</div></div>	Items	ACC. Q'TY	Bright dot	$N \leq 4$ (D>5mm)	Dark dot	$N \leq 4$ (D>5mm)	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
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R	G	B	R	G	B	R	G	B																												

NO.	CLASS	ITEM	JUDGEMENT
14.4.4	MINOR	LCD GLASS CHIPPING	 $Y > S$ Reject
14.4.5	MINOR	LCD GLASS CHIPPING	 $X \text{ or } Y > S$ Reject
14.4.6	MAJOR	LCD GLASS GLASS CRACK	 $Y > (1/2) T$ Reject
14.4.7	MAJOR	LCD GLASS SCRIBE DEFECT	 <ol style="list-style-type: none"> <li><math>a &gt; L/3</math> , <math>A &gt; 1.5\text{mm}</math>. Reject</li> <li>B : ACCORDING TO DIMENSION</li> </ol>
14.4.8	MINOR	LCD GLASS CHIPPING ( ON THE TERMINAL AREA )	 $= (x+y)/2 > 2.5 \text{ mm}$ Reject
14.4.9	MINOR	LCD GLASS CHIPPING ( ON THE TERMINAL SURFACE )	 $Y > (1/3) T$ Reject
14.4.10	MINOR	LCD GLASS CHIPPING	 $Y > T$ Reject

### 14.5 INSPECTION STANDARD OF TOUCH PANEL (Contains the CTP)

NO.	CLASS	ITEMS		JUDGEMENT	
14.5.1	MAJOR	Touch Panel Crack			Reject
14.5.2	MINOR	Touch Panel Chipping	Corner	 $X \leq 2\text{mm}, Y \leq 2\text{mm}, Z < 1/2T$	Accept
			Edge	 $X \leq 3\text{mm}, Y \leq 3\text{mm}, Z < 1/2T$	Accept
14.5.3	MINOR	Scratch Dust and Foreign materiel (Linear Type)	$W \leq 0.05, L \leq 5.0\text{mm}$		Accept
			$0.05\text{mm} < W \leq 0.07\text{mm}; L \leq 5.0\text{mm}$ Distance between scratch $> 5.0\text{mm}$		Accept 3 ea Max.
			$W > 0.07\text{mm}$		Reject
14.5.4	MINOR	Scratch Dust and Foreign materiel (Round Type : $\leq (\text{Length} + \text{Width})/2$ )	$0.25\text{mm}$		Accept
			$0.25\text{mm} < \leq 0.35\text{mm}$ Distance between spots $> 5.0\text{mm}$		Accept 5 ea Max.
			$> 0.35\text{mm}$		Reject
14.5.5	MINOR	Touch Panel Dent / Fish Eyes	$0.35\text{mm}$		Accept
			$0.35\text{mm} < \leq 1.0\text{mm}$ Distance $> 5.0\text{mm}$		Accept 3 ea Max.
			$> 1.0\text{mm}$		Reject
14.5.6	MINOR	Touch Panel Air Bubble	$0.2\text{mm}$		Accept
			$0.2\text{mm} < \leq 0.5\text{mm}$ Distance between bubbles $> 5.0\text{mm}$		Accept 3 ea Max.
			$> 0.5\text{mm}$		Reject
14.5.7	MINOR	Touch Panel Printing area Scratch	$0.03\text{mm} < W \leq 0.05\text{mm}, L \leq 5\text{mm}$ Distance between scratch $> 5.0\text{mm}$		Accept 3 ea Max.
			$W > 0.05\text{mm}$ or $L > 5\text{mm}$ ( $W > 0.05$ Follow 8.5.4 Round type )		Reject
14.5.8	MINOR	Touch Panel White Haze Mark / Dust		Can not be removed	Reject