Technical Note

Initialization Sequence for DDR SDRAM

Introduction

The double data rate (DDR) synchronous dynamic random access memory (SDRAM) device is a volatile and complex memory device. When power is removed from the device, all contents and operating configurations are assumed to be lost. Each time the memory is powered up, a predefined sequence of steps is required to initialize the internal state machines in the device and to configure various user-defined operating parameters.

This technical note describes the flow for the initialization sequence and the configurable device parameters.

Initializing DDR SDRAM

To ensure proper device functionality, a predefined sequence of 20 steps must be completed in conjunction with device power-up or a power-on reset:

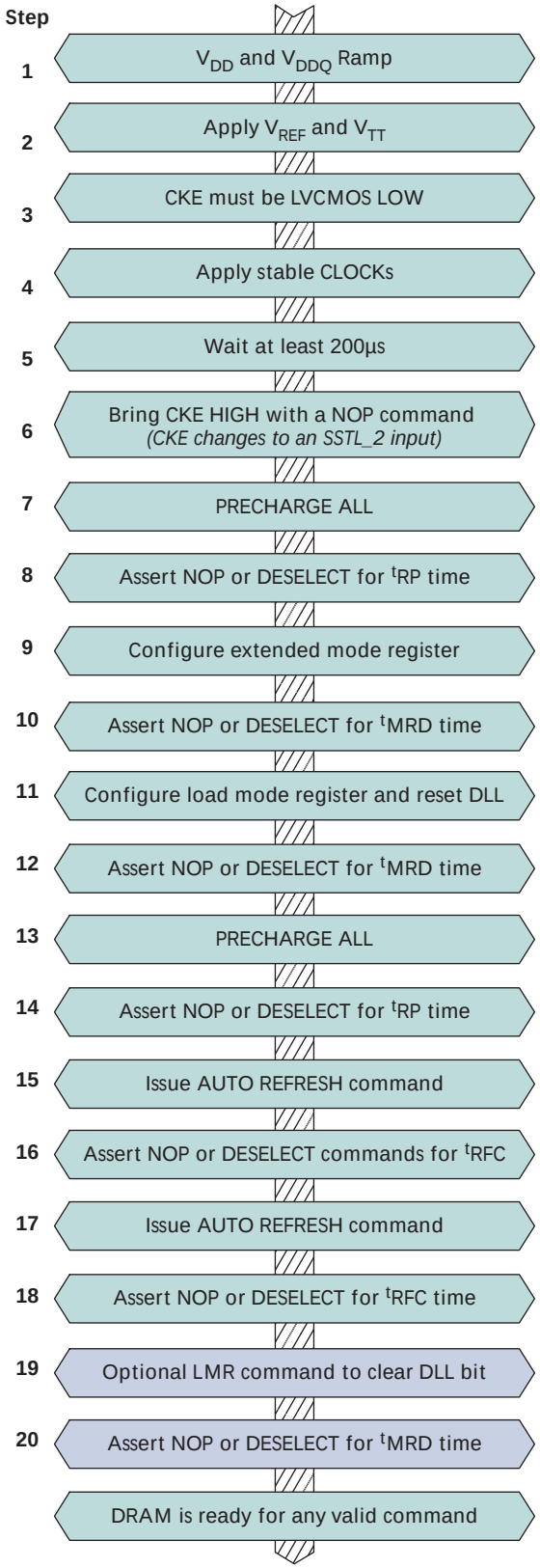
1. **Supply device power.** The device core power (V_{DD}) and device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. At all times, V_{DDQ} must be $\geq V_{IN(DC)max}$. Although not required, both V_{DD} and V_{DDQ} are typically from the same power source.
2. **Apply the reference voltage (V_{REF}) then the termination voltage (V_{TT}).** The reference voltage can ramp any time after V_{DDQ} and should always be equal to $V_{DDQ}/2$. During ramp, it is critical that the voltage at the device I/O pin does not exceed that of V_{DDQ}. Termination resistors may provide an IR drop between the actual V_{TT} levels and input voltage at the DRAM input.
3. **Assert and hold clock enable (CKE) to an LVCMOS logic LOW.** During the initial power ramp, the CKE input does not recognize SSTL_2 logic levels. A logic LOW on CKE prevents the DRAM from receiving unwanted commands and keeps the DRAM from driving the I/O pins.
4. **Provide a stable clock.** After the system has established reliable device power and CKE has been driven LOW, a stable clock is provided.
5. **Wait for 200µs of valid clocks.** At least 200µs of valid clocks are required before CKE goes HIGH and any command is sent to the DRAM.
6. **Initialize DRAM internal logic.** To initialize DRAM internal logic, bring CKE to an SSTL_2 logic HIGH and assert either a NO OPERATION (NOP) or DESELECT on the command bus. At this point, the CKE input transitions from an LVCMOS input to an SSTL_2 input only and thereafter remains an SSTL_2 input.
7. **Assert a PRECHARGE ALL command.**
8. **Provide NOP or DESELECT commands for at least ^{t}RP.**

9. **Program the extended mode register.** The LOAD MODE REGISTER (LMR) command is used to program the extended mode register. At this point, the delay-locked loop (DLL) and the I/O drive strength must be configured. To enable the DLL, set E0 = 0; for standard I/O drive, set E1 = 0; for reduced drive levels, set E1 = 1. All other bits must be set to 0.
10. P**rovide NOP or DESELECT commands for at least ^{t}MRD.**
11. **Program the mode register for the desired operating modes.** The LMR command is used to program the mode register operating modes. All mode register bits other than M[7:0] must be set to 0. This step also performs a DLL reset. Anytime a DLL reset occurs, 200 clock cycles must occur before any READ command can be issued.
12. **Provide NOP or DESELECT commands for at least ^{t}MRD.**
13. **Issue a PRECHARGE ALL command with A10 set to a logic HIGH.**
14. **Provide NOP or DESELECT commands for at least ^{t}RP.**
15. **Issue an AUTO REFRESH command.** As part of the initialization sequence, two AUTO REFRESH commands must be issued. The standard flow is to issue one at Step 15 and one at Step 17. Alternately, these may occur any time after Step 10.
16. **Provide NOP or DESELECT commands for at least ^{t}RFC.**
17. **Issue the second AUTO REFRESH command.**
18. **Provide NOP or DESELECT commands for at least ^{t}RFC.**
19. **Issue an LMR command to clear the DLL bit.** Although not required for Micron® devices, JEDEC requires an LMR command to clear the DLL bit (set M8 = 0). If an LMR command is issued, the same operating parameters should be set, as configured in Step 11.
20. **Provide NOP or DESELECT commands for at least ^{t}MRD.** The DRAM is now properly initialized and is ready for any valid command.

NOTE: 200 clock cycles are required between the DLL reset in Step 11 and any READ command.

NOTE: There is no RESET pin on any DDR components. The only way to reset a DDR SDRAM is to cycle power, then perform the initialization sequence.

Figure 1: Initialization Flow Diagram



Configuration of Operating Parameters

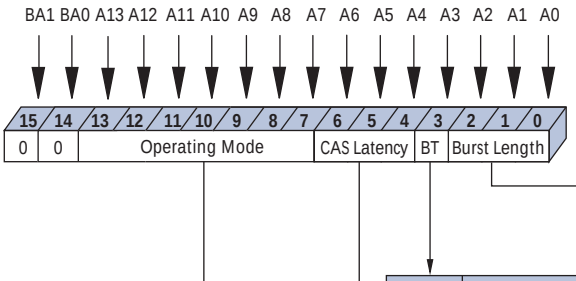
As part of the initialization sequence, the device operating parameters must be set. For standard DDR SDRAM this includes two internal registers, the mode register (MR), and the extended mode register (EMR).

The LMR command is used to program the mode registers. The LMR command is issued in conjunction with the DRAM bank addresses (BA[1:0]) and selects either the MR or the EMR. The DRAM row addresses (A[13:0]) provide the op-code to be written. The least significant row address corresponds to the least significant bit within the mode registers.

Mode Register

The mode register (MR) has seven configurable bits that can be dynamically updated to reflect changing system requirements. They include M[2:0], which are used to set the burst length; M3, which is used to set the burst type; M[6:4], which define the CAS latency; and M8, which is used to perform a DLL reset. All other bits are reserved for future use and must be set to 0. To address the mode register, set BA1 = 0 and BA0 = 0.

Figure 2: Mode Register



M3	Burst Type
0	Sequential
1	Interleaved

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (DDR400 only)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

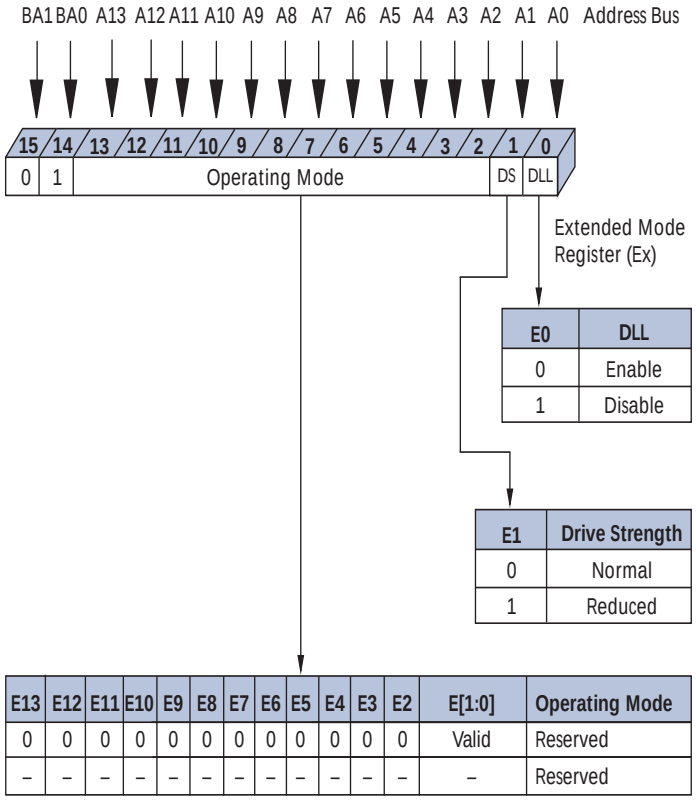
M13	M12	M11	M10	M9	M8	M7	M[6:0]	Operating Mode
0	0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
–	–	–	–	–	–	–	–	All other states reserved

Notes: 1. Set BA1 =0 and BA0 = 0 to access the mode register.
2. A13 is only used on the 1Gb device.
3. A12 is only used on 256Mb and larger devices.

Extended Mode Register

The extended mode register (EMR) has two configurable bits that usually are not changed after the device has been initialized. Bit E0 is used to enable the device DLL and bit E2 defines the output drive strength. All other bits are reserved for future use and must be set to 0. To point to the EMR, set BA1 = 0 and BA0 = 1.

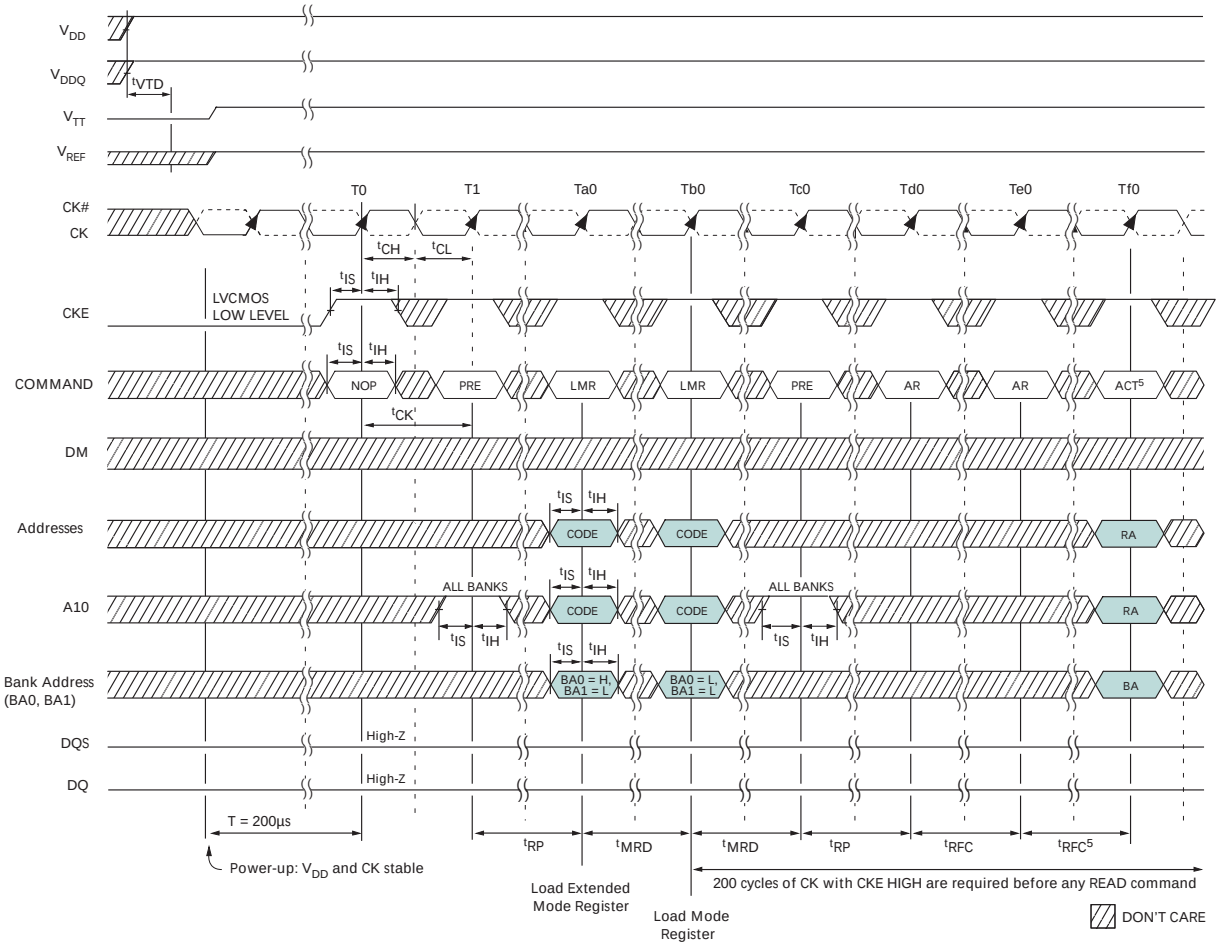
Figure 3: Extended Mode Register



E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E[1:0]	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	–	–	Reserved

Notes:
1. Set BA1 = 0 and BA0 = 1 to access the EMR.
2. A13 is only used on the 1Gb device.
3. A12 is only used on 256Mb and larger devices.
4. Reduced drive strength is available on x16 devices only.

Figure 4: Initialization Waveform Sequence



Summary

The proper DRAM initialization sequence must be followed whenever the device is first powered up or anytime there is an interruption in device power. Failure to follow documented steps will jeopardize device functionality. The steps in this technical note provide a general flow for proper initialization; for exact device timing or device voltage levels, refer to the DDR component data sheet(s). For the latest data sheets, refer to Micron's Web site at www.micron.com/products.

Revision History

Rev. C 8/10

- Initializing DDR SDRAM: Updated description.
- Figure 1: Initialization Flow Diagram: Updated figure.
- Updated template and formats.
- Minor grammatical corrections.

Rev. B 10/05

- Updated template.
- Corrected step 9.

Rev. A 1/04

- Initial release.